Université d'Ottawa
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Faculty of Engineering

School of Electrical Engineering
and Computer Science

CEG 4136 Computer Architecture III: Quiz #4

Date: November 30th

Professor: Dr. M. Bolic

Duration: 35 min

Session: Fall 2022

Total Points = 8 (There is 1 point bonus)

Note: Closed book exam. Calculators are not allowed.

Name: _____ Student ID: _____

QUESTION 1 (1 point each, total 5 points)

Short questions

a) What is a systolic array, and where is it used?

PARALLEL HARDWARE ARCHITECTURE FOR STREAMING DATA FOR REGULAR ALGORITHMS THAT PERFORM THE SAME OPERATION OF DATA. MAC AND MATRIX MUL

b) Explain ways to prevent deadlocks in interconnection networks.

THROUGH ROUTING STRATEGIES SUCH AS X-Y ROUTING THROUGH THE EFFICIENT USE OF VIRTUAL BUFFERS

c) What is the purpose of programmable DSP processors? What mathematical operation do they accelerate?

MULTIPLY AND ACCUM.

d) What is the purpose of the virtual channel in case the next link is blocked in the interconnection network? How does the virtual channel help in this case?

VIRTUAL BUFFERS HELP BECAUSE THEY ALLOW DATA THAT GO TO A DIFFERENT LINK TO BE STORED.

e) Describe ways to reduce power consumption in chip multiprocessors.

DVFS, CHOOSING WIRTER. CORES, TURNING OFF SOME PARTS LIKE CACHE SETS, STOP SPECULATI

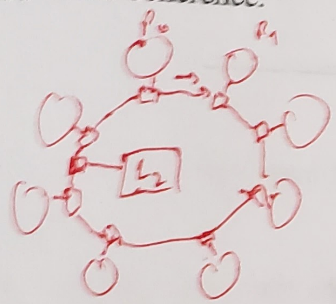
QUESTION 2 (1 point each, total 2 points)

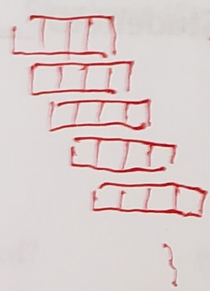
An on-chip interconnection network is based on a unidirectional ring. There are 8 cores on the chip. All cores have a private L1 cache, but they all share a large L2 cache. Assume that there is no contention on any of the wires.

a) Draw this system and the network and explain how the coherence packet is sent through the network (what happens in each node; how does the node know whether to forward the packet...). The switching is a virtual cut-through. What should be the size of the buffers used in switches if the size of the largest packet that the network can support is 64 bytes?

b) Assume that the cache coherence is based on a snooping protocol. In this case, one node needs to send a coherence packet to all other nodes and to continue its operation after receiving the packet back. Assume that the coherence packet is 4 bytes (1 byte header and 3 bytes payload) and the links support one-byte transfers. The switching is virtual cut-through switching. Assume 0 cycles for all the overheads, including the sender and receiver overheads and routing delay in each router. Compute the latency in cycles required to support the coherence.

a)





TIME OF FLICH

8 LINKS, 9 NODES

TIME

TRANSM TIME 3

TOTAL 12

WILL ACCEPT 11 AS A SOL

ASSUMPTION 1

T = OV SENDER OV + L × (R+1) + M + RECEIVE (8, 4, RED)

ASSUMPTION 2

EACH NODE RECEIVES AND PROCESSES THE PACKET, = 12

ASSUME PROCESSING TIME = 0 : ALMOST LIKE STORE AND FORWARD

T = N (L+1) + L × R = 4 + (8+1) = 36

WILL ACCEPT 32 AS A SOL.

QUESTION #3 (1 point each, total 2 points)

Code for implementation of the function F&A (X, Rx, Ry) using LL and SC primitives is shown below.

```
F&A(X,Rx,Ry)
    LL Rx,X            Rx ← X
    ADD R1,Rx,Ry       R1 = Rx + Ry
    SC R1,X            R1 → X      0 IF UNSUCCESSFUL
    BEQZ R1,F&A        IF NOT, BRANCH TO F&A
Return
```

a) What does this code do? Add comments next to each instruction and describe what it does (for example, how is R1 from SC used in BEQZ?).

b) How does it ensure that there are no race conditions during the addition operation?