University of Ottawa

Faculty of Engineering

Department of Computer Engineering

Computer Architecture I

CEG2136

Group 25

LAB 1: Introduction to Quartus II Design Software

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BACKGROUND

The objective of this laboratory is to get familiarized with the Altera Quartus II Design Software and the Altera FPGA based DE2 - 115 platform. The tools will be explored using a simple circuit with AND, NAND and NOR gates seen below. Predictions of the circuit behaviour will be done using logic functions and truth tables. The circuit will be designed using the Graphic Editor and the results obtained following compilation, simulation and debugging will be compared with the predicted outcomes.

It is important to be able to accurately simulate circuits as it is a useful way to draft projects and be able to edit and design plans in a low risk environment with minimal costs.

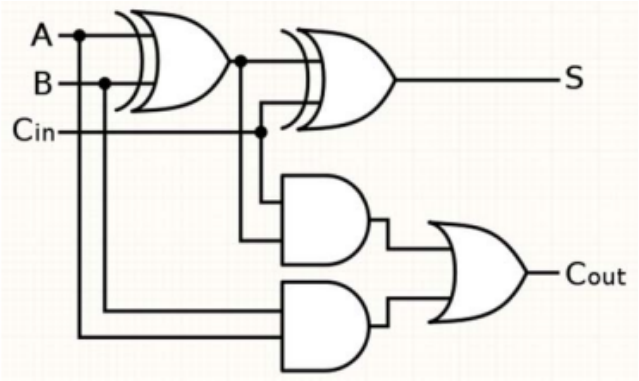


Figure 1. Logic diagram of a simple circuit with full adder S = A+B, Cin/out is a carry bit

DESIGN

Preparation

2. Equations of implemented logic functions

$S = (A \oplus B) \oplus Cin$
$Cout = (A \oplus B) \bullet Cin + A \bullet B$

3. Truth table derivation

Table 1. Truth table for circuit in Figure 1

A	B	Cin	A⊕B	A•B	S	Cout
0	0	0	0	0	0	0

0	0	1	0	0	1	0
0	1	0	1	0	1	0
0	1	1	1	0	0	1
1	0	0	1	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	1
1	1	1	0	1	1	1

4. Truth tables for NAND and NOR functions

a. NAND

Table 2. Truth table for a NAND gate

A	B	x
0	0	1
0	1	1
1	0	1
1	1	0

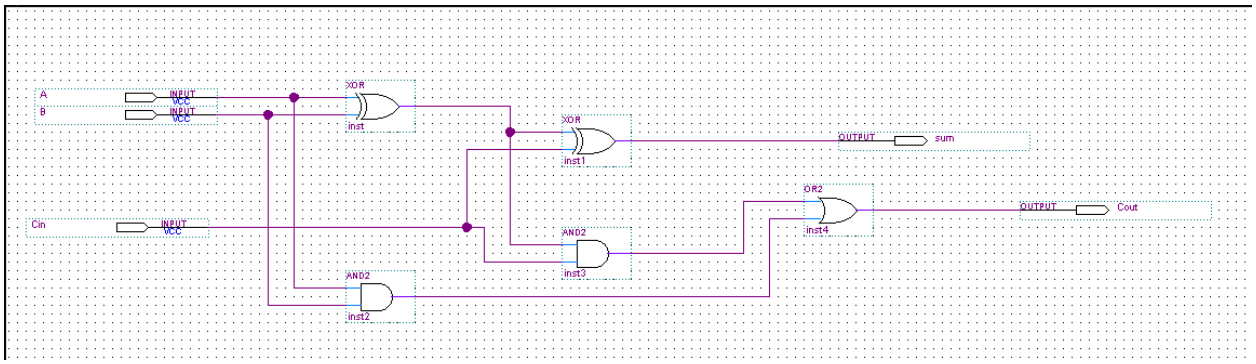
b. NOR

Table 3. Truth table for a NOR gate

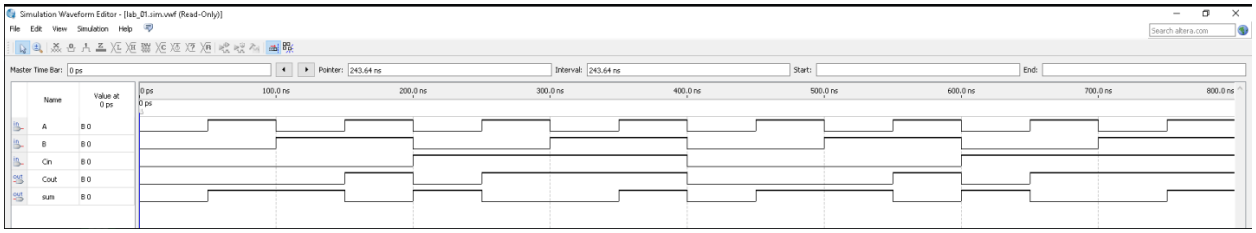
A	B	x
0	0	1
0	1	0
1	0	0
1	1	0

SIMULATION AND VERIFICATION

Block diagram



Waveform simulation



DISCUSSION

The experimental data provided the same results as the ones predicted in the design portion of the investigation indicating a successful use of the Altera Quartus II Design Software. The waveform diagram showed that both outputs are zero when all the inputs are zero and similarly both outputs are one when all inputs are one. This can also be seen in the first and last rows of Table 1 respectively. Likewise all the other predicted outcomes can be matched to their corresponding section in the waveform diagram e.g. when input A is one, B is zero and Cin is one, the predicted output was that the Sum would be zero and Cout would be one which matches the results in the simulation results.

CONCLUSION

Through this experiment we were able to explore how logic circuits can be simulated using virtual tools. This is particularly useful when building circuits for real life applications as it can be much more cost, space and time efficient. There were two parts to this lab and since the labs were performed online, the simulation results for the circuits and the predicted truth tables were used to validate the behaviour of the circuit.