THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
EECE 353 – Digital Systems Design
Midterm – June 2011

A

Use of one single-sided hand-written sheet is permitted.
Answer all problems.
Time: 50 minutes.

This examination consists of 6 pages (including this page). Please check that you have a complete copy. You may use both sides of each sheet if needed.

#	MAX	GRADE
1	5	
2	4	
3	3	
4	5	
5	3	
TOTAL	20	

SOLUTION

Surname First name

Student Number

Signature

IMPORTANT NOTE: The announcement "stop writing" will be made at the end of the examination. Anyone writing after this announcement will receive a score of 0. No exceptions, no excuses.

All writings must be on this booklet. The blank sides on the reverse of each page may also be used.

Each candidate should be prepared to produce, upon request, his/her Library/AMS card.

Read and observe the following rules:

No candidate shall be permitted to enter the examination room after the expiration of one-half hour, or to leave during the first half-hour of the examination.

Candidates are not permitted to ask questions of the invigilators, except in cases of supposed errors or ambiguities in examination-questions.

***Caution** - Candidates guilty of any of the following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:*

Making use of any books, papers or memoranda, calculators, audio or visual cassette players or other memory aid devices, other than as authorized by the examiners.

Speaking or communicating with other candidates.

Purposely exposing written papers to the view of other candidates.

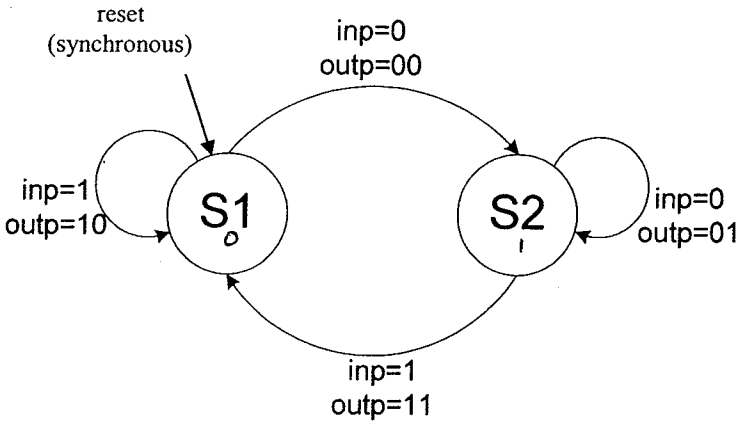
The plea of accident or forgetfulness shall not be received.

1. TRUE/FALSE:

Label each statement with "T" or "F". Be very clear. Answers that look like a combination of "T" and "F" will be marked wrong. [5 marks]

Statement	T/F
Testbenches should only contain synthesizable VHDL.	F
In VHDL, the "case" statement can be used outside a process block.	F
In the datapath circuit of lab3, the register file (8 registers) along with its read and write ports can be specified in a single process block.	F
Standard cell ASICs generally have lower power consumption than FPGAs.	T
Mealy and Moore state machines are examples of sequential circuits.	T

2. Describe the following Mealy state machine using **synthesizable VHDL**. The reset signal is synchronous and active high. The state transitions take place at rising clock edges. [4 marks]

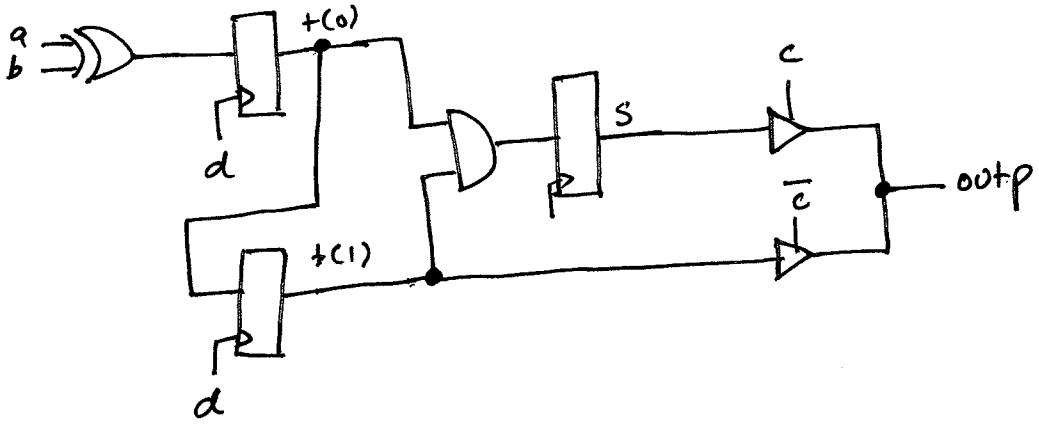


Write your VHDL code on the next page. Use the back side of the page if you need more space.

```
library IEEE;
use IEEE.std_logic_1164.all;

entity mealy_fsm is
   port( clk, reset : in std_logic;
         inp : in std_logic;
         outp : out std_logic_vector (1 downto 0));
end mealy_fsm;

architecture behav of mealy_fsm is

     signal state: std_logic;          -- S1=0 ; S2=1.

begin
        process (clk)
        begin
            if (clk='1') then
                if (reset='1') then
                    state <= '0';
                else
                    case state is
                        when '0' => if (inp='0') then
                                        state<='1';
                                    else state <='0';
                                    end if;
                        when others => if (inp='1') then
                                           state <='0';
                                       else state<='1';
                                       end if;
                    end case;
                end if;
            end if;
        end process;

       process (state, inp)
       begin
            case (state & inp) is
                when "00" => outp <= "00";
                when "01" => outp<= "10";
                when "10" => outp <= "01";
                when others => otstp<="11";
            end case;
        end process;
end behav;
```

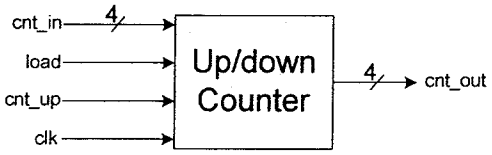
3. Draw a schematic of a circuit that has the same behaviour as the following VHDL code. You can use flip-flops, basic gates, multiplexers, and/or tri-state buffers in your diagram. [3 marks]

```
library IEEE;
use IEEE.std_logic_1164.all;

entity circuit is
    port (a, b, c, d : in std_logic;
          outp : out std_logic);
end circuit;

architecture defn1 of circuit is
    signal s : std_logic;
    signal t : std_logic_vector(1 downto 0);
begin
    process(d)
    begin
      if (d = '1') then
            t <= t(0) & (a xor b);
            s <= t(0) and t(1);
      end if;
    end process;
    process(s, c)
    begin
      if(c = '1') then
            outp <= s;
      else
            outp <= 'z';
      end if;
    end process;
    process(t, c)
    begin
      if(c = '0') then
            outp <= t(1);
      else
            outp <= 'z';
      end if;
    end process;

end defn1;
```



4. Consider the following 4 bit counter. The counter is capable of counting forwards and backwards, and it also has parallel load capability. The counter has 3 inputs (`cnt_load`, `cnt_up`, `cnt_in`) in addition to the clock signal (`clk`). On each rising edge of `clk`, the counter output (`cnt_out`) gets a value according to the following table:

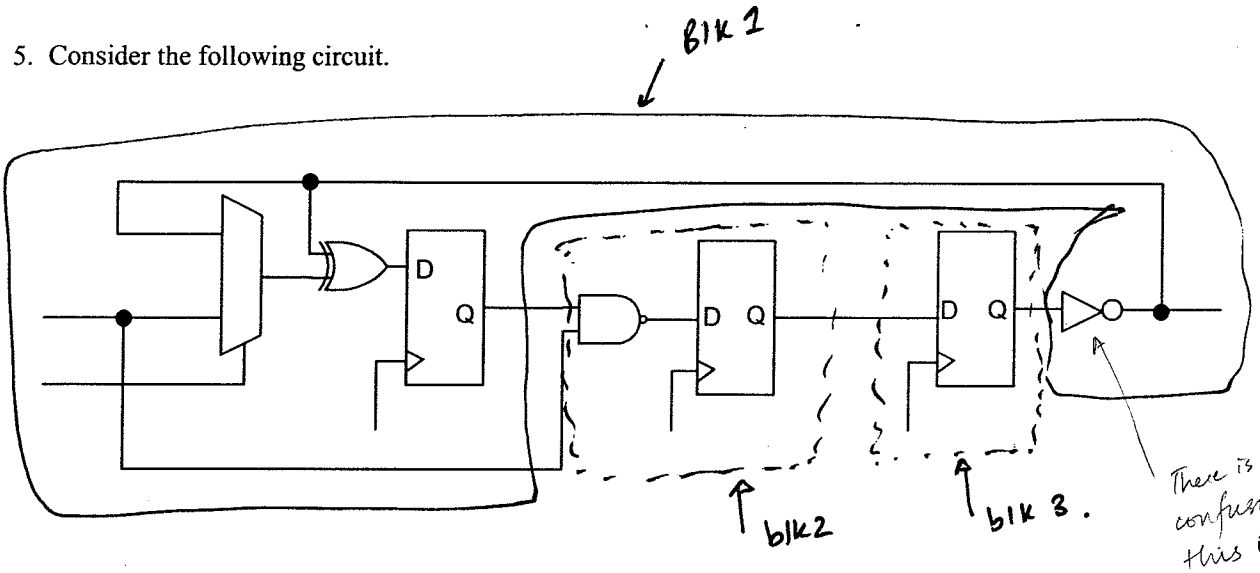
cnt_load	cnt_up	cnt_out
1	d (don't care)	cnt_in
0	1	Previous value of cnt_out + 1
0	0	Previous value of cnt_out - 1



Describe this circuit using synthesizable VHDL. Marks will be deducted for solutions which are excessively complex or long. [5 marks]

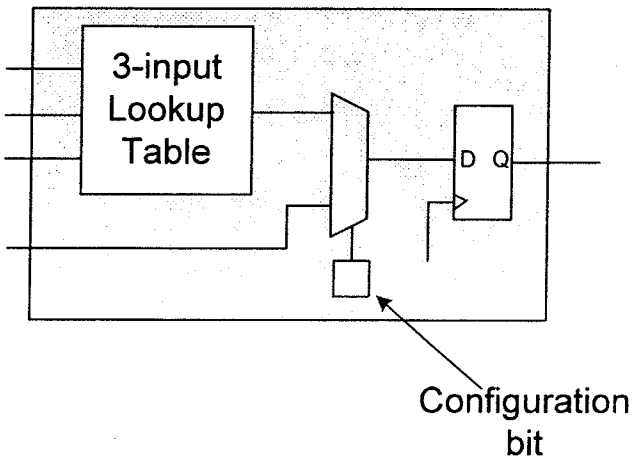
```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity up_down_counter is
      port ( clk, load, cnt_up : in std_logic;
             cnt_in : in std_logic_vector (3 downto 0);
             cnt_out : out std_logic_vector (3 downto 0) );
end up_down_counter;

architecture behav of up_down_counter is
    signal cnt : std_logic_vector ( 3 downto 0);
begin
    process (clk)
    begin if (clk='1') then
            if (load='1') then
                cnt <= cnt_in;
            elsif (cnt_up='1') then
                cnt <= cnt + 1;
            else
                cnt <= cnt - 1;
            endif;
        endif;
    end process;

    cnt_out <= cnt;    -- outside the process!

end behav;
```

5. Consider the following circuit.



There is some confusion about this inverter. It is OK if you group it with blk3 flip flop!

This circuit is to be implemented on an FPGA that has the following logic block architecture.



How many of these logic blocks are required to implement the above circuit? Indicate the portion of the circuit implemented by each logic block (possibly by drawing circles on the above diagram) [3 marks]

3 logic blocks are required.