EELE4054:Digital VLSI Circuit Design
Final Examination - F2020
Department of Electrical Engineering
Lakehead University

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- This is an open book test. You should **not** use any resources other than textbooks, lecture notes, lab manuals, assignments and calculator during the exam.
- Check that there are **6** questions in this examination.
- All answers must be written in **print**. Possibly lose marks due to unreadable answer.
- Provide your name, student number and signature on the first page of your test submission.
- Number and initial all pages of your test submission.
- Ensure your answer pages are submitted in the order questions are given on the test paper. Possibly lose marks if the answers are not in order. Also upside-down pages deserve marks reduction.
- 2 hours and 50 minutes exam time.
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  - unless otherwise allowed by the course instructor, and, in accordance with Section III: Violations of this Academic Integrity Code, I understand that providing any false or misleading information, or by accessing any outside assistance, constitutes a breach of academic integrity as outlined in Lakehead University's Academic Integrity and Policies.

[10] Question 1: Answer the True [T] or False [F] questions.

1) T F Assume an unit inverter drives a load capacitor, C_L. We know that the parasitic capacitance of the NMOS and PMOS transistors are proportional to the size of the transistor while the equivalent resistance of the transistors is inversely proportional to the size of the transistor. As a consequence, increasing the the width of the NMOS and PMOS transistors will not reduce the inverter delay as RC constant won't change.
2) T F In a low-skewed inverter, the logic effort of rising edge transition is larger than that of falling edge transition because the strong discharge path is presented.
3) T F Given CLK is a system clock, and RESET is an internal reset signals. An always block starts with **always@(negedge CLK or RESET)**. Since CLK and RESET are listed in the sensitive signal lists in the always block, this RESET signal is viewed as an synchronize reset.
4) T F A 16-bits decoder is designed in a 130 nm CMOS process, the estimated delay is 560 ps with an measured FO4 inverter delay of 46 ps. If an FO4 inverter delay is 20 ps in a 45 nm CMOS process, the estimated delay of the same design is about 243 ps.
5) T F Fig. 1 shows a CLK and an ENA signal. Within the two dotted line, according to the transition activities of the ENA signal, we can determine the activity factor of ENA is 3/8.

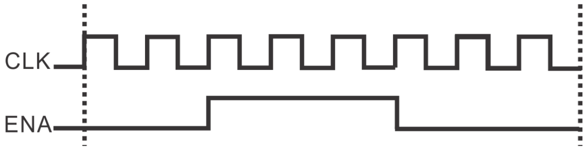

Fig. 1

[10] Question 2: Fig. 2 shows a timing diagram of a counter. Please write a complete and synthesible Verilog program to implement this counter.

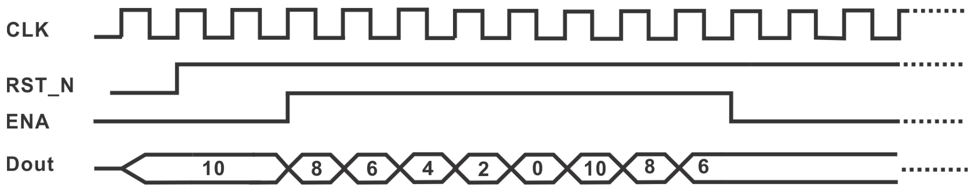

Fig. 2: counter timing diagram.

[16] Question 3 Given input signals, e.g. rst_n, clk, and Din, The state transition diagram and outputs are illustrated in Fig. 3. Please answer the following questions:

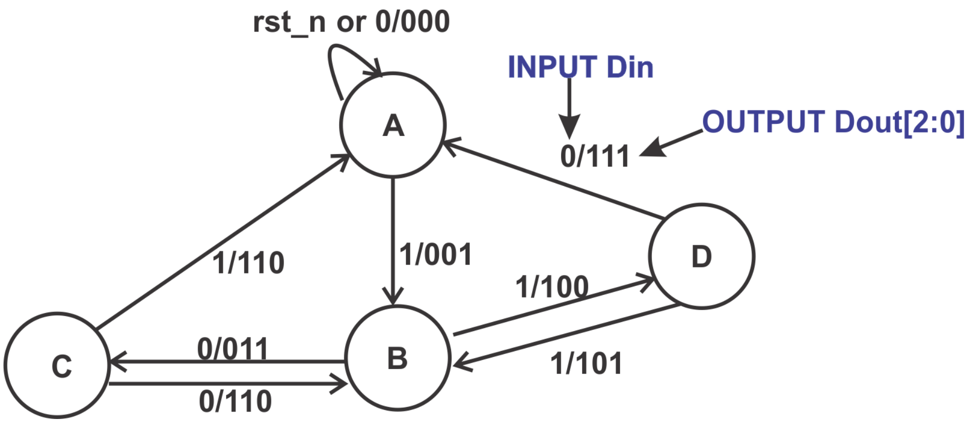

Fig. 3: State diagram.

1) What type of the FSM is and why? [2 marks]
2) Write a complete and synthesible Verilog program to implement this synchronous logic function. Note: you should use two/three always coding style. If only one always is used, you may lose marks. [14 marks]

[15] Question 4: Fig. 4 illustrates a 2-bit decoder for a memory circuit. The output word line is to control each word line in the memory design. For instance, if $A_1A_0 = 00$, word 0 is selected. If $A_1A_0 = 01$, word 1 is selected. Assume truth and complementary values are available as shown in the figure. The delay from the input to the output is about 6 FO4 inverters delay. Each of the output word bit should be capable of driving load capacitance of 5000 C. Please answer the following questions:

1) Based on the given delay, determine the size of transistors in each of logic gates. Using equivalent C to represent the size of total transistors. Note: no need to break the size into PMOS and NMOS. [10]
2) Is there alternative design to be faster than Fig. 4? And why?[2]
3) Assume V_{DD} is 1.2 V, operation frequency is 1 GHz, and capacitance unit, 1 C, is equal to 20 fF. Given the input A_0 and A_1 are random data. What is the switching power at word 0? [3]

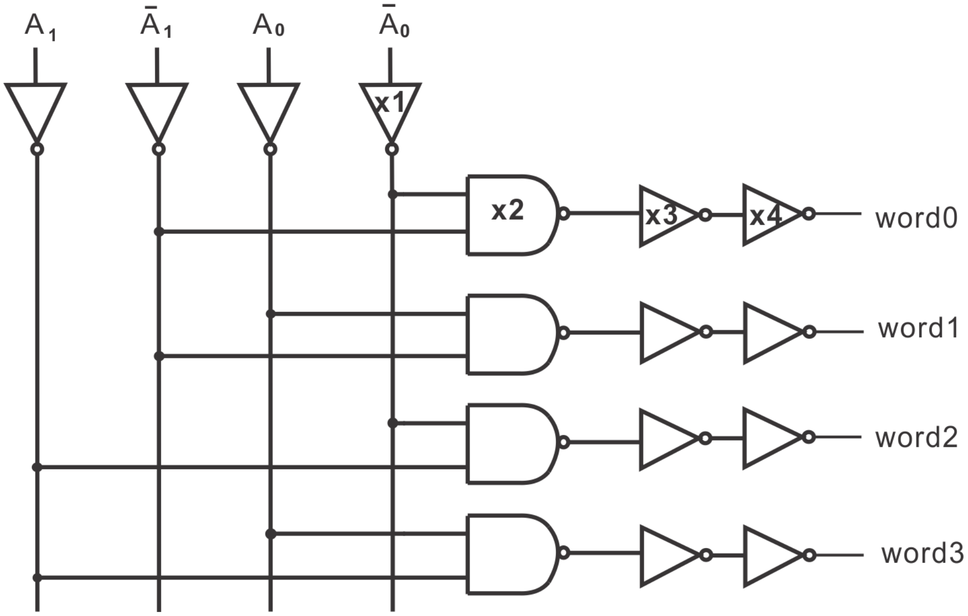

Fig. 4: Decoder.

[18] Question 5: Given a Boolean function as $F = A \cdot (B + C)$. Please answer the following questions:

1) Construct the transistor-level logic gates using one complex compound gate and one inverter. Label the width of transistors to achieve effective rising and falling resistances equal to an unit inverter ($W_p/W_n = 2/1$). [4]
2) Sketch a stick diagram for the compound gate only. Based on λ rules, estimate the width and the height of your design. Note: Each layer should be clearly labeled, e.g. metal 1, poly, n^+/p^+, contacts, etc. [4]
3) Based on the stick diagram, label the parasitic capacitance that affect the delay in the transistor-level logic gates. Note: If the diffusion has one contact, the equivalent parasitic capacitance has the same number as the width of that transistor but with unit of C. For example, for the unit inverter, 2C denotes equivalent parasitic capacitance from one diffusion of PMOS. If a diffusion node is shared by two transistors with one contact, only count its capacitance once from one of two diffusion areas. If the shared diffusion requires no contact, count its capacitance not only once from one of two diffusion areas but the value is also reduced by half. [4]
4) Determine the worst rising and falling delay of the complex compound gate by using Elmore delay model. Assume the load of this compound gate is an unit inverter, having gate capacitance of 3C. [6]

[14] Question 6: A synchronized design is shown in Fig. 5. Table I/II/III list the timing information for the inputs, logic gates and DFFs. The clock's period is 10 ns.

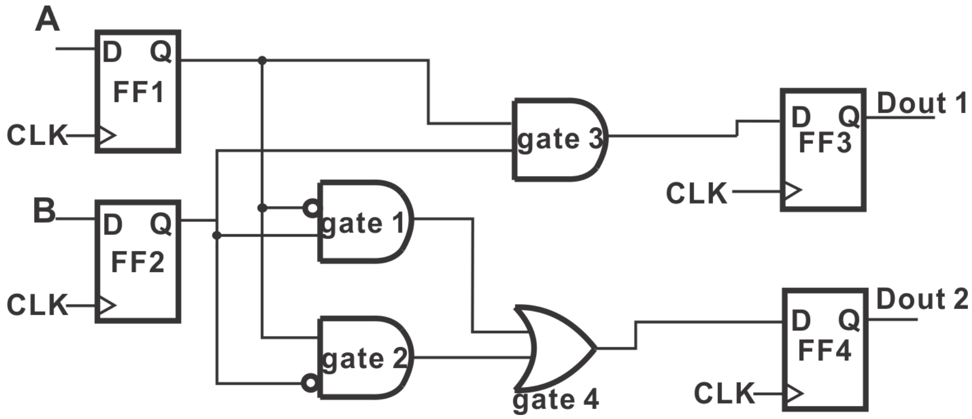

Fig. 5: A synchronized circuit.

TABLE I: Input data(ns)

	A	B
Arrivial	2	1

TABLE II: DFF timing(ns)

	Setup Time	Hold Time	CLK to Q delay(max.)	CLK to Q delay(min.)
$FF_{1,2}$	4	2	1	0.5
$FF_{3,4}$	6	4	1	0.5

TABLE III: Logic gates timing(ns)

	gate 1	gate 2	gate 3	gate 4
Propagation	7	5	3	8
Contamination	1	1	1	3

Please answer the following questions:

1) Check slacks for each of timing paths and identify the timing violations. [10]
2) How to fix those timing violations? [2]
3) What if there is 2 ns clock skew added to the clock arriving at $FF_{3,4}$? Are there any new timing violations? Justify your answer. [2]