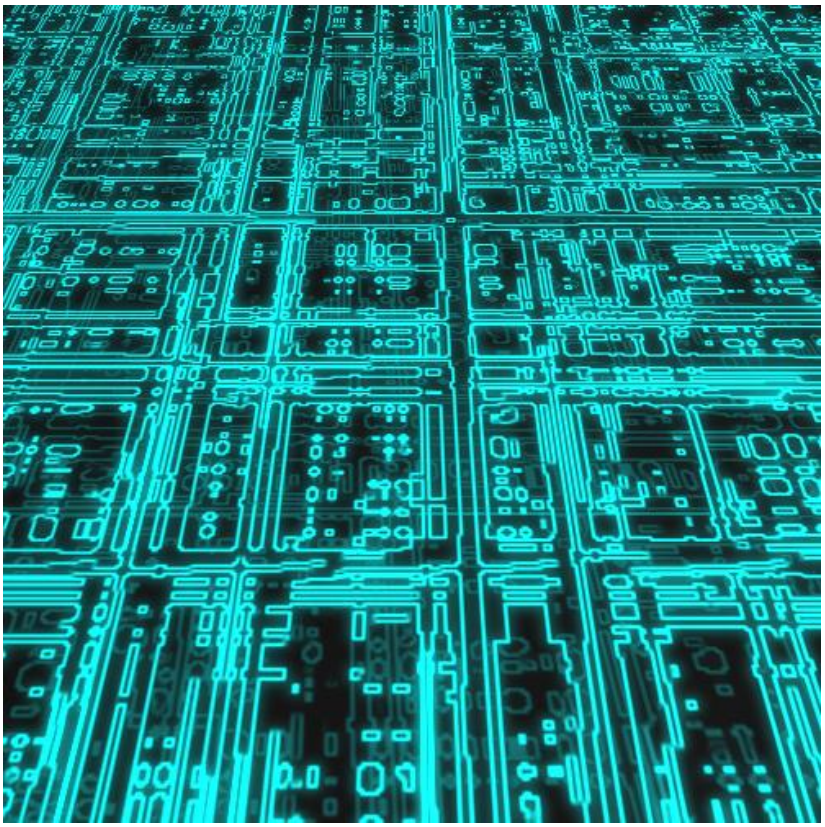

Lab 2: Full Adder

HANDS ON REPORT

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ELEC 2607 B (Robert Gauthier)
Lab Section L70
November 3rd 2020

Part 1: Connecting and testing the power supply

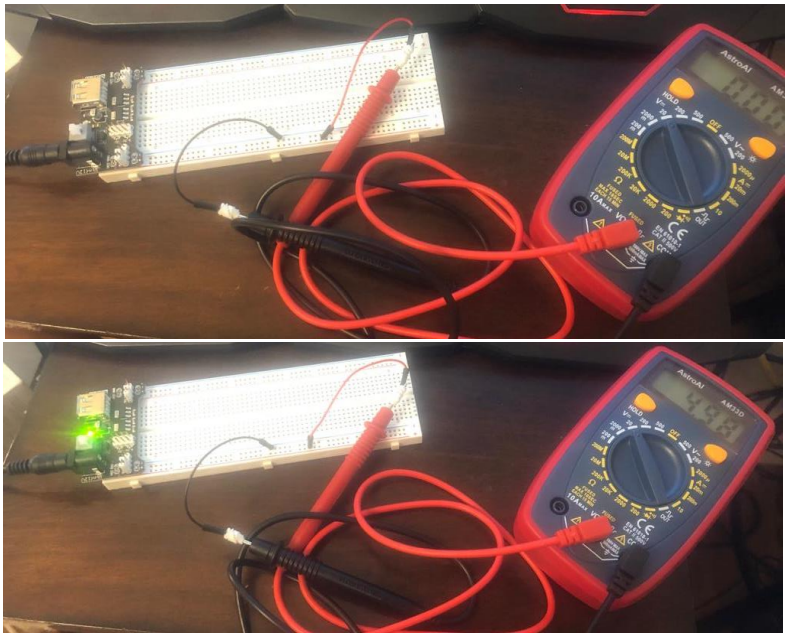

Figure 1 (Power supply voltage is tested with power off (top image) and power on (bottom image))

Power Off Voltage	Power On Voltage
0.00V	4.98V

Table 1 (Power on and off voltages recorded)

The power supply was tested with a digital multimeter by placing its positive (red) lead in the 5-volt terminal of the breadboard power rail and the negative (black) lead in the ground terminal of the power rail. The power board was powered with a 9-volt 1-amp power supply and the leads of the DMM were attached to the board using a double-sided male wire secured through electrical tape. The breadboard, power adaptor, and power board will always be used unless said otherwise.

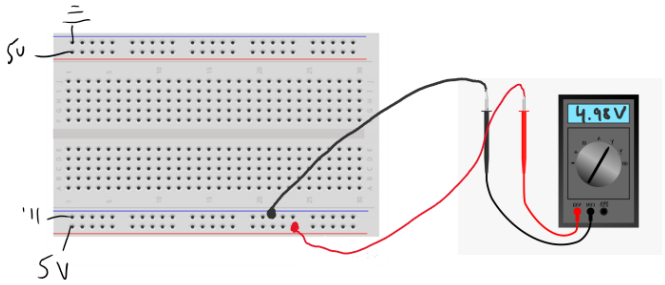

Figure 2 (Circuit schematic shown for testing voltage)

Part 2: Connecting and testing the XOR gate (SN74LS86AN)

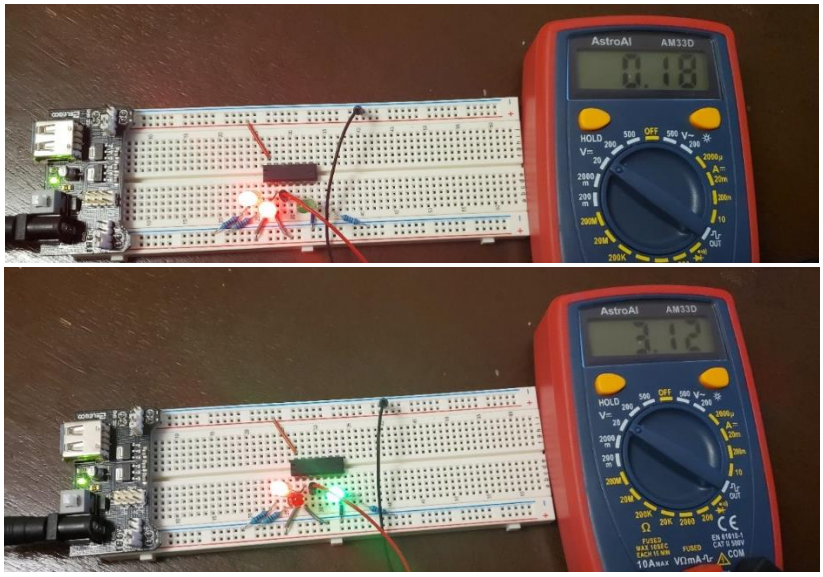

Figure 3 (XOR output voltage is displayed with logic low output(top image) and logic high output(bottom image))

Logic Low Output Voltage (Green LED Off)	Logic High Input Voltage (Green LED On)
0.18V	3.12V

Table 2 (Logics low and logic high output voltages recorded)

Components Used:

- 2-input XOR gate chip (SN74LS00N)
- Digital Multimeter (DMM)
- Green LED
- Two Red LEDs
- Connecting Wires
- Three 1k ohm resistors

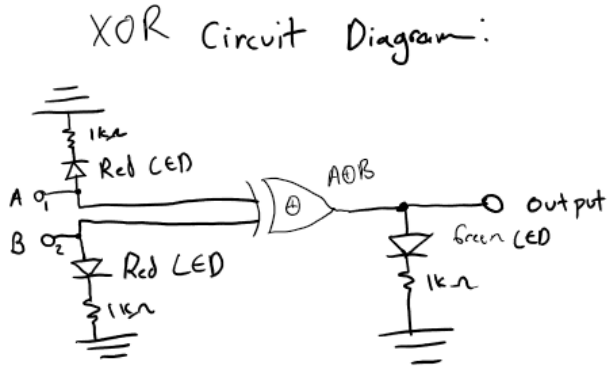

Figure 4 (Circuit diagram for XOR gate setup with two LED inputs and one LED output)

All 4 of the XOR gates on the XOR chip were tested with the two red LEDs displaying the inputs as either logic high (1) or logic low (0) then the Exclusive OR result of the two was displayed by the output green LED as either logic high (1) or logic low (0). The DMM was connected to ground and the output although visual feedback of the voltage inputs and outputs were provided via the LEDs. When the two red LEDs were powered on both inputs were at logic high making it not an Exclusive OR high output as only one can be on therefore output to the green LED resulted in it not being powered on, same case applies to both inputs at logic low. When either red LED was powered on the green LED was powered on as only one input was high. This test showed the XOR gate functioned correctly.

Input (A)	Input (B)	Output (A ⊕ B)
0	0	0
0	1	1
1	0	1
1	1	0

Table 3 (Truth table for XOR gate created with logic change)

Part 3: Connecting and testing the AND gate (SN74LS08N)

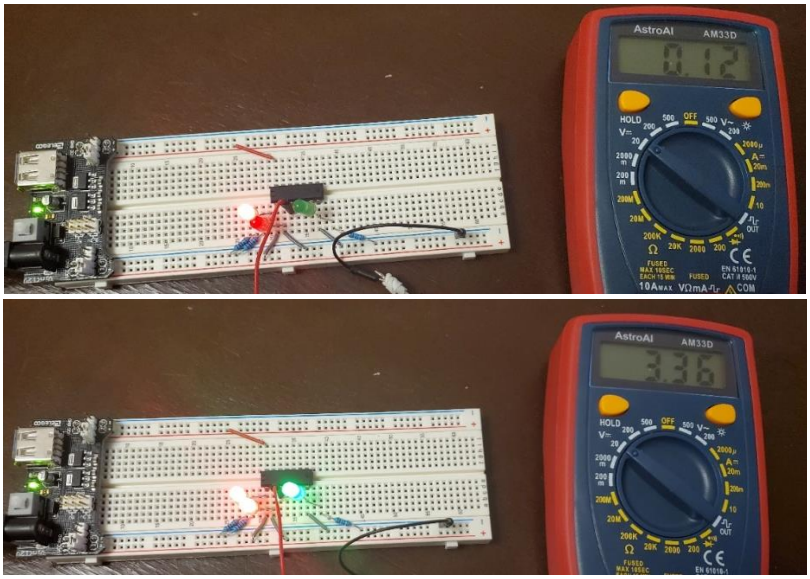

Figure 5 (AND output voltage is displayed with logic low output(top image) and logic high output(bottom image))

Logic Low Output Voltage (Green LED Off)	Logic High Input Voltage (Green LED On)
0.12V	3.36V

Table 4 (Logics low and logic high output voltages recorded)

Components Used:

- 2-input AND gate chip (SN74LS08N)
- Digital Multimeter (DMM)
- Green LED
- Two Red LEDs
- Connecting Wires
- Three 1k ohm resistors

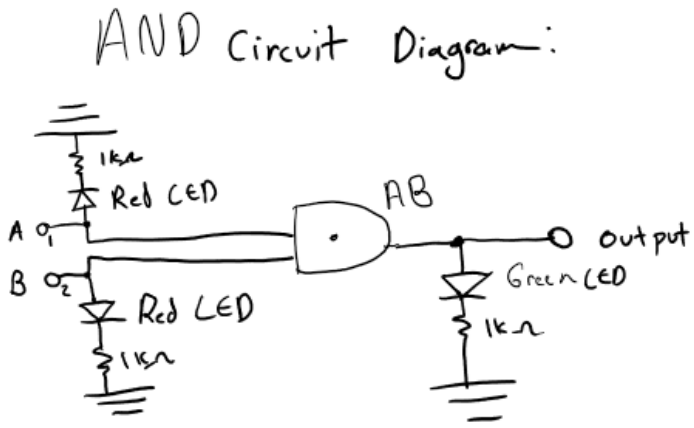

Figure 6 (Circuit diagram for AND gate setup with two LED inputs and one LED output)

All 4 of the AND gates on the AND chip were tested with the two red LEDs displaying the inputs as either logic high (1) or logic low (0) then the AND result of the two was displayed by the output green LED as either logic high (1) or logic low (0). The DMM was connected to ground and the output although visual feedback of the voltage inputs and outputs were provided via the LEDs. When the two red LEDs were powered on both inputs were at logic high making the AND result equal to logic high too therefore output to the green LED resulted in it getting powered on. When either red LED was powered on or both were off the green LED was powered off as only one input was high. This test showed the AND gate functioned correctly.

Input (A)	Input (B)	Output ($A \cdot B$)
0	0	0
0	1	0
1	0	0
1	1	1

Table 5 (Truth table for AND gate created with logic change)

Part 3: Connecting and testing the OR gate (SN74LS32N)

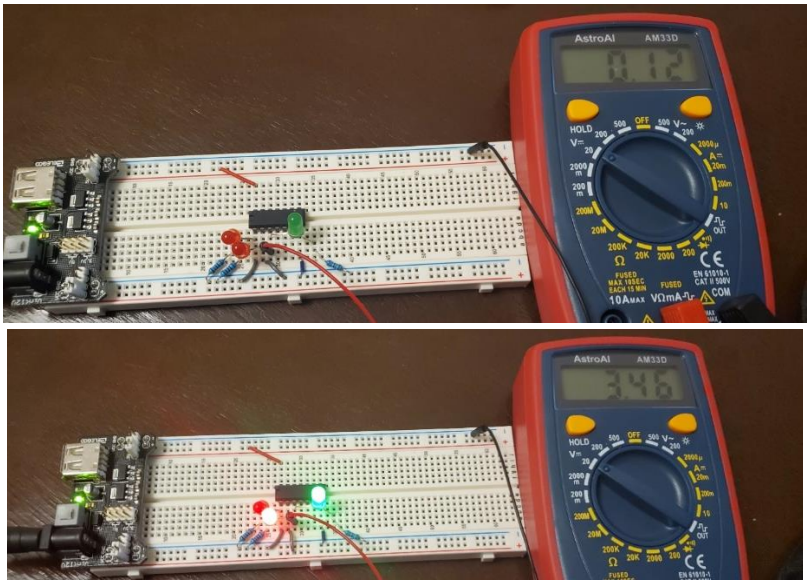

Figure 7 (OR output voltage is displayed with logic low output(top image) and logic high output(bottom image))

Logic Low Output Voltage (Green LED Off)	Logic High Input Voltage (Green LED On)
0.12V	3.46V

Table 6 (Logics low and logic high output voltages recorded)

Components Used:

- 2-input OR gate chip (SN74LS32N)
- Digital Multimeter (DMM)
- Green LED
- Two Red LEDs
- Connecting Wires
- Three 1k ohm resistors

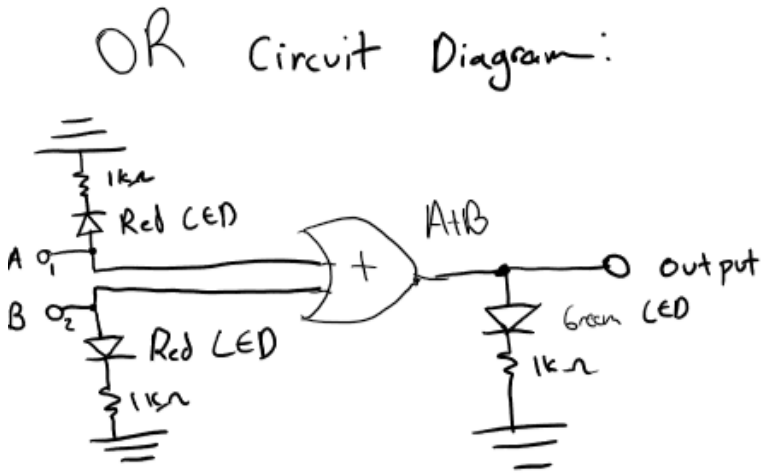

Figure 8 (Circuit diagram for OR gate setup with two LED inputs and one LED output)

All 4 of the OR gates on the OR chip were tested with the two red LEDs displaying the inputs as either logic high (1) or logic low (0) then the OR result of the two was displayed by the output green LED as either logic high (1) or logic low (0). The DMM was connected to ground and the output although visual feedback of the voltage inputs and outputs were provided via the LEDs. When the two red LEDs were powered on both inputs were at logic high making the OR result equal to logic high too therefore output to the green LED resulted in it getting powered on, the same case applied to either LED being on. When both red LED inputs were off the green LED was powered off as no input was high. This test showed the OR gate functioned correctly.

Input (A)	Input (B)	Output (A + B)
0	0	0
0	1	1
1	0	1
1	1	1

Table 7 (Truth table for OR gate created with logic change)

Part 5 & 6: Connecting and testing the SUM & CARRY circuit

SUM and CARRY truth tables

SUM Circuit Truth Table			
X	**Y**	C_i	SUM
0	0	0	0
0	0	1	1
1	0	0	1
1	0	1	0
0	1	0	1
0	1	1	0
1	1	0	0
1	1	1	1

Table 8 (Truth table for SUM circuit)

CARRY Circuit Truth Table			
X	**Y**	C_i	C_{OUT}
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	1
0	1	1	1
1	0	1	1
1	1	1	1

Table 9 (Truth table for CARRY circuit)

SUM and CARRY K-map Boolean Expressions

SUM K-Map		
XY \ C_i	0	1
00	0	1
01	1	0
11	0	1
10	1	0

Table 10 (K-map for SUM circuit)

SUM expression derived from K-Map is

$$\boldsymbol{SUM = X \oplus Y \oplus C_i}$$

CARRY K-Map		
XY \ C_i	0	1
00	0	0
01	0	1
11	1	1
10	0	1

Table 11 (K-map for CARRY circuit)

CARRY expression derived from K-Map is

$$\boldsymbol{CARRY = XY + XC_i + YC_i}$$

SUM Circuit with XOR Gates

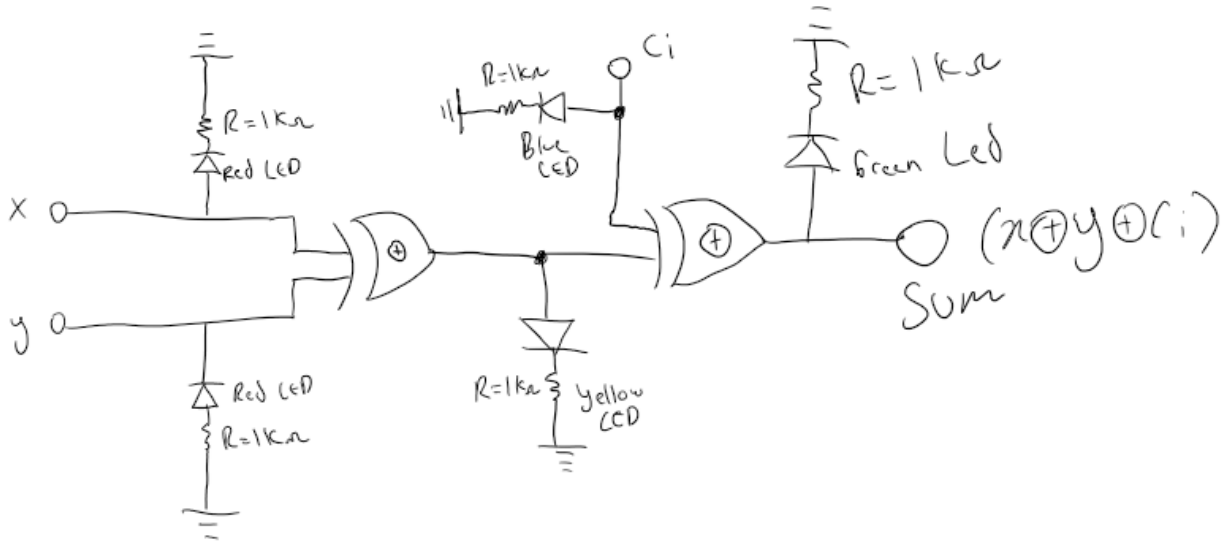

Figure 9 (Circuit diagram for SUM Circuit)

CARRY Circuit with AND-OR Gates

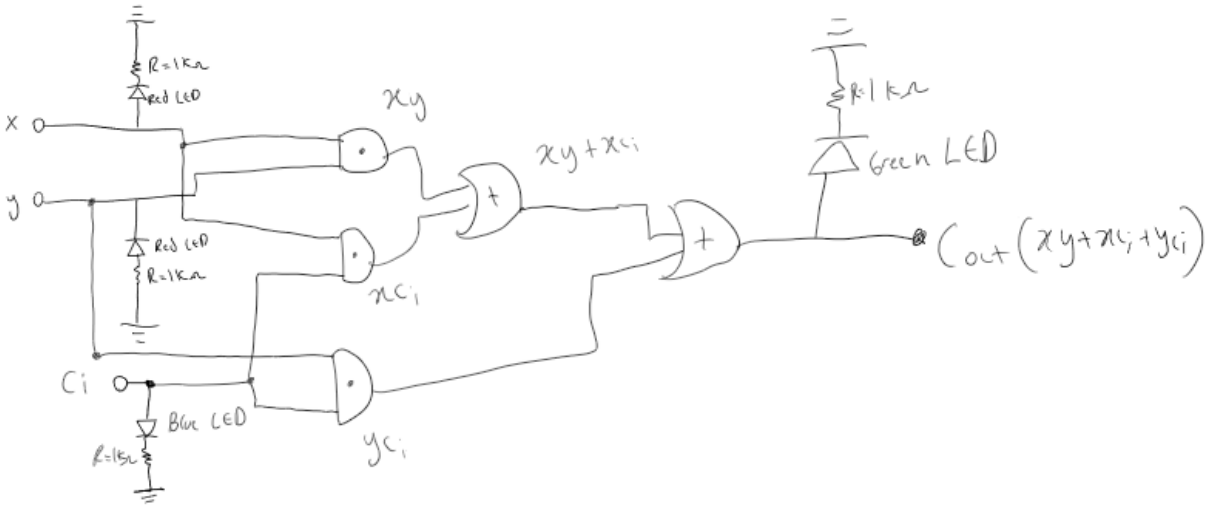

Figure 10 (Circuit diagram for CARRY Circuit)

Connecting and testing the SUM and CARRY circuits

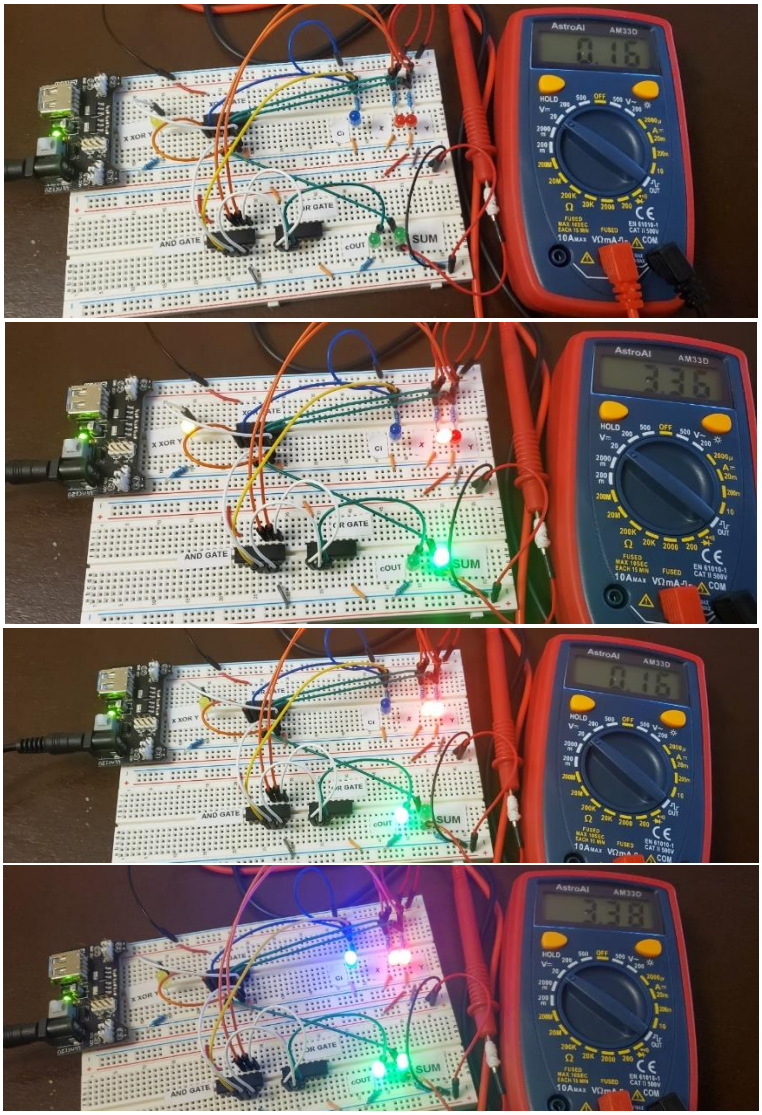

Figure 11 (Output voltage is displayed with all four possible outputs in SUM-CARRY circuit)

Output Low-Low Sum Voltage	Output Low-High Sum Voltage	Output High-Low Sum Voltage	Output High-High Sum Voltage
0.16V	3.36V	0.16V	3.38V

Table 12 (All four output states SUM output voltages recorded)

Components Used:

- One 2-input OR gate chip (SN74LS32N)
- One 2-input AND gate chip (SN74LS08N)
- One 2-input XOR gate chip (SN74LS00N)
- Digital Multimeter (DMM)
- Two Green LEDs
- Two Red LEDs
- One Blue LED
- One Yellow LED
- Connecting Wires
- Six 1k ohm resistors

The sum circuit was constructed using one XOR gate chip as only two XOR gates were utilized. The two red LED's served as input variables X and Y and the blue LED served as another input variable for the carry in. X and Y were put through a XOR gate and their result was displayed using a yellow LED. The result of the XOR of X and Y was then XOR with the carry input as seen in the schematic in Figure 12 below and the result was displayed with a green LED which was labelled as the first output sum. The carry circuit was constructed using OR and AND chips. The result from the XOR of X and Y from the previous circuit was used as and input with the carry input in an AND gate. Then the result was put in an OR gate with the AND result of X and Y and the carry output was produced which was then labelled as cOUT and displayed with a second green LED.

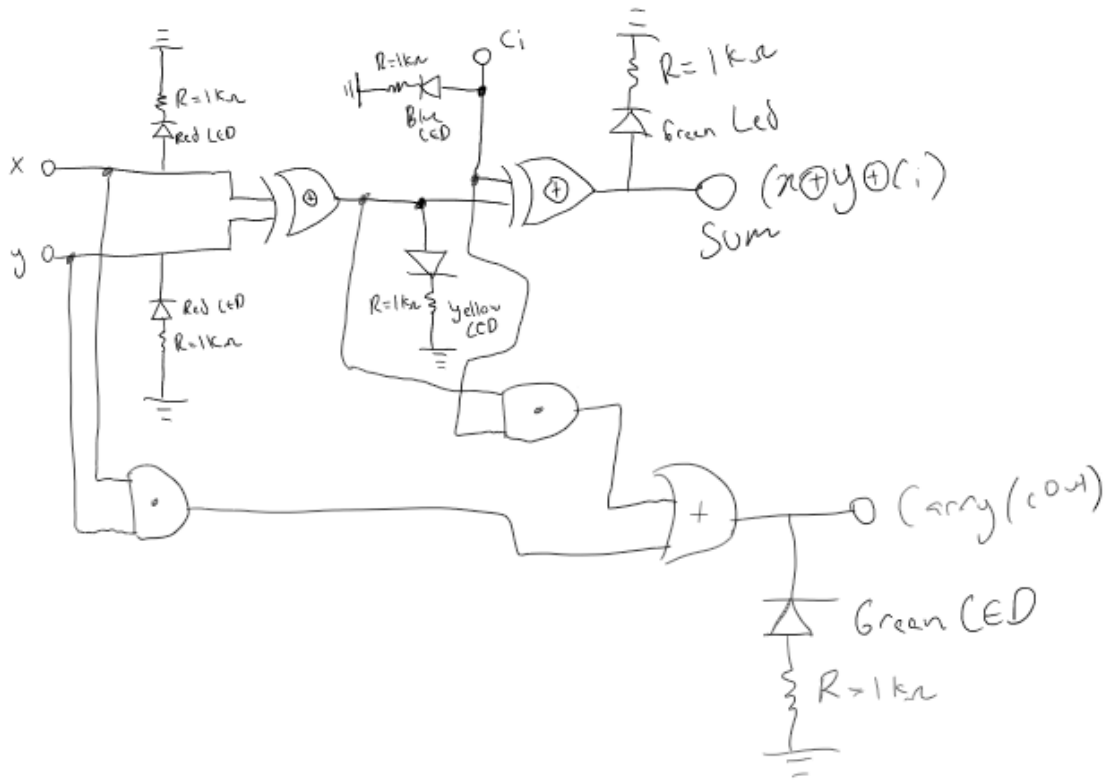

Figure 12 (Combined SUM-CARRY circuit constructed with XOR, AND, and OR gates)