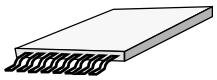
CARLETON UNIVERSITY

Department of Electronics



ELEC 2607 **Switching Circuits** **August 2020**

Laboratory 3 T-Bird

In the Laboratory

The software used will be the Xilinx™ ECS Graphic Entry System, and the logic will be simulated using the ModelSim™ simulator. You will be then programming hardware on a CPLD (complex Programmable Logic Device), so you can see the lights flashing. Unfortunately, a T-Bird is not supplied. **NOTE: In the fall of 2020 no actual circuits are built in the DOE LABORATORY portion of lab 3.** Circuits are built in the hands-on section of the lab and must be demonstrated to the TA through video uploads (Maximum file size 100 MB).

Simulation

The Verilog test fixture file

To simulate your circuit, you need a file to generate the clock and switch signals. This file is usually called a test bench file. The ECS software calls it a ".tf" or test fixture file. This file is given at the end of the lab.

"//" precedes a comment.

"#13" means a delay of 13 time units before the next instruction is simulated. The time units for this simulation are seconds, as given by the `timescale 1 s / 100 ms command. The delays accumulate, thus #7 x = 1;

#5 y = 0; give a total delay of 12 before the simulator finishes making y zero.

The included test fixture file generates signals for only four of the possible button combinations. You must add statements to test the others.

Simulations in your report

Print out a copy of your revised test fixture file (up to the $stop) for your report.

You will need print the simulation waveforms so you can **annotate** them in your report. TAs will be very hard on people who think they can staple a printout into the report with no comment!

There are some very short glitches showing in the simulations. Ask the TA or the Prof about them, alternately read ahead in the notes about hazards. Explaining them is a good thing to put in the report.

Implementation (Optional for Fall 2020-2021)

This program was intended to be implemented on a Complex Programmable Logic Device (CPLD). The particular device will be a Xilinx XCR3064XL-6 PC44, 44-pin logic-array. They run from a 3.3 V power supply and have a pin-to-pin delay of 2ns. Obviously, your taillights will not need to run that fast.

It is basically a large collection of ANDs feeding a smaller collection of ORs, which feed flip-flops. How these arrays work will be described later in the Array Logic course notes.

fCLK and CLK

The circuit board containing the CPLD has a clock generator on it. This generator is set up for the MIDI lab and is so fast that the tail-light flashes become a blur. For this reason, there is a frequency divider circuit built into the *tbirdtop.sch* file, which divides down the 8 Hz fCLK signal to a 1 Hz CLK for flasher timing.