View Statistics - Hybrid Quiz4

Include exempted users in stats

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Question Details

Export to CSV | Export to Excel

Has Start Date 10/12/2019 Now

Has End Date 10/19/2019 Now Apply

(Number of First Attempts: 29) What do the statistics on this page mean?

Question 1 Difficulty: 1

A generic computer architecture consists of these 3 main parts:

I/O system, Processor and display	1	(3.45 %)
➡ I/O system, Processor and Memory	28	(96.55 %)
Processor, keyboard and display	0	(0 %)
Memory, keyboard and display	0	(0 %)

Average Grade: 0.97 / 1 (96.55 %)
Standard Deviation: 18.57 %
Point Biserial: 0.58
Discrimination Index: 12.50 %

Question 2 Difficulty: 1

CU (Control Unit) and ALU (Arithmetic and Logic Unit) reside in:

Memory	0	(0 %)
➡ CPU	27	(93.1 %)
I/O System	0	(0 %)
None of these	2	(6.9 %)

Average Grade: 0.93 / 1 (93.1 %)
Standard Deviation: 25.79 %
Point Biserial: 0.51
Discrimination Index: 25.00 %

Question 3 Difficulty: 1

The Control Unit (CU) controls the operations based on a sequence of instructions stored in the Memory

Average Grade: 1 / 1 (100 %)
Standard Deviation: 0.00 %
Point Biserial: n/a
Discrimination Index: 0.00 %

➡ True	29	(100 %)	
False	0	(0 %)	

Question 4 Difficulty: 1

At the Control Unit (CU), the Instructions execution consists of three phases.

Average Grade: 0.93 / 1 (93.1 %)
Standard Deviation: 25.79 %
Point Biserial: 0.35
Discrimination Index: 25.00 %

Read, Execute, Write	2	(6.9 %)
Fetch, Read, Write	0	(0 %)
➡ Fetch, Decode , Execute	27	(93.1 %)

Question 5 Difficulty: 1

Fetching Instruction means that the Instruction is read from the Memory

Average Grade: 0.86 / 1 (86.21 %)
Standard Deviation: 35.09 %
Point Biserial: 0.75
Discrimination Index: 50.00 %

➡ True	25	(86.21 %)
False	4	(13.79 %)

Question 6 Difficulty: 1

In the CPU which part manipulates, changes, combines and calculates data value

Average Grade: 0.97 / 1 (96.55 %)
Standard Deviation: 18.57 %
Point Biserial: 0.58
Discrimination Index: 12.50 %

CU	0	(0 %)
MEMORY	1	(3.45 %)
➡ ALU	28	(96.55 %)

Question 7 Difficulty: 1

CPU interfaces with the Memory and the I/O via:

Average Grade: 0.97 / 1 (96.55 %)
Standard Deviation: 18.57 %
Point Biserial: 0.13
Discrimination Index: 12.50 %

Address bus,	0	(0 %)
Address bus and Data Bus,	1	(3.45 %)
➡ Address bus, Data Bus and Control Bus	28	(96.55 %)
Control Bus Only	0	(0 %)

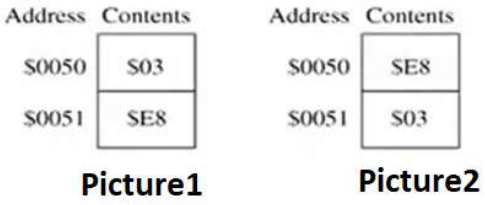
Question 8 Difficulty: 1

For Motorola Processor, when 16 bit data is stored in memory, the most significant byte of the data is stored at the memory location specified by the effective address, and the least significant byte is stored at the effective address plus one. This is referred to as **"big endian"** format.

We want to store $03E8 at address starting $0050 , the data would appear like this:

Two different viewpoints of storing $03E8 in memory

Example of big and little endian formats of a 16-bit number.



Which one of these pictures represents big endian Format.,

➡ Picture1	27	(93.1 %)	Average Grade: 0.93 / 1 (93.1 %)
Picture2	2	(6.9 %)	Standard Deviation: 25.79 %
			Point Biserial: 0.35
			Discrimination Index: 25.00 %

Question 9 Difficulty: 1

Data Bus is is bidirectional

			Average Grade: 1 / 1 (100 %)
➡ True	29	(100 %)	Standard Deviation: 0.00 %
False	0	(0 %)	Point Biserial: n/a
			Discrimination Index: 0.00 %

Question 10 Difficulty: 1

Address Bus is is bidirectional

			Average Grade: 1 / 1 (100 %)
True	0	(0 %)	Standard Deviation: 0.00 %
➡ False	29	(100 %)	Point Biserial: n/a
			Discrimination Index: 0.00 %