Name: Q. J. Zhang Student #: Section:

Question	Max Marks	Score
1	10	
2	20	
3	20	
4	25	
5	20	
Total	95	

CARLETON UNIVERSITY

FINAL
EXAMINATION
August 21, 2012

Duration: 3 hours

Department name and course number: Electronics ELEC-2507

Course Instructor(s): Q-J Zhang Number of students: 64

AUTHORIZED MEMORANDA:

NON-PROGRAMMABLE CALCULATOR

Students MUST count the number of pages in this examination paper before beginning to write, and report any discrepancies immediately to a proctor. **This question paper has 18 pages.**

This examination question paper MAY NOT be taken from the examination room.

This exam consists of 5 questions, which should be answered on this exam paper in the space provided. Attempt all questions. Marks allocated to each question are indicated (total marks = 95).

Note: The solution must be clearly indicated. Multiple solutions or solutions that are not clearly identified, will be marked incorrect. Using approximate relations (unless they are given below or specified in a question) is not accepted. Clearly state all assumptions made. **Clearly mark the units for all final answers. Clearly indicate axis/units for any graphs. SHOW YOUR WORK!**

Diode:

Forward current: $I_D = I_S\,(exp(V_D/V_T) - 1))$

Small signal resistance: $r_d = V_T/I_D$

$V_T = \frac{kT}{q} = 25mV$ at room temperature

Bipolar Transistor:

Active mode operation: $V_{BE} = 0.7V$

Saturation mode operation: $V_{CEsat} = 0.2V$

$i_C = \beta i_B \quad i_C = \alpha i_E \quad i_E = i_B + i_C$

$g_m = \frac{I_C}{V_T} \quad r_\pi = \frac{\beta}{g_m} \quad r_o = \frac{V_A}{I_C}$

$r_e = \frac{\alpha}{g_m} = \frac{r_\pi}{\beta+1} \quad \alpha = \frac{\beta}{\beta+1}$

Operational Amplifier:

$V_o = A(V_+ - V_-)$; $R_i = \infty$; $R_o = 0$

MOSFET:

$\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m, $g_m = 2\,I_D / V_{ov}$;

$$I_{DS} = k' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right];$$

$$I_{DS,sat} = k' \frac{W}{L}\frac{(V_{GS} - V_t)^2}{2}(1 + \lambda V_{DS});$$

$k' = \mu C_{ox}$; $K = k' \frac{W}{L}$

$V_{OV} = V_{GS} - V_t$

$$g_m = k' \frac{W}{L}(V_{GS} - V_t) = \sqrt{2k' \frac{W}{L} I_{DS}}$$

$$r_{DS,triode} = \left[k' \frac{W}{L}(V_{GS} - V_t)\right]^{-1}; \quad r_o = \frac{V_A}{I_D}$$

Q1: Answer the following by filling in the corresponding circles with your selection *a*, *b*, *c* or *d*
(10 marks)

i) What is the gain, V_o/V_{in}, for the circuit in Fig. 1.i, assuming the operational amplifier is ideal?

(a) 3
(b) -3
(c) 4
(d) -4

C

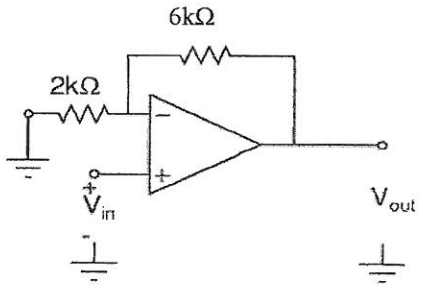


Fig. 1.i

ii) For a center-tapped full wave rectifier using ideal diodes, the peak-to-peak input voltage is ±12V. Which one of the following diodes you will be the optimum picks for your circuit taking into consideration of proper circuit functioning ?.

(a) diodes with a PIV (peak inverse voltage) of 6V.
(b) diodes with a PIV of 12V.
(c) diodes with a PIV of 18V.
(d) diodes with a PIV of 24V.

d

iii) Using a piecewise-linear model for the diode in the circuit in Fig. 1.iii., what is the voltage V_D in that circuit (given the linear-piecewise diode data of $V_{D0} = 0.65V$ and $r_D=20\Omega$)?

(a) 1.4V
(b) 1V
(c) 0.65V
(d) 0.4V

b

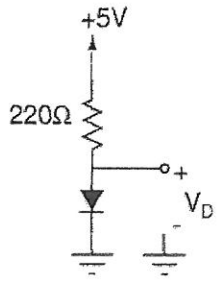


Fig. 1.iii

Q52

iv) In the circuit in Fig. 1.iv, each diode has a forward constant voltage drop of 0.7V. What is the value of V_{out} if V_{in} is **-4V**?

(a) -4V
(b) 0.7V
(c) -2.1V
(d) 2.1V

a

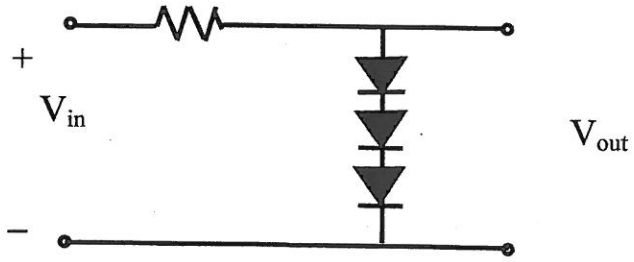


Fig 1.iv

v) Given the characteristic curves for a MOSFET in Fig. 1.v, what are the regions I and II known as?

(a) I – triode, II – saturation
(b) I – cut-off, II – saturation.
(c) I - saturation, II - active.
(d) I – triode, II – active

a

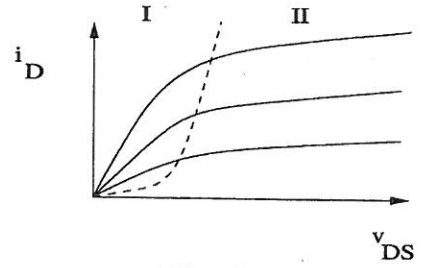
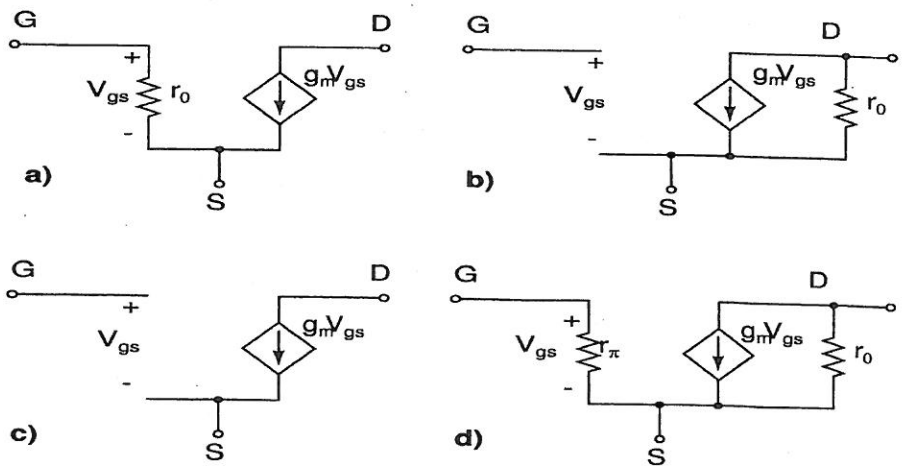


Fig. 1.v

vi) What is the correct small signal model equivalent circuit for a MOSFET with *channel length modulation*?

b



Q1

vii) Which of the following statements is **incorrect** for an ideal operational amplifier?

(a) It has an infinite open loop gain.
(b) It has an infinite common-mode rejection.
(c) It has a zero input impedance.
(d) It has a zero output impedance.

c

viii) Which of the following statements is **incorrect** about a well designed common emitter amplifier?

(a) The transistor should be biased in the active mode.
(b) The input can be coupled through a coupling capacitor.
(c) The input resistance should be very small.
(d) The gain depends upon the resistance in the collector branch of the circuit.

c

ix) What is V_c for the DC circuit shown in Fig.1.ix, given the transistor has a β of 100 and assuming V_{BE} is 0.7V.

(a) 8V
(b) 7.8V
(c) 4.8V
(d) 4V

b

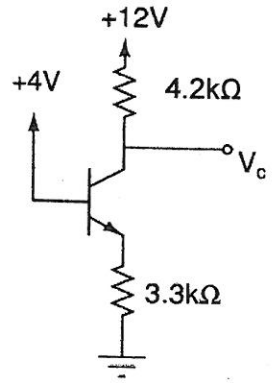


Fig.1.ix

x) The bipolar junction transistor can be placed in the cut-off mode of operation when the

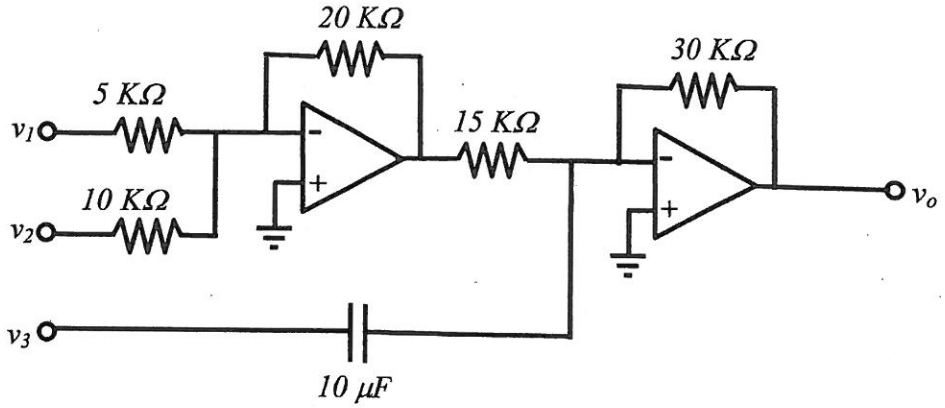
(a) emitter-base junction is forward biased and the collector-base junction is reverse biased,
(b) emitter-base junction is forward biased and the collector-base junction is forward biased,
(c) emitter-base junction is reverse biased and the collector-base junction is forward biased,
(d) emitter-base junction is reverse biased and the collector-base junction is reverse biased.

d

QJz

Q2. Operational Amplifier

a) For the circuit below, write an **Time-Domain** expression of the output voltage $v_o(t)$ in terms of the 3 input voltages $v_1(t)$, $v_2(t)$, and $v_3(t)$. Assume that the op-amp is ideal. **(5 marks)**



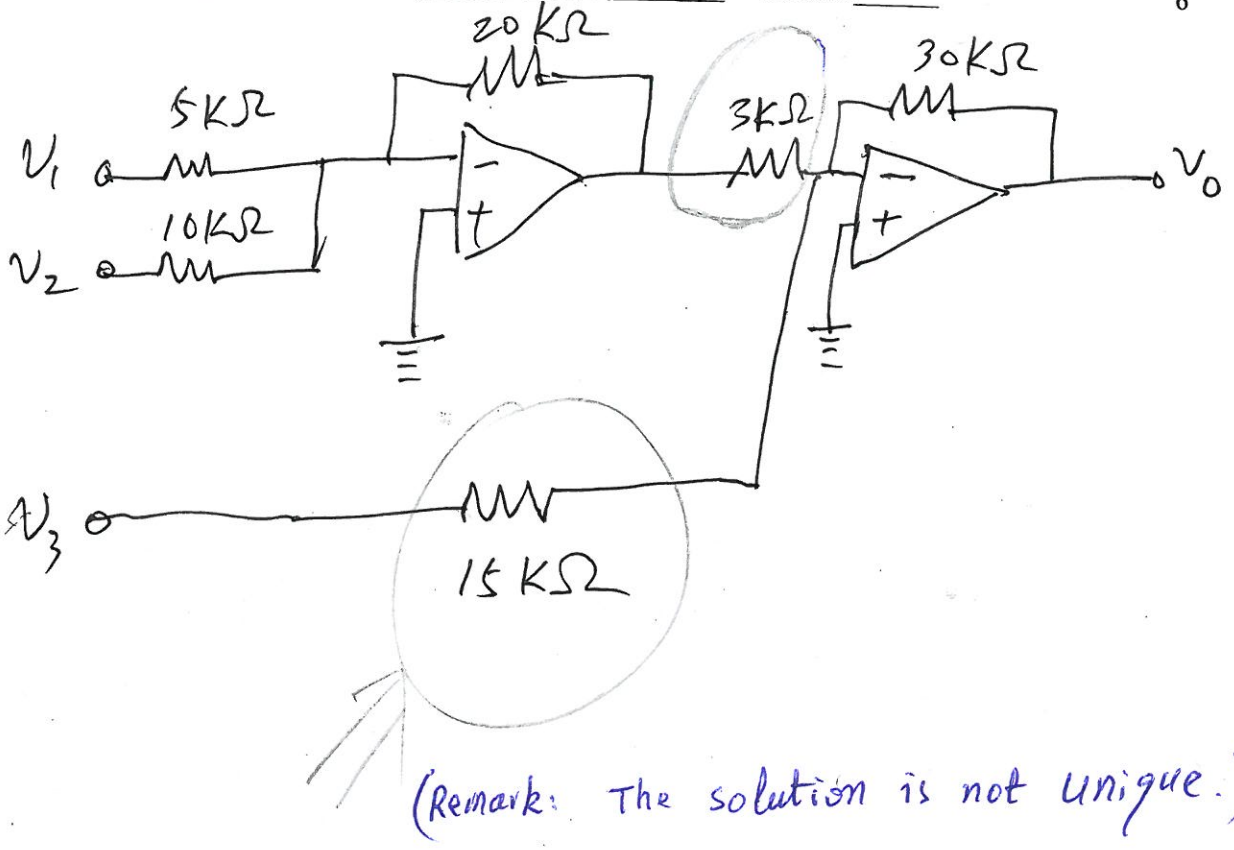
$$V_o = -(10\mu F \times 30K\Omega)\frac{dv_3}{dt} - \frac{30K\Omega}{15K\Omega}\left(-\frac{20}{5}V_1 - \frac{20}{10}V_2\right)$$

answer: $V_o = 8V_1 + 4V_2 - 0.3\frac{dV_3}{dt}$

b) Modify the circuit in a) by changing at most two components such that the response will become

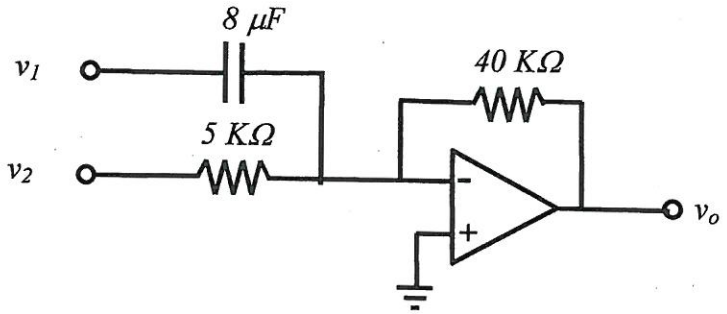
$v_o = 40v_1 + 20v_2 - 2v_3$

Re-draw the circuit clearly labeling the values of all components **(4 marks)**



(Remark: The solution is not unique.)

c) Consider the op-amp circuit below. Assume that all the op-amps are ideal. Write the expression for the response v_o (using **phasor notations**) in terms of v_1 and v_2. **(2 marks)**

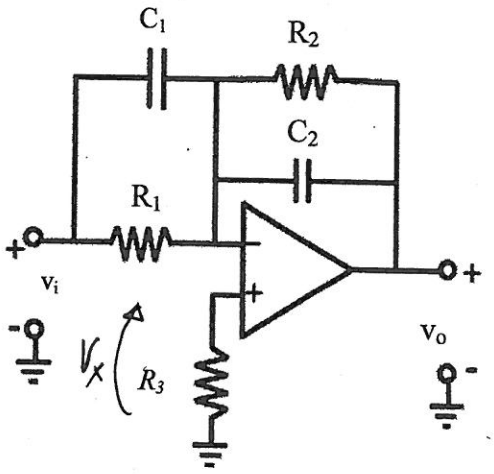


$$V_o = -\,40\,k\Omega \cdot 8\,\mu F\, j\omega\, V_1 - \frac{40}{5} V_2$$

answer: $V_o = -0.32\, j\omega V_1 - 8 V_2$

$j\omega$ ← Greek omega

d) Consider the circuit below, where the op-amp is ideal.



i) Derive the gain $H(j\omega) = v_0(j\omega)/v_i(j\omega)$. Show the steps **(6 marks)**

$$H = \frac{R_2 \,//\, \frac{1}{j\omega C_2}}{R_1 \,//\, \frac{1}{j\omega C_1}} \quad , V_x = 0$$

$$= -\frac{R_2}{j\omega C_2} \cdot \frac{1}{R_2 + \frac{1}{j\omega C_2}} \cdot \frac{\left(R_1 + \frac{1}{j\omega C_1}\right) j\omega C_1}{R_1}$$

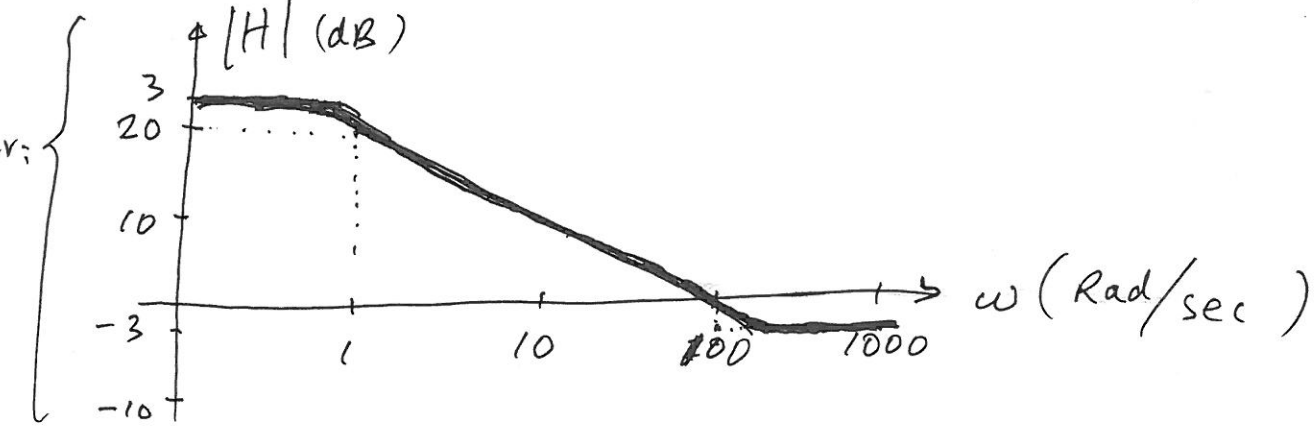
$$\boxed{H = -\frac{R_2}{R_1} \frac{j\omega R_1 C_1 + 1}{j\omega R_2 C_2 + 1}}$$

← $j\omega$ omega

ii) Suppose $R_1 = 500\ \Omega$, $R_2 = 10K\Omega$, $R_3 = 45K\Omega$, and $C_1 = 20\mu F$, and $C_2 = 100\mu F$. Sketch the magnitude of the gain (in DB) with respect to angular frequency **(3 marks)**

$$H = -\frac{10K\Omega}{500\Omega} \frac{j\omega 500\Omega \cdot 20\mu F + 1}{j\omega 10K\Omega \cdot 100\mu F + 1} = -20 \frac{j\omega 0.01 + 1}{j\omega + 1}$$

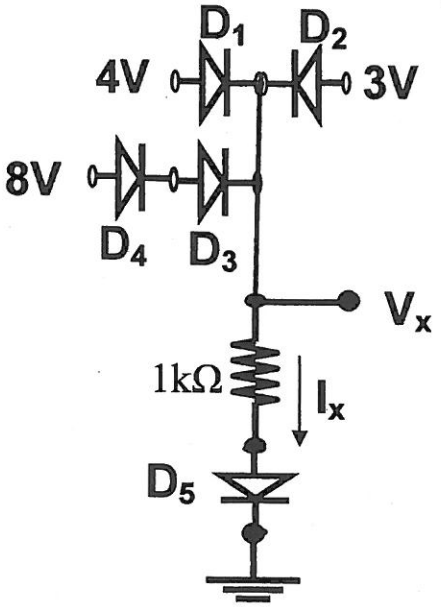
answer:

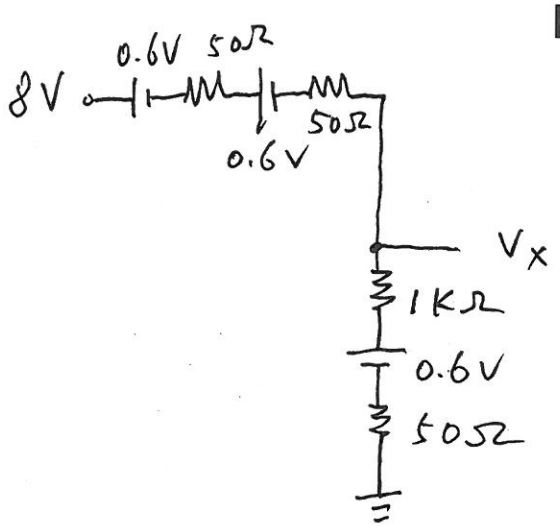


Q3:

Q3: Diodes

a) Consider the circuit below. Suppose the model for each of the diodes is a piece-wise linear model with V_{D0}=0.6V and r_D = 50Ω. For the given inputs, find the output voltage V_x and the current I_x? **(7 Marks)**





$$I_x = \frac{8V - 0.6V - 0.6V - 0.6V}{1K\Omega + 50\Omega + 50\Omega + 50\Omega} = \frac{6.2V}{1.15K} = 5.39mA$$

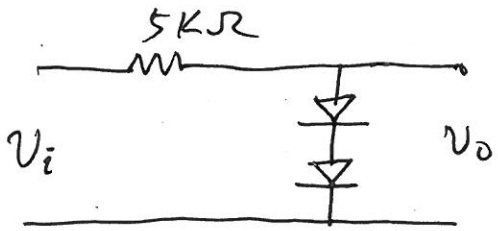
$V_x = 0.6 + 5.39 \times (1K + 50\Omega)$
$= 6.26V$

$V_x = 6.26V$
$I_x = 5.39mA$

b) Design limiter circuits using only diodes and 5kΩ resistors to provide an output signal limited to the specified ranges (given below). Assume a constant-voltage drop model for the diodes with $V_D = 0.7$ V.

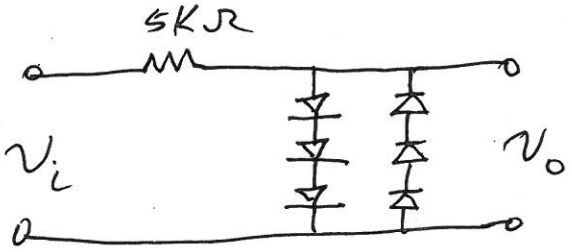
i. Output specification: 1.4V and below.

(2 marks)



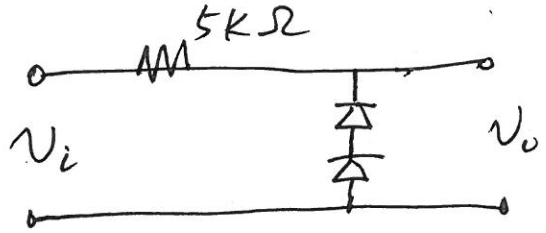
ii. Output specification: ±2.1 V.

(2 marks)

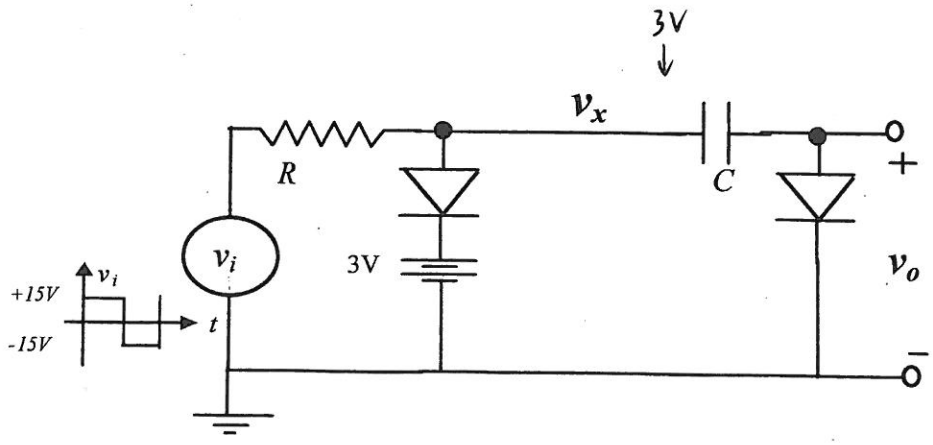


iii. Output specification: -1.4 V and above.

(2marks)



c) For the circuit below, if the input were a pulse train of ±15V, what would be the minimum and maximum voltages at v_x and v_o? Assume ideal diodes. **(3 Marks)**



v_{xmin} = -15

v_{xmax} = 3

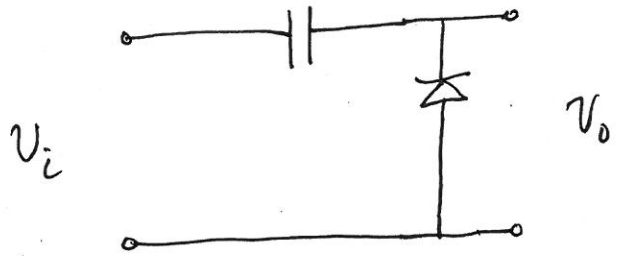
$v_{o\,min}$ = -18

$v_{o\,max}$ = 0

d) Using diodes and capacitors design clamper circuits for a -6V to 6V peak to peak square wave periodic input, v_I, to satisfy the following output specifications. Assume that the time constant of the circuit are much larger than the cycle time (period) of the input wave form. Assume ideal diode models.

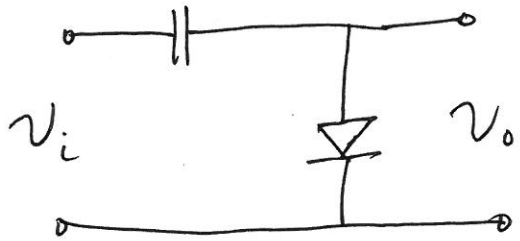
i. Output specification: $0V \leq v_o \leq 12V$

(2 marks)



ii. Output specification: $-12V \leq v_o \leq 0V$

(2 marks)



Q3

Q4: BJT

For the amplifier in Fig. 4.1, $V_{CC} = 15V$. The values for the resistors are $R_1 = 12K\Omega$, $R_2 = 8.5K\Omega$, $R_3 = 1K\Omega$, $R_4 = 1K\Omega$, $R_s = 10\Omega$, and $R_L = 2K\Omega$. The values of the coupling capacitors C_1, C_2 and C_3 are very large and can be considered to be infinity. The transistor parameter $\beta = 100$.

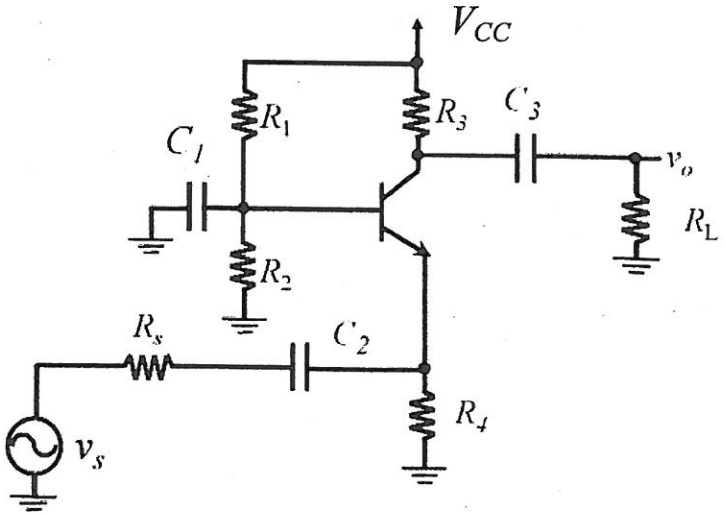
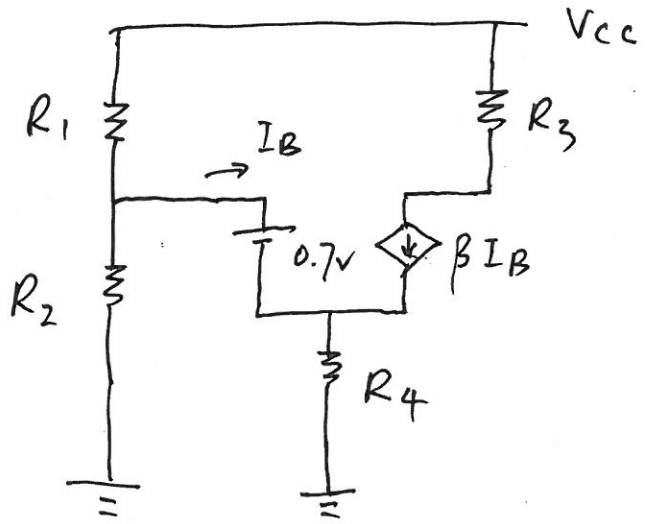


Fig. 4.1

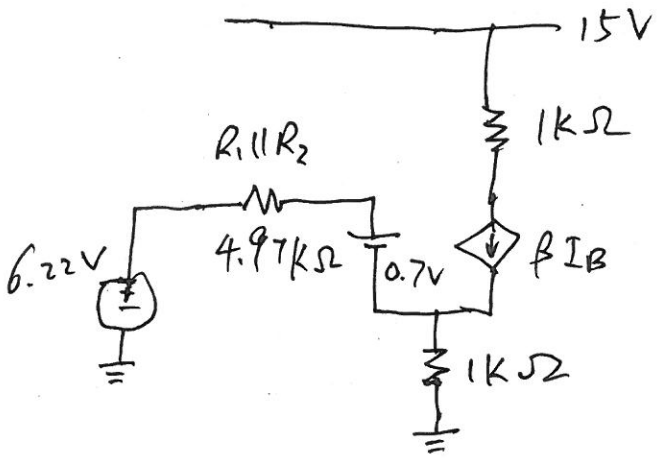
a) Draw the DC equivalent circuit that can be used for calculating DC voltages and currents **(3 marks)**



Q3.

b) Assuming room temperature, determine values for V_B, V_C, I_B, and I_C (Where V_B and V_C represent the voltages at the base and collector, respectively; and I_B, and I_C represent the currents through the base and the collector terminals, respectively.)

(7 marks)



$$I_B = \frac{6.22 - 0.7}{4.97 + 101 \times 1} = 0.05208\ mA$$

$I_c = 5.2\ mA$

$V_C = 15 - 1 \times 5.2 = 9.8\ V, \quad V_B = 1 \times 5.2 + 0.7 = 5.9\ V$

V_C= 9.8V

V_B= 5.9V

I_B= 0.052 mA

I_C= 5.2 mA

c) The BJT in Fig. 4.1 had an early voltage of 150V. Compute parameters $\mathbf{r_e}$, $\mathbf{g_m}$, **and** $\mathbf{r_o}$,

(3 marks)

$$g_m = \frac{I_C}{V_T} \longrightarrow \frac{5.2\ mA}{25\ mV} = 0.208\ A/V$$

$$r_e = \frac{\alpha}{g_m} = \frac{\beta}{1+\beta}\frac{1}{g_m} = \frac{0.99}{0.208} = 4.8\ \Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{150}{5.2} = 28.84\ K\Omega$$

g_m= 0.208 A/V

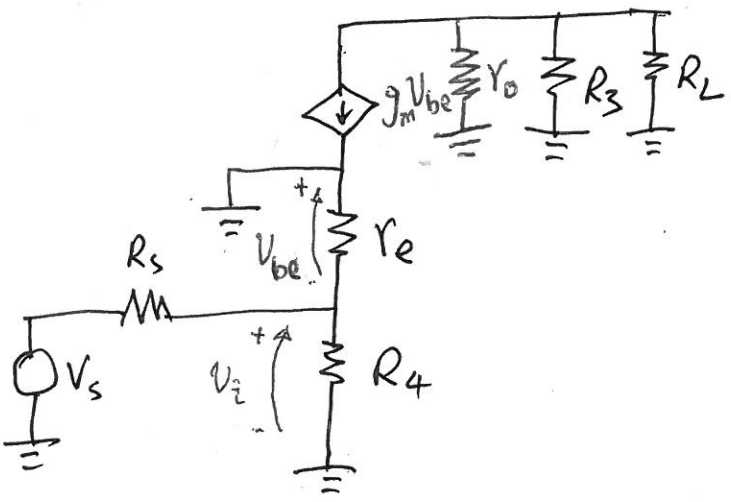
r_o= 28.84 KΩ

r_e = 4.8 Ω

d) Draw the small signal AC equivalent circuit based on parameters calculated above in c)

(5 marks)

Q1.



e) Find the value of the input resistance R_i

(2 marks)

$$R_i = R_4 \| r_e = \frac{1000 \times 4.8}{1000 + 4.8} = 4.77$$

R_i= 4.77

f) Find the value of the intermediate voltage gain, $A_{vl} = v_i/v_s$, where v_i is the small-signal voltage between the emitter and the ground.

(1 mark)

$$A_{v_1} = \frac{v_i}{v_s} = \frac{R_4 \| r_e}{R_s + R_4 \| r_e} = \frac{R_i}{R_s + R_i}$$

$$= \frac{4.77}{10 + 4.77} = 0.324$$

A_{v1}= 0.324

g) Find the value of the intermediate voltage gain $A_{v2} = v_o/v_i$.

(3 marks)

$$V_o = -g_m V_{be}(R_3 \| r_o \| R_L) = g_m V_i (R_3 \| r_o \| R_L)$$

$$A_{v2} = g_m (R_3 \| r_o \| R_L)$$

$$= 0.208 \times (1K \| 2K \| 28.84K)$$

$$= 0.208 \times (0.652\ K\Omega)$$

$$= 135.56$$

A_{v2}= 135.56

h) Find the overall voltage gain, $G_v = v_o/v_s$.

(1 mark)

$$A_v = A_{v1} \cdot A_{v2}$$

$$= 0.324 \times 135.56$$

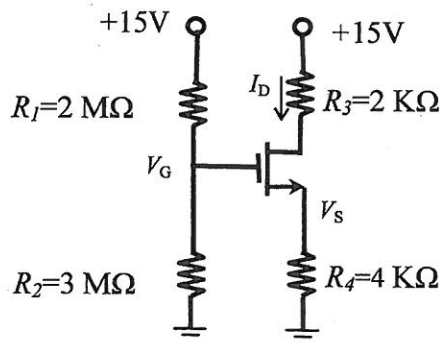
$$= 43.923$$

G_v= 43.92

Name:_____ Student #:_____ Section:_____

Q5: MOSFET

a) In the figure below, the transistor has $V_t = 1V$, $k_n' = 200\ \mu A/V^2$, $L = 1\ \mu m$, and $W = 5\ \mu m$.



i) Find the bias voltages V_G, V_S and current I_D **(3 marks)**

$V_G = \frac{3}{2+3} * 15 = 9$, $\quad K_n = k_n' \cdot \frac{W}{L} = 1\ mA/V^2$

$I_D = \frac{1}{2} K_n V_{OV}^2 = \frac{1}{2} K_n (V_G - V_S - V_t)^2 = \frac{1}{2}(8 - V_S)^2$

$I_D = \frac{V_S}{R_4} = \frac{1}{4} V_S$

$\frac{1}{2}(8 - V_S)^2 = \frac{1}{4} V_S$, $\quad 2V_S^2 - 33V_S + 128 = 0$

$V_S = \frac{33 \pm \sqrt{33^2 - 4 \cdot 2 \cdot 128}}{2 \times 2}$, $= \begin{cases} 10.2655 \\ 6.2344 \end{cases}$

$I_D = \frac{1}{4} V_S = \begin{cases} 2.566\ mA \\ 1.5586\ mA \leftarrow V \end{cases}$

V_G 9V $\quad V_S$ 6.23V $\quad I_D$ 1.558 mA

ii) Verify the mode of operation of the transistor and state what mode the transistor is in (**3 marks**)

$V_{GS} = V_G - V_S = 9 - 6.23 = 2.77 > V_t$

$V_{DS} = 15 - 2k\Omega \times 1.558mA - 6.23V$

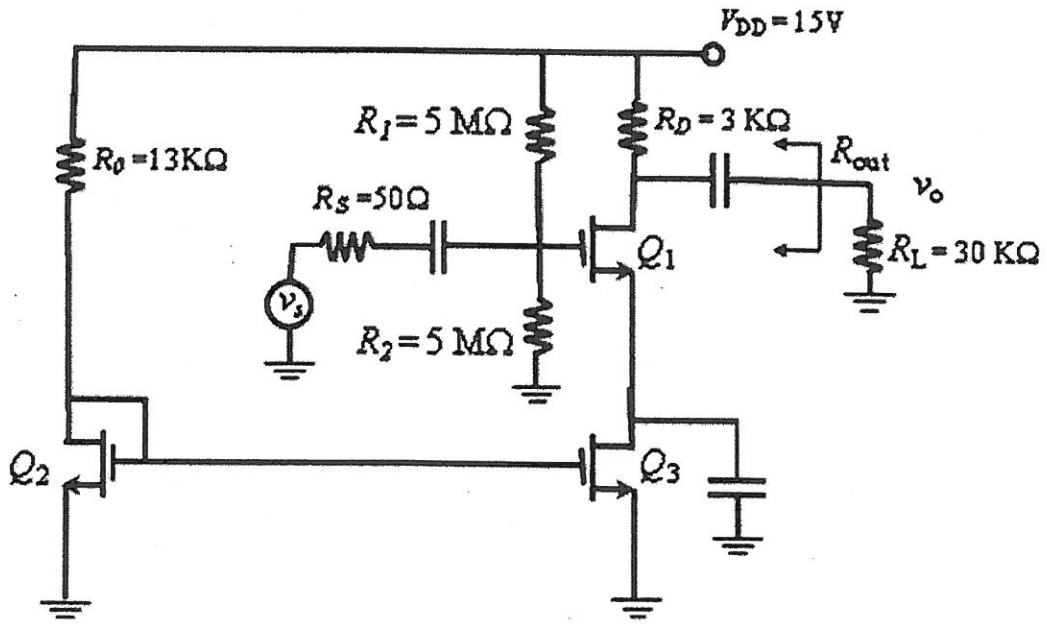
$= 5.654$

$V_{ov} = V_{GS} - V_t = 2.77 - 1 = 1.77$

$V_{DS} > V_{ov}$ ✓

Mode= Saturation

b) Consider the amplifier in the figure below. Assume that for all the MOSFETs, $V_t = 1V$, $k_n' = 200\ \mu A/V^2$. The channel length of the MOSFETs are $L_1 = L_2 = L_3 = 1\ \mu m$. The channel width are $W_1 = 10\ \mu m$, $W_2 = 10\ \mu m$, and W_3 is unknown.



i). Assume that the current mirror by Q_2 and Q_3 will provide a constant current of 2mA to bias the transistor Q_1. Determine channel width W_3. **(3 marks)**

$$\frac{I_{D2}}{I_{D3}} = \frac{W_2/L_2}{W_3/L_3}, \quad I_{D3} = 2mA, \quad K_n = k_n' \frac{W}{L} =$$

$$I_{D2} = \frac{V_{DD} - V_{GS}}{R_0} = \frac{15 - V_{GS}}{13}$$

$$I_{D2} = \frac{1}{2} k_n' \frac{W_2}{L_2} (V_{GS} - V_t)^2 = (V_{GS} - 1)^2$$

$$\frac{15 - V_{GS}}{13} = (V_{GS} - 1)^2, \quad 13V_{GS}^2 - 25V_{GS} - 2 = 0$$

$$V_{GS} = \frac{25 \pm \sqrt{25^2 + 4 \times 13 \times 2}}{2 \times 13} = \frac{25 \pm 27}{26} = \begin{cases} 2 & \leftarrow V \\ -0.076 & \leftarrow X \end{cases}$$

$$V_{GS} = 2V$$

$$I_{D2} = 1mA$$

$$\frac{I_{D2}}{I_{D3}} = \frac{W_2/L_2}{W_3/L_3}, \Rightarrow \frac{1}{2} = \frac{10}{W_3} \Rightarrow W_3 = 20$$

W_3 20 μm

ii). Compute the small-signal parameter g_m of transistor Q_1, assuming the drain current for Q1 is biased at 2mA. **(2 marks)**

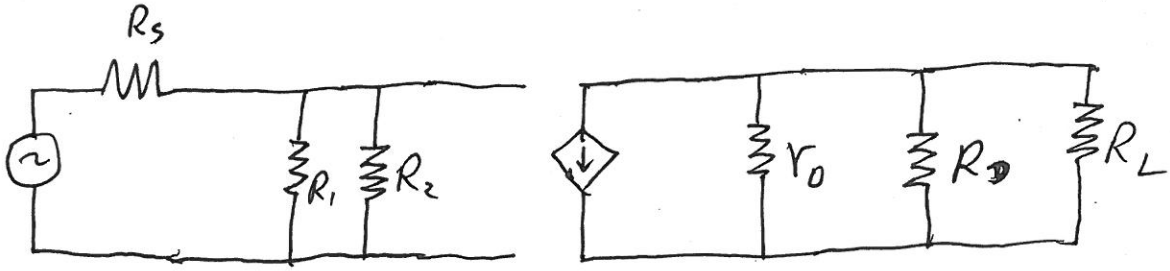
$$g_m = \frac{2 I_{D1}}{V_{OV}}$$

$$I_{D1} = 2mA, \quad I_{D1} = \frac{1}{2} k_n' \frac{W_1}{L_1} V_{OV}^2 = V_{OV}^2, \quad V_{OV} = \sqrt{I_{D1}} = 1.414$$

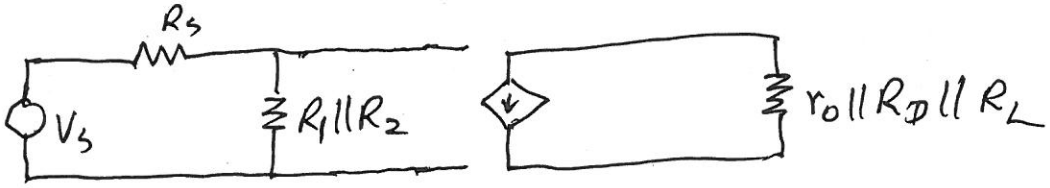
$$g_m = \frac{2 I_{D1}}{V_{OV}} = \frac{2 \times 2}{1.414} = 2.828$$

g_m 2.828 A/V

iii). Assume that the current mirror by Q_2 and Q_3 makes an ideal current source. Assume all the capacitors are infinitely large. Suppose the channel length modulation for Q_1 is to be considered. Draw the small-signal equivalent circuit. **(2 marks)**



or



iv). Compute a value for the voltage gain $G_v = v_0/v_s$ assuming that V_A= 100V for Q_1. **(5 marks)**

$$r_o = \frac{V_A}{I_D} = \frac{100}{2mA} = 50K\Omega$$

$$v_o = -g_m v_{gs} (r_o \| R_D \| R_L)$$

$$v_{gs} = \frac{R_1 \| R_2}{R_S + R_1 \| R_2} \cdot v_s$$

$$G_v = \frac{v_o}{v_s} = -g_m (r_o \| R_D \| R_L) \cdot \frac{R_1 \| R_2}{R_S + R_1 \| R_2}$$

$$= -2.828 \times 2.5864 \cdot \frac{2.5}{2.5 + 50 \times 10^{-6}}$$

$$= -7.314$$

G_v = −7.314

v). Compute the value of the amplifier output resistance R_{out}. **(2 marks)**

$$R_{out} = R_D \| r_o$$

$$= 3K\Omega \| 50K\Omega$$

$$= \frac{3 \times 50}{3 + 50}$$

$$= 2.83K\Omega$$

R_{out} = 2.83 KΩ

END