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Faculty of Engineering
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CEG2136: Computer Architecture I / CEG2536: Architecture des Ordinateurs I
MIDTERM EXAMINATION
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Question 1 (20 points)

a) (5 points) You have a SRAM memory chip with a capacity of 64k x 8

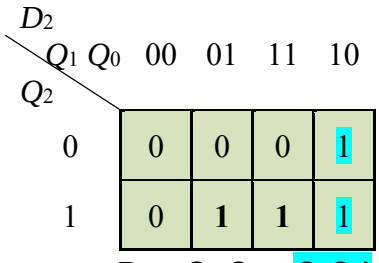
1) How many data lines does it have? *Answer 1)* .....**8**.....
2) How many address lines does it have? *Answer 2)* .....**16**.....
3) What is its capacity expressed in "*bits*"? *Answer 3)* $2^{16}2^3$ bits = $\mathbf{2^{19}}$ bits = 2^9 kbits = 512 kbits = 0.5 M bits

b) **15 points** Using D-type flip-flops, design a 3-bit Gray code counter which has the following counting sequence:

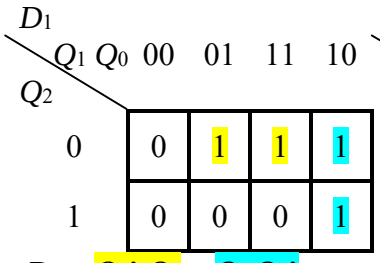
000 → 001 → 011 → 010 → 110 → 111 → 101 → 100
↑← ← ← ← ← ← ← ← ← ← ← ← ← ←↓

Draw the transition table of the counter and derive the excitation equations of the D flip flops' inputs.

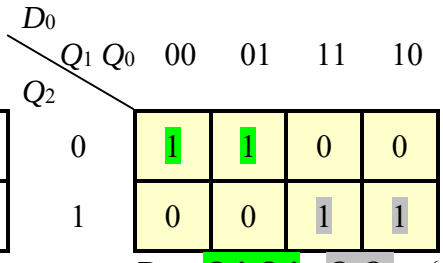
$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	D_2	D_1	D_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	1
0	1	0	1	1	0	1	1	0
0	1	1	0	1	0	0	1	0
1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	0	1



$D_2 = \mathbf{Q_2\, Q_0} + Q_1Q_0'$

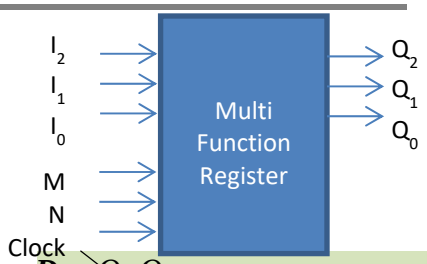


$D_1 = Q_2'\, Q_0 + Q_1\, Q_0'$



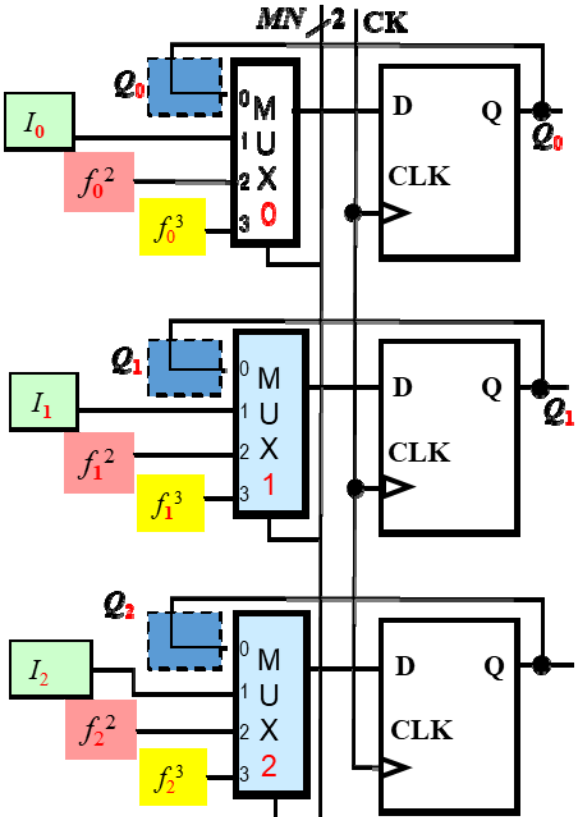
$D_0 = Q_2'\, Q_1' + Q_2Q_1 = (Q_1 \oplus Q_0)'$

Question 2 (20 points) Design a 3-bit register whose function is described in the following table, where M and N are two control bits. Using the proper digital components (encoders, decoders, multiplexers, etc.) logic gates, and D flip-flops, draw a detailed diagram of the logic circuit of the register.



f^{MN}	M	N	Operation	With counters	Next state	D_i
f^0	0	0	No change		$Q_2\ Q_1\ Q_0$	Q_i
f^1	0	1	Loading external inputs $I_2I_1I_0$	$I_2\ \ I_1\ \ I_0$		I_i
f^2	1	0	Decrement by 1 (count down)	$Q_2\ Q_1\ Q_0$ -1		?
f^3	1	1	Increment by 3 (count up)	$Q_2\ Q_1\ Q_0$+3		?

Using the D FF Excitation equation $D_i = Q_i^{n+1}$ for i=0,1,2



f^2: MN=10: Q-1

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

f_0^2: $D_0 = Q_0'$

D_2 $Q_1\ Q_0$: 00 01 11 10 / Q_2: 0 → 1 0 0 0; 1 → 0 1 1 1

$D_2 = Q_2Q_1 + Q_2Q_0 + Q_2'Q_1'Q_0'$

f_2^2: $D_2 = (Q_2 \oplus (Q_0 + Q_1))'$

D_1 $Q_1\ Q_0$: 00 01 11 10 / Q_2: 0 → 1 0 1 0; 1 → 1 0 1 0

$D_1 = Q_1'Q_0' + Q_1Q_0 = Q_1 \odot Q_0$

f_1^2: $D_1 = (Q_1 \oplus Q_0)'$

f^3: MN=11: Q+3

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	0	1	0

f_0^3: $D_0 = Q_0'$

D_2 $Q_1\ Q_0$: 00 01 11 10 / Q_2: 0 → 0 1 1 1; 1 → 1 0 0 0

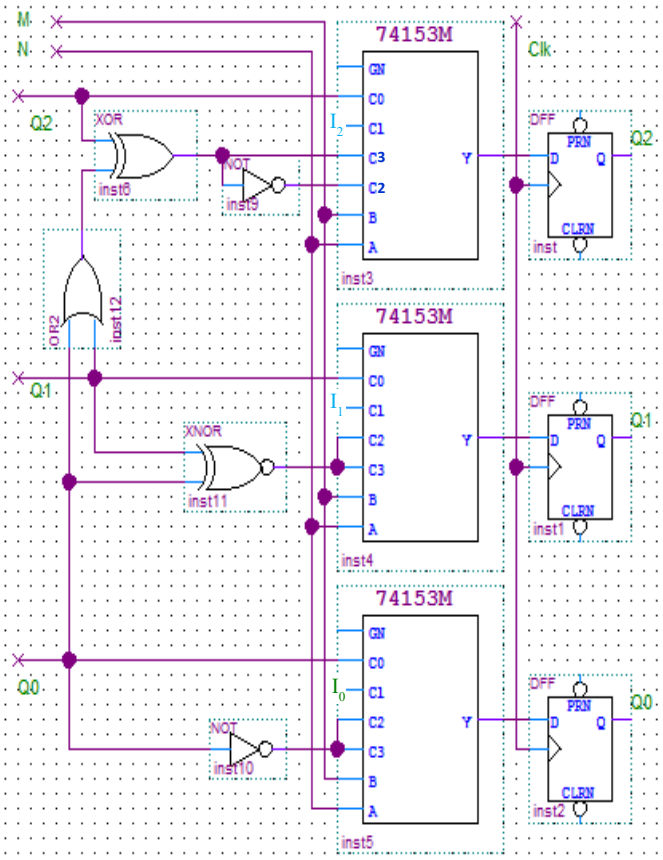
$D_2 = Q_2'Q_1 + Q_2'Q_0 + Q_2Q_1'Q_0'$

f_2^3: $D_2 = Q_2 \oplus (Q_0 + Q_1)$

D_1 $Q_1\ Q_0$: 00 01 11 10 / Q_2: 0 → 1 0 1 0; 1 → 1 0 1 0

$D_1 = Q_1'Q_0' + Q_1Q_0 = Q_1 \odot Q_0$

f_1^3: $D_1 = (Q_1 \oplus Q_0)'$



OR Comprehensive solution:

Control	Present State			Next State			Excitation Equations
MN	$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	
00	x	x	x	$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$D_i = Q_i$, i = 0,1,2
01	x	x	x	I_2	I_1	I_0	$D_i = I_i$, i = 0,1,2
10	0	0	0	1	1	1	
	0	0	1	0	0	0	$D_2 = Q_2(Q_0+Q_1) + Q_2'Q_1'Q_0'$
	0	1	0	0	0	1	$= Q_2 \odot (Q_1+Q_0)$
	0	1	1	0	1	0	$D_1 = Q_1'Q_0'+Q_1Q_0$
	1	0	0	0	1	1	
	1	0	1	1	0	0	$D_0 = Q_0'$
	1	1	0	1	0	1	
	1	1	1	1	1	0	
11	0	0	0	0	1	1	
	0	0	1	1	0	0	$D_2 = Q_2'(Q_0+Q_1) + Q_2Q_1'Q_0'$
	0	1	0	1	0	1	$= Q_2 \oplus (Q_1+Q_0)$
	0	1	1	1	1	0	$D_1 = Q_1'Q_0'+Q_1Q_0$
	1	0	0	1	1	1	
	1	0	1	0	0	0	$D_0 = Q_0'$
	1	1	0	0	0	1	
	1	1	1	0	1	0	

$D_2 = M'N'Q_2 + M'N\, I_2 + M\, N'\, Q_2 \odot (Q_1+Q_0) + M\, N\, Q_2 \oplus (Q_1+Q_0)$

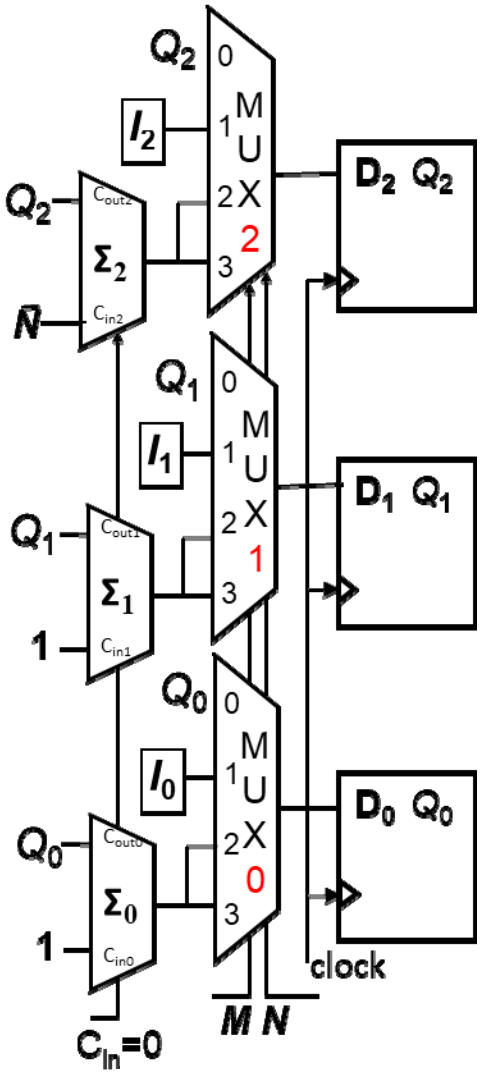
$D_1 = M'N'Q_1 + M'N\, I_1 + M\, N'\, (Q_1 \odot Q_0) + M\, N\, (Q_1 \odot Q_0) = M'N'Q_1 + M'N\, I_1 + M\, (Q_1 \odot Q_0)$

$D_0 = M'N'Q_0 + M'N\, I_0 + M\, Q_0'$

Implementation with MUX's and gates (as above) or with gates, exclusively.

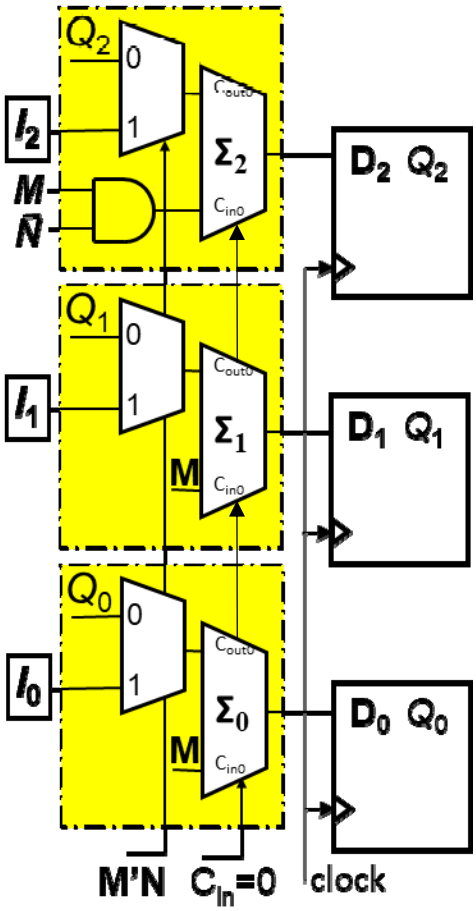
… or with MUX's & adders

MN	Operation	$D_2D_1D_0$
00	No change	$Q_2\ Q_1\ Q_0$
01	Loading $I_2\ I_1\ I_0$	$I_2\ \ I_1\ \ I_0$
1 0	Decrement by 1	$Q_2\ Q_1\ Q_0 + 1\ 1\ 1$
1 1	Increment by 3	$Q_2\ Q_1\ Q_0 + 0\ 1\ 1$



… or with adders

MN	$D_2D_1D_0$ =	1st term +	2nd term +	*cy*
00	$Q_2Q_1Q_0$ =	$Q_2\ Q_1\ Q_0$ +	0 0 0 +	0
01	$I_2\ I_1\ I_0$ =	$I_2\ \ I_1\ \ I_0$ +	0 0 0 +	0
1 0	$Q_2Q_1Q_0$ -1 =	$Q_2\ Q_1\ Q_0$ +	1 1 1 +	0
1 1	$Q_2Q_1Q_0$+3 =	$Q_2\ Q_1\ Q_0$ +	0 1 1 +	0



Question 3 (30 points)

The 2's complement representation is used in an 8-bit register which contains the binary value 11011000.

a. What is the decimal value of the number stored initially in the register?

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
R	1	1	0	1	1	0	0	0

Conversion to decimal

1101 1000 = - x => x = 2's complement of 1101 1000 = 0010 1000 = 40 => 1101 1000 = **- 40**

or

$1101\ 1000 = -2^7 + 2^6 + 2^4 + 2^3 = -128 + 64 + 16 + 8 = -128 + 88 = -40$

b. What is the register value after an arithmetic shift right? Give your result both in binary and decimal.

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0	1	1	0	0	0
1	1	1	0	1	1	0	0

Conversion to decimal

1110 1100 = -y => y = 2's complement of 1110 1100 = 0001 0100 = 20 => 1110 1100 = - 20

or

$1110\ 1100 = -2^7 + 2^6 + 2^5 + 2^3 + 2^2 = -128 + 64 + 32 + 8 + 4 = -128 + 108 = -20$

c. Starting again from the initial number 11011000, determine the register value after an arithmetic shift left, both in binary and decimal.

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0	1	1	0	0	0
1	0	1	1	0	0	0	0

Conversion to decimal:

1011 0000 = -z => z = 2's complement of 1011 0000 = 0101 0000 = 64+16 = 80 => 1011 0000 = - 80

or

$1011\ 0000 = -2^7 + 2^5 + 2^4 = -128 + 32 + 16 = -128 + 48 = -80$

d. What arithmetic operations are performed by these shifts?

Division by 2 in b.
Multiplication by 2 in c.

e. Is there any overflow?

NO

Justify your answer.

Both results (-20 and -80) can be represented with 8 bits 2's complement representation, i.e., are included in the range of the numbers that can be represented with 8 bits 2's complement representation [-128,127]: -128 < -20 < 127 and -128 < -80 < 127
Overflow can be signalized by a circuit that detects if the 2 m.s.b. are not identical, but not carry, since there are no adders to generate carries.

Question 4 (30 points)

A 3-bit arithmetic circuit takes three control bits, x, y and z, and two 3-bit data inputs, A and B. The operations supported by the arithmetic unit are described in the following table. Draw a detailed logic diagram of the circuit using 1-bit full adders and the digital components of your choice (encoders, decoders, multiplexers, etc.) (Note: A' is the 1's complement of A)

x y \ z	0	1
0 0	F = A + B (add)	F = A + B + 1
0 1	F = A + B'	F = A - B (subtract)
1 0	F = A (transfer)	F = A + 1 (increment)
1 1	F = A - 1 (decrement)	F = A' + 1 (2's complement of A)

The result F will be calculated with 3 adders:

$F = R + S + cy = F_2F_1F_0 = R_2R_1R_0 + S_2S_1S_0 + cy$

x y \ z	0	1
0 0	$A_2A_1A_0 + B_2\ B_1\ B_0 + 0$	$A_2\ A_1\ A_0 + B_2\ B_1\ B_0 + 1$
0 1	$A_2A_1A_0 + B_2'B_1'B_0' + 0$	$A_2\ A_1\ A_0 + B_2'B_1'B_0' + 1$
1 0	$A_2A_1A_0 + 0\ 0\ 0 + 0$	$A_2\ A_1\ A_0 + 0\ 0\ 0 + 1$
1 1	$A_2A_1A_0 + 1\ 1\ 1 + 0$	$A_2'A_1'A_0' + 0\ 0\ 0 + 1$

NOTE: MUX's inputs might be numbered in a weird order below!!!