

Quiz 1
Fall 2019

Odd

- Q1. The next figure shows the state diagram of a logic circuit which has a unique one-bit external input x .
- Start off by deriving the state table of the circuit. Then, assuming that JK flip-flops are to be used in the implementation, extend the state table with the excitation table of the circuit.
 - Find simplified expressions for each flip-flop inputs.

SOLUTION:

1. Map the FSM logic diagram to State table.

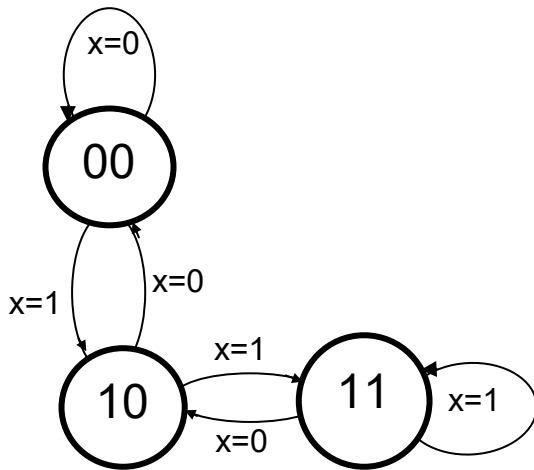
To find the excitation table, fill the J and K columns using:

A) the “copy & paste recipe:”

- $J = \text{next state}$ if present state is 0
- $J = \text{don't care (x)}$ if present state is 1
- $K = \text{don't care (x)}$ if present state is 0
- $K = \text{complement of the next state}$ if present state is 1

... or B) The JK FF Excitation Table, i.e.:

	if $Q^n = 0$	if $Q^n = 1$
J =	[1] Q^{n+1}	[2] x
K =	[3] x	[4] $(Q^{n+1})'$



	A^n	B^n	X	A^{n+1}	B^{n+1}	J_A	K_A	J_B	K_B
or:	Q_1^n	Q_0^n		Q_1^{n+1}	Q_0^{n+1}	J_1	K_1	J_0	K_0
(0)	0	0	0	0	0	0	x	0	x
(1)	0	0	1	1	0	1	x	0	x
(2)	0	1	0	x	x	x	x	x	x
(3)	0	1	1	x	x	x	x	x	x
(4)	1	0	0	0	0	x	1	0	x
(5)	1	0	1	1	1	x	0	1	x
(6)	1	1	0	1	0	x	0	x	1
(7)	1	1	1	1	1	x	0	x	0

2. Find simplified expressions for each flip-flop inputs

J_A

	BX	00	01	11	10
A		0	1	3	2
0		0	1	x	x
1		x	x	x	x

$J_A = X$

K_A

	BX	00	01	11	10
A		0	1	3	2
0		x	x	x	x
1		1	0	0	0

$K_A = B'X'$

J_B

	BX	00	01	11	10
A		0	1	3	2
0		0	0	x	x
1		0	1	x	x

$J_B = AX$

K_B

	BX	00	01	11	10
A		0	1	3	2
0		x	x	x	x
1		x	x	0	1

$K_B = X'$

OR

b)

$J_1 = X$

	Q_1	Q_0	00	01	11	10
X						
0	0	x	x	x		
1	1	x	x	x		

$K_1 = Q'_0 X'$

	Q_1	Q_0	00	01	11	10
X						
0	x	x	0	1		
1	x	x	0	0		

$J_0 = X Q_1$

	Q_1	Q_0	00	01	11	10
X						
0	0	x	x	0		
1	0	x	x	1		

$K_0 = X'$

	Q_1	Q_0	00	01	11	10
X						
0	x	x	1	x		
1	x	x	0	x		

P2. Design a 3-bit shift right register which has a data input *Serial In* and a control input “*Sh*” (shift). The operation of the sequential circuit is described in the functional Table 1. Design the sequential circuit using three D flip-flops.

(P2.1.) Provide the equations for the next state variables of the D flip-flops $\{Q_i^{n+1}, i = [0, 1, 2]\}$

(P2.2.) Draw the logic diagram of the circuit that you designed; explain your work.

(P2.3.) Design a D flip-flop using a T flip-flop; draw the logic diagram of your designed D FF.

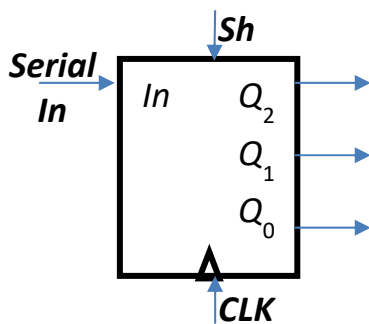


Table 1.

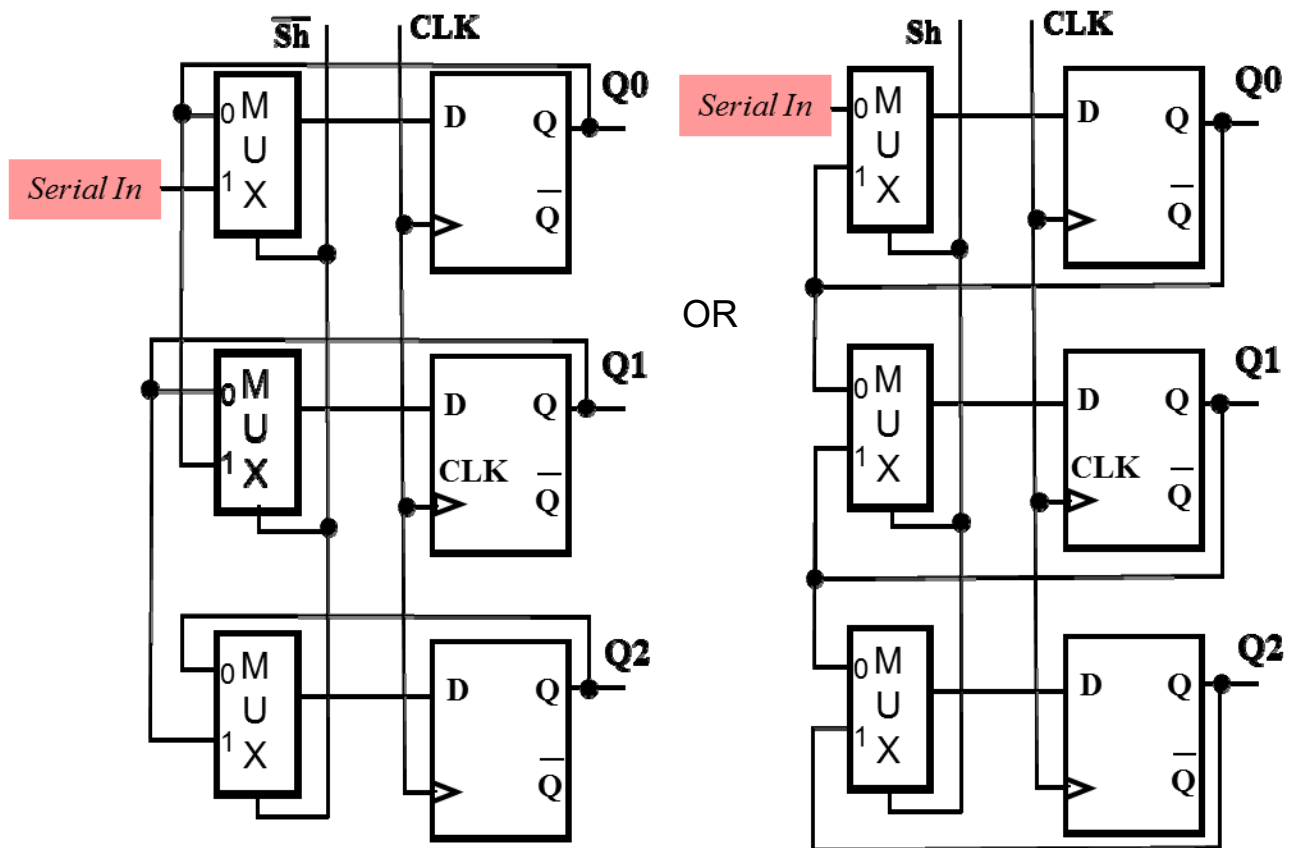
<i>Sh</i>	Function	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	Shift Left	Q_1^n	Q_0^n	Serial In
1	Preserve present state	Q_2^n	Q_1^n	Q_0^n

$$Q_2^{n+1} = Sh Q_2^n + Sh' \cdot Q_1^n$$

$$Q_1^{n+1} = Sh Q_1^n + Sh' \cdot Q_0^n$$

$$Q_0^{n+1} = Sh Q_0^n + Sh' \cdot \text{Serial In}$$

(P2.2.) Draw the logic diagram of the circuit that you designed.



... or implementation with gates!

(P2.3) Design a D flip-flop using a T flip-flop; draw the logic diagram of your designed D FF

Q^n	D	Q^{n+1}	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

or $T = \overline{Q^n} \cdot T + Q^n \cdot \overline{T}$
 $T = Q^n \oplus T$

