uOttawa
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NAME / ID#

**Quiz 1**
**Fall**
**2018**

**Odd**

P1. The next figure shows the state diagram of a logic circuit which has a unique one-bit external input x.

1. Start off by deriving the state table of the circuit. Then, assuming that JK flip-flops are to be used in the implementation, extend the state table with the excitation table of the circuit.
2. Find simplified expressions for each flip-flop inputs.

**SOLUTION:**

**1.** 13 points Map the FSM logic diagram to State table.

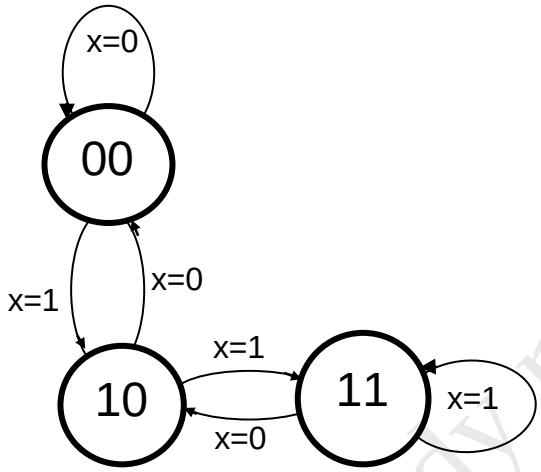
To find the excitation table, fill the J and K columns using:

A) the "copy & paste recipe:"

[1] J = next state if **present state is 0**
[2] J = don't care (x) if ***present state is 1***
[3] K = don't care (x) if **present state is 0**
[4] K = complement of the next state if present state is 1

… or B) The JK FF Excitation Table, i.e.:

| | if $Q^n = 0$ | if $Q^n = 1$ |
|---|---|---|
| J = | [1] $Q^{n+1}$ | [2] x |
| K = | [3] x | [4] $(Q^{n+1})'$ |

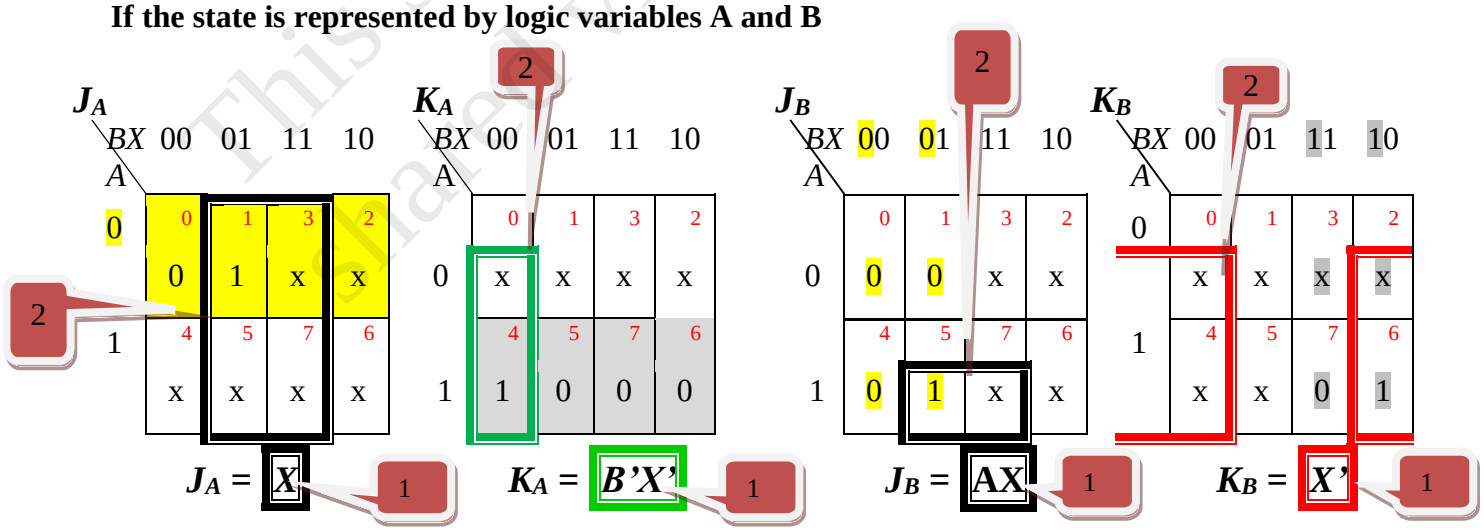



1 point for correct labeling the table

| | $A^n$ or $Q_1^n$ | $B^n$ or $Q_0^n$ | $X$ | $A^{n+1}$ or $Q_1^{n+1}$ | $B^{n+1}$ or $Q_0^{n+1}$ | $J_A$ or $J_1$ | $K_A$ or $K_1$ | $J_B$ or $J_2$ | $K_B$ or $K_0$ |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 0.5 x 8 = **4** | | 0.5 x 8 = **4** | | 0.5 x 8 = **4** | |
| (0) | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x |
| (1) | 0 | 0 | 1 | 1 | 0 | 1 | x | 0 | x |
| (2) | 0 | 1 | 0 | x | x | x | x | x | x |
| (3) | 0 | 1 | 1 | x | x | x | x | x | x |
| (4) | 1 | 0 | 0 | 0 | 0 | x | 1 | 0 | x |
| (5) | 1 | 0 | 1 | 1 | 1 | x | 0 | 1 | x |
| (6) | 1 | 1 | 0 | 1 | 0 | x | 0 | x | 1 |
| (7) | 1 | 1 | 1 | 1 | 1 | x | 0 | x | 0 |

**2.** 12 points Find simplified expressions for each flip-flop inputs

**If the state is represented by logic variables A and B**



**OR, if the state is represented by logic variables $Q_1$ and $Q_0$**

**b)**

$J_1 = X$

| $Q_1\,Q_0$ / $X$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | x | x | x |
| 1 | 1 | x | x | x |

$K_1 = Q'_0\,X'$

| $Q_1\,Q_0$ / $X$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | x | x | 0 | 1 |
| 1 | x | x | 0 | 0 |

$J_0 = X\,Q_1$

| $Q_1\,Q_0$ / $X$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | x | x | 0 |
| 1 | 0 | x | x | 1 |

$K_0 = X'$

| $Q_1\,Q_0$ / $X$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | x | x | 1 | x |
| 1 | x | x | 0 | x |

P2. 25 points Design a 3-bit shift ~~**right**~~ left register which has a data input *Serial In* and a control input "*Sh*" (shift). The operation of the sequential circuit is described in the functional Table 1. Design the sequential circuit using three D flip-flops.

(P2.1.) 6 pts Provide the *equations for the next state variables* of the D flip-flops $\{Q_i^{n+1},\ i = [0, 1, 2]\}$, by firstly filling out the *next state* columns of Table 1.

(P2.2.) 13 pts Draw the logic diagram of the circuit that you designed; explain your work.

(P2.3.) 6 pts Design a D flip-flop using a T flip-flop; draw the logic diagram of your designed D flip-flop.

**Because of the typo in the first line of question (written "right" instead of "left", do accept any implementation: left or right**

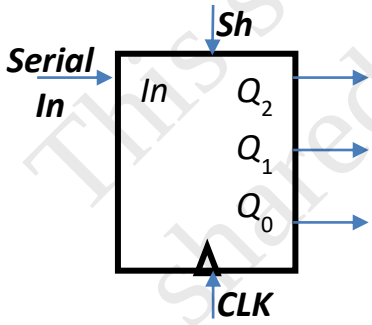



Table 1.

| *Sh* | Function | $Q_2^{n+1}$ | $Q_1^{n+1}$ | $Q_0^{n+1}$ |
|---|---|---|---|---|
| **0** | *Shift Left* | $Q_1^n$ | $Q_0^n$ | ***Serial In*** |
| **1** | *Preserve present state* | $Q_2^n$ | $Q_1^n$ | $Q_0^n$ |

0.5 0.5 0.5 0.5 0.5 0.5

$Q_2^{n+1} = Sh\ Q_2^n + Sh' \cdot Q_1^n$

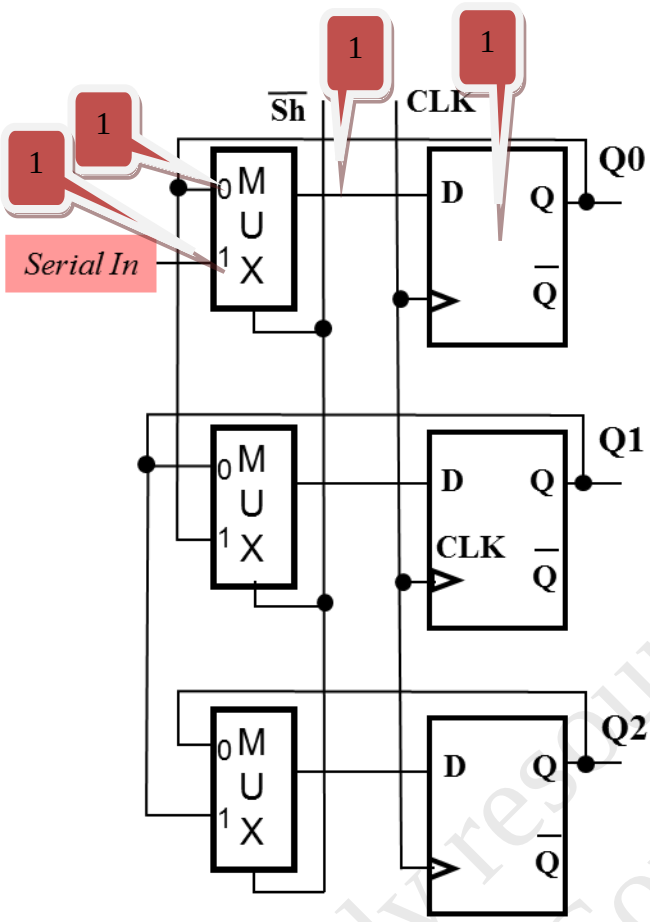
$Q_1^{n+1} = Sh\ Q_1^n + Sh' \cdot Q_0^n$

$Q_0^{n+1} = Sh\ Q_0^n + Sh' \cdot Serial\ In$

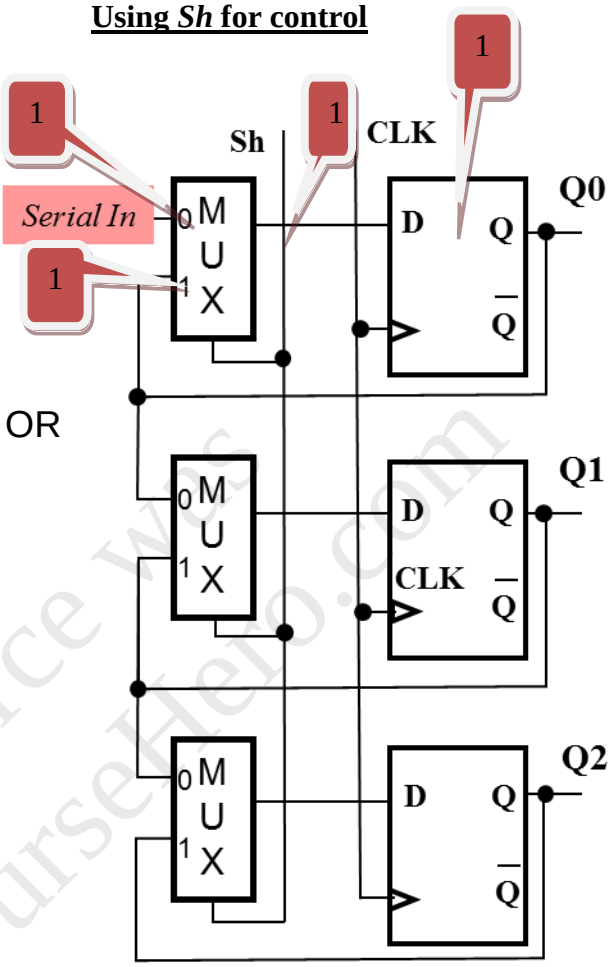
1 1 1

***(P2.2.)*** Draw the logic diagram of the circuit that you designed. 13 pts = 3 x 4 pts +1point (for clock & Sh)

**Using *Sh'* for control**




**Using *Sh* for control**



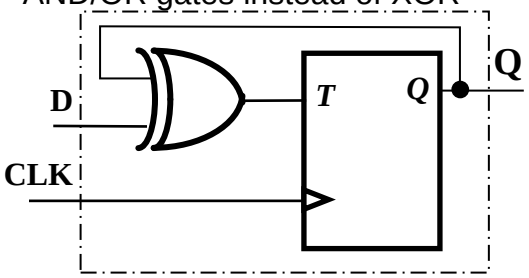

**… also accept implementation with gates!**

(P2.3) 6 pts Design a D flip-flop using a T flip-flop; draw the logic diagram of your designed D FF

| 1pt | $Q^n$ | $D$ | $Q^{n+1}$ | 1pt | T | 1pt |
|---|---|---|---|---|---|---|
| 0.25 | 0 | 0 | 0 | 0.25 | 0 | 0.25 |
| 0.25 | 0 | 1 | 1 | 0.25 | 1 | 0.25 |
| 0.25 | 1 | 0 | 0 | 0.25 | 1 | 0.25 |
| 0.25 | 1 | 1 | 1 | 0.25 | 0 | 0.25 |

2 pts = logic diagram

acceptable implementation with AND/OR gates instead of XOR




$T = Q'D + QD'$ or $T = Q \oplus D$ 1pt