Department of Electronics

ELEC 4601

Midterm Exam

Tuesday 18th October 14, 2016

2:35 to 3:55

Student ID:

Student Name:

Instructions:

1) **The exam is 5 questions.**
2) **Questions 1-4 are mandatory. Question 5 is optional.**
3) **This is a closed book exam.**
4) **Mention any assumption you make to answer any question.**
5) **Use the provided space to answer the questions. If more space is needed you can use back of pages.**

Question #1 (5 marks)

A. What is the basic difference between programmed I/O and interrupt-based I/O?

Interrupt-based I/I is **device-initiated** transfer while programmed I/O is **CPU-controlled** transfer

B. Explain the main advantage of Direct-Memory-Access (DMA) I/O mechanism over other I/O techniques.

DMA-controller performs the actual data transfer **without CPU involvement**

C. List the three main different types of microprocessor systems buses and the typical usage of each bus type.

1- **Internal bus: used for CPU internal components**
2- **Memory bus: for CPU-memory interface**
3- **I/O bus: for I/O devices**

D. What is the main difference between synchronous and asynchronous bus transfer? Mention one advantage of each transfer type

Synchronous bus transfer **needs a master clock**. Advantages: **simple implementation**
Asynchronous bus transfer **does not need master clock**. Advantages: could be **faster** since no waiting is needed for clock rising/falling edges

E. Instruction execution can be generally described by three phases 1) fetch, 2) decode, and 3) execute.

I. Explain briefly each phase

Fetch: copy instruction from **memory** to **instruction register**
Decode: Interpret/identify/ the **opcode**
Execute: generate **control signals** to execute the instruction

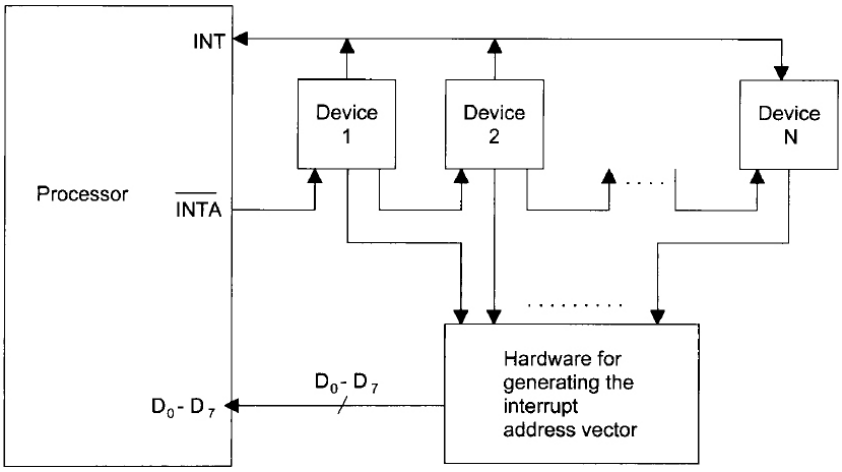
II. Explain how pipelining mechanism can be used to speed up the instruction execution

By executing the **three phases in parallel**, more instructions are executed in less number of cycles

Question #2 (5 marks)

The figure shown describes a daisy-chain mechanism where multiple devices can interrupt a processor.

A. Using the given diagram, explain the purpose of daisy-chain mechanism and how it handles multiple interrupts priorities.



Daisy-chain mechanism is responsible for organizing multiple interrupts from multiple devices.
In daisy-chain, **the closer** the device to the CPU **the higher** the priority of the device.

B. In order to execute an interrupt service routine, the processor must do a context switch. Explain what is the context switch and why it is needed to handle interrupts.

Context switching is the process of saving all registers information of the current program to prepare the CPU to serve a new program. It is needed in interrupt handling to save current program information before branching to the interrupt service routine and resuming the old program when interrupt service routine returns.

C. Mention another mechanism that can be used to handle multiple interrupts priorities.

Polling interrupt.

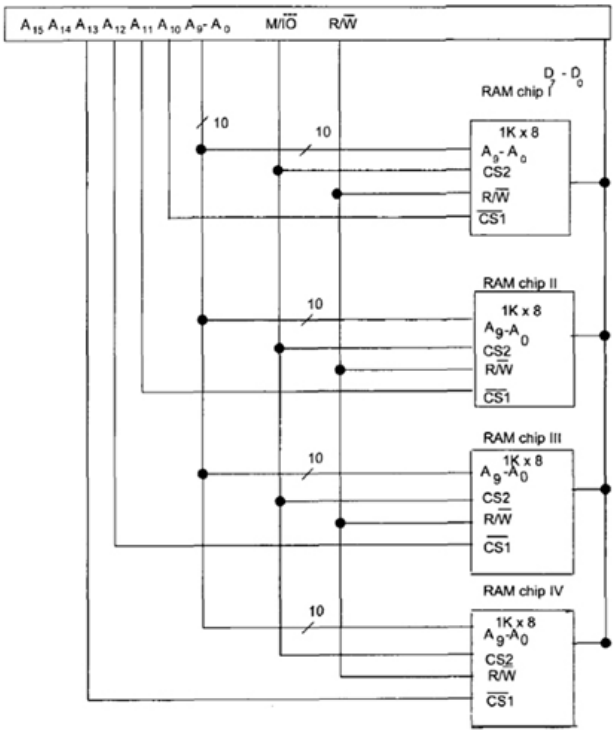
Question #3: (5 marks)

A 1KB RAM memory unit is used to build 4KB memory as shown in the given diagram. The 1KB memory unit is controled according to the given function table.

$\overline{CS1}$	CS2	R/$\overline{W}$	Function
0	1	0	Write Operation
0	1	1	Read Operation
1	X	X	The chip is not selected
X	0	X	The chip is not selected

Answer the following questions:

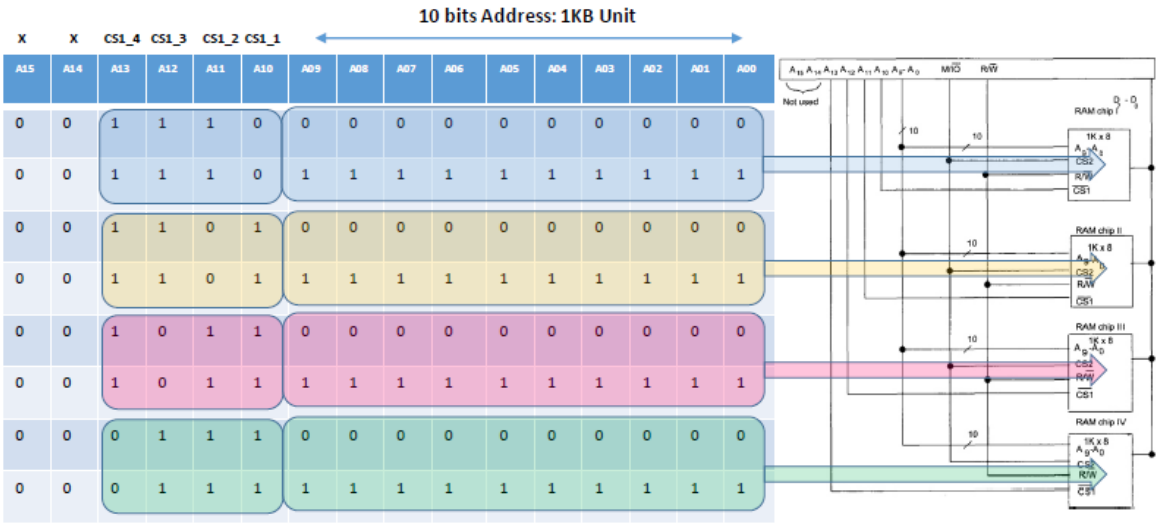
A. Explain in details how each memory unit will be selected and calculate the address space of each memory unit



RAM chip	Start Address (Hex)	End Address (Hex)
1		
2		
3		
4		

Check slide 16 of lecture 6 "memory organization and addressing modes"

See the address space numbers below. You should fill the table with these numbers

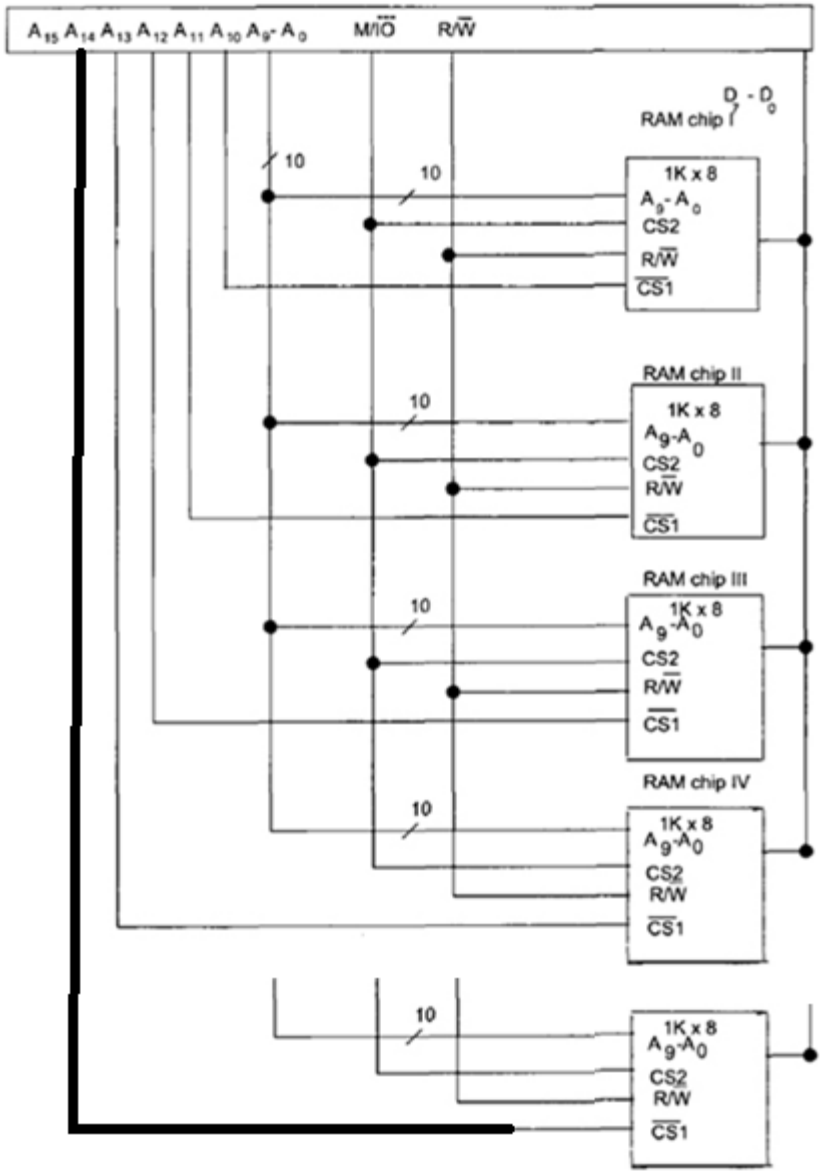


3800-3BFF → SRAM Unit 1 **2C00-2FFF → SRAM Unit 3**
3400-37FF → SRAM Unit 2 **1C00-1FFF → SRAM Unit 4**

Question #3 (continued):

B. Described how a fifth 1KB unit can be added and calculate the new address space for all the five 1KB units

RAM chip	Start Address (Hex)	End Address (Hex)
1		
2		
3		
4		
5		



See the address space numbers below. You should fill the table with these numbers

In the calculation table below, we can set A15 to 1 as well as it is a don't care bit. The solution in this case is also valid.

Unit	A15	A14	A13	A12	A11	A10	A9	A8	A7-A0	Address Range
1	0	1	1	1	1	0	0	0	00	7800
1	0	1	1	1	1	0	1	1	FF	7BFF
2	0	1	1	1	0	1	0	0	00	7400
2	0	1	1	1	0	1	1	1	FF	77FF
3	0	1	1	0	1	1	0	0	00	6C00
3	0	1	1	0	1	1	1	1	FF	6FFF
4	0	1	0	1	1	1	0	0	00	5C00
4	0	1	0	1	1	1	1	1	FF	5FFF
5	0	0	1	1	1	1	0	0	00	3C00
5	0	0	1	1	1	1	1	1	FF	3FFF

Question #3 (continued):

C. Mention two limitations of the given design and show how a full decoding design can be implemented to eliminate these two limitations. Use any necessary additional hardware components to realize your design and list the address spaces for the first 4 RAM units.

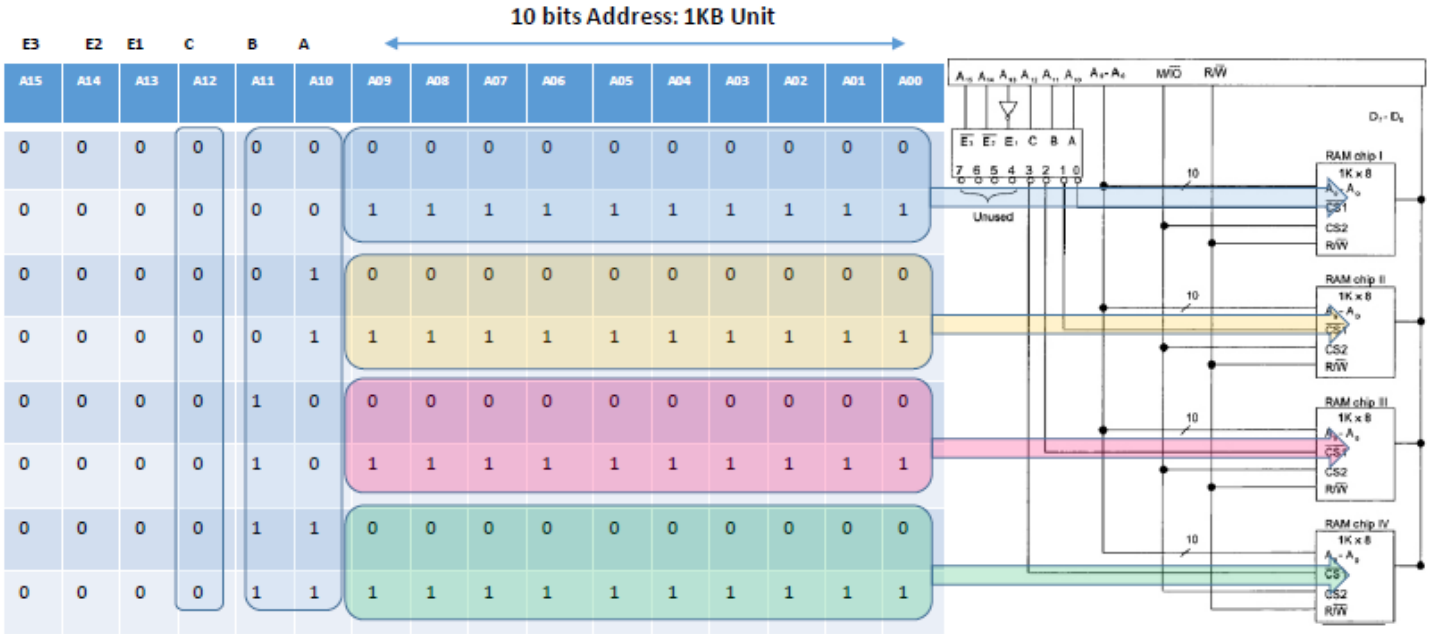
RAM chip	Start Address (Hex)	End Address (Hex)
1		
2		
3		
4		
5		

Draw your design here

Limitations are 1) Address space gaps 2) Two addresses may point to the same location 3) Software errors may select two memory chips at the same time.

Check slide 25 of lecture 6 “memory organization and addressing modes”

See the address space numbers below. You should fill the table with these numbers



Address Range (Hex)	RAM Chip Number
0000-03FF	I
0400-07FF	II
0800-0BFF	III
0C00-0FFF	IV

Question #4: (5 marks)

Consider a CPU executes instructions using three phases: Fetch, Decode, and Execute. Given the following assumptions:

- If the decode phase recognizes an EXIT or END instruction, the CPU will stop fetching new instructions and stop decoding any already fetched instructions.
- Branching instructions are recognized in the decoding phase. However, the branch target is known in the execute phase.

Program A

```
I1 print "A"      ;print letter A
I2 print "B"      ;print letter B
I3 print "C"      ;print letter C
I4 print "D"      ;print letter D
I5 END            ;terminate the program
```

Answer the following questions:

A. Without applying any pipelining mechanism, show the sequence of execution of program A and the generated output by filling the following table

Fetch	I1			I2			I3			I4			I5		
Decode		I1			I2			I3			I4			I5	
Execute			I1			I2			I3			I4			I5

Output A B C D

Time →

B. Show the execution sequence and generated outputs if a 3-phases pipeline is used to execute the instructions of program A. Use the generated outputs to discuss what advantages the pipelining mechanism provides.

Fetch	I1	I2	I3	I4	I5										
Decode		I1	I2	I3	I4	I5									
Execute			I1	I2	I3	I4	I5								

Output A B C D

Time →

With pipelining mechanism, execution is faster since all three phases are performed **simultaneously**.

Question #4 (continued):

C. Consider program B. Show the sequence of execution and the generated outputs output if the same 3-phases pipeline mechanism is applied without any special handling of branching instructions. Does the program generate the correct sequence? And if it does not explain the reasons.

Program B
I1 print "A"
I2 print "B"
I3 jump to I6
I4 print "D"
I5 EXIT
I6 print "C"
I7 jump to I4
I8 END

Fetch	**I1**	**I2**	**I3**	**I4**	**I5**	**I6**									
Decode		**I1**	**I2**	**I3**	**I4**	**I5**									
Execute			**I1**	**I2**	**I3**	**I4**	**I5**								

Output A B x D ....

Time →

Since the target branching is not known until the fifth cycle. By the fifth cycle, instructions I4 and I5 have been already decoded and fetched respectively. Because there is no special handling for branching instructions, the sequence of execution will be incorrect.

D. Mention two mechanisms that can be used to handle branching problems in pipelining.

Pre-fetching

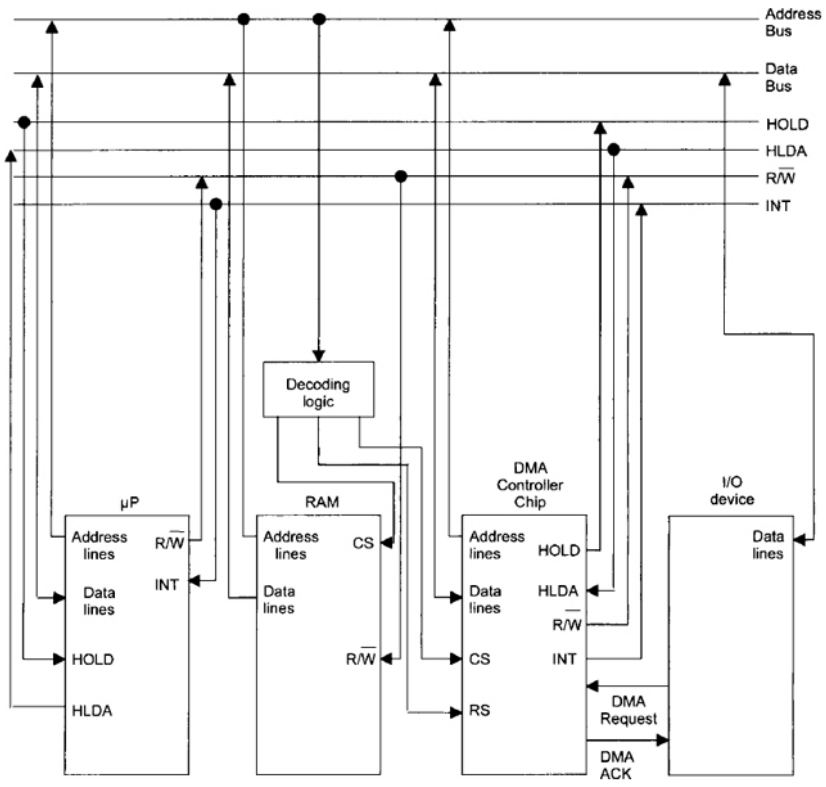
Delayed-fetching

Branching Prediction (software using optimized compilers or hardware using Branch Evaluation Unit)

Question #5: Optional (5 marks)

The given block diagram shows a direct memory access (DMA) I/O design

A. Explain the DMA-I/O concept.
B. Explain the detailed steps of DMA "block transfer" type using the signal names indicated on the given diagram.
C. Explain briefly the other two DMA transfer types.



A: Instead of keeping the CPU busy transferring data between an I/O device and the memory, a dedicated hardware component (DMA-controller) handles the transfer and releases the CPU from this overload.

B:

See lecture slides

➢I/O device requests DMA transfer via the DMA request line connected to the controller chip.

➢The DMA controller chip then sends a HOLD signal to the CPU and waits for the HOLD acknowledge (HLDA) signal.

➢On receipt of the HLDA, the controller chip sends a DMA ACK signal to the I/O device.

➢The controller takes over the bus and controls data transfer between RAM and the I/O device.

➢On the completion of data transfer, the controller interrupts the CPU by the INT line and returns the bus to the CPU by disabling the HOLD and DMA ACK signals.

C:

Cycle stealing: The microprocessor is stopped completely for one cycle and the DMA transfer is performed instead.

Interleaved DMA: DMA controller chip takes over the system bus when the CPU is not using it.