

*ENG3380* Assignment #1 (Solutions)  
School of Engineering, University of Guelph, Winter 2019

Prepared by: Shawki Areibi

1. Consider three different processors  $P_1$ ,  $P_2$  and  $P_3$  executing the same instruction set.  $P_1$  has a 3 GHz clock rate and a CPI of 1.5.  $P_2$  has a 2.5 GHz clock rate and CPI of 1.0.  $P_3$  has a 4.0 GHz clock rate and has a CPI of 2.2
- (a) **Which** processor has the highest performance expressed in instructions per second?
- (b) If the processors each execute a program in 10 seconds, **find** the number of cycles and the number of instructions.
- (c) we are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. **What** clock rate should we have to get this time reduction?

**Solution of Question #1:**

- (a) Processor  $P_2$  has the highest performance (instructions/second):
- Performance of  $P_1$  (instructions/sec) =  $\frac{3 \times 10^9}{1.5} = 2 \times 10^9$
  - Performance of  $P_2$  (instructions/sec) =  $\frac{2.5 \times 10^9}{1.0} = 2.5 \times 10^9$
  - Performance of  $P_3$  (instructions/sec) =  $\frac{4 \times 10^9}{2.2} = 1.8 \times 10^9$
- (b) The number of cycles:
- Cycles ( $P_1$ ) =  $10 \times 3 \times 10^9 = 30 \times 10^9$
  - Cycles ( $P_2$ ) =  $10 \times 2.5 \times 10^9 = 25 \times 10^9$
  - Cycles ( $P_3$ ) =  $10 \times 4 \times 10^9 = 40 \times 10^9$
- (c) The number of instructions:
- No. Instructions ( $P_1$ ) =  $\frac{10 \times 3 \times 10^9}{1.5} = 20 \times 10^9$
  - No. Instructions ( $P_2$ ) =  $\frac{10 \times 2.5 \times 10^9}{1.0} = 25 \times 10^9$
  - No. Instructions ( $P_3$ ) =  $\frac{10 \times 4 \times 10^9}{2.2} = 18.18 \times 10^9$
- (d) The required clock rate for each processor:
- Reducing execution time by 30% means that new execution time is 7 seconds.
  - $CPI_{new} = CPI_{old} \times 1.2$  .. So,  $CPI_{P_1} = 1.8$ ,  $CPI_{P_2} = 1.2$ ,  $CPI_{P_3} = 2.6$
  - $f = \frac{No.Instr \times CPI}{time}$ , then
    - $f(P_1) = \frac{20 \times 10^9 \times 1.8}{7} = 5.14$  GHz
    - $f(P_2) = \frac{25 \times 10^9 \times 1.2}{7} = 4.28$  GHz
    - $f(P_3) = \frac{18.18 \times 10^9 \times 2.6}{7} = 6.75$  GHz

2. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C and D).  $P_1$  with a clock rate of 2.5 GHz and CPIs of 1,2,3, and 3.  $P_2$  with a clock rate of 3 GHz and CPIs of 2,2,2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D. **Which** is faster Processor  $P_1$  or  $P_2$ ?

- (a) **What** is the global CPI for each implementation?  
 (b) **Find** the clock cycles required in both cases.

**Solution of Question #2:**

(a) The global CPI for each implementation:

- Since the given program with a dynamic instruction count of 1.0E6 instructions is divided into classes of 10% A, 20% B, 50% C and 20% D, then
  - Class A = 10%  $\times$  1.0E6 =  $10^5$  instr.
  - Class B = 20%  $\times$  1.0E6 =  $2 \times 10^5$  instr.
  - Class C = 50%  $\times$  1.0E6 =  $5 \times 10^5$  instr.
  - Class D = 20%  $\times$  1.0E6 =  $2 \times 10^5$  instr.
- $Time = \frac{No.Instr \times CPI}{ClockRate}$ 
  - Total Time  $P_1 = \frac{(10^5 \times 1) + (2 \times 10^5 \times 2) + (5 \times 10^5 \times 3) + (2 \times 10^5 \times 3)}{(2.5 \times 10^9)} = 10.4 \times 10^{-4} s$
  - Total Time  $P_2 = \frac{(10^5 \times 2) + (2 \times 10^5 \times 2) + (5 \times 10^5 \times 2) + (2 \times 10^5 \times 2)}{(3 \times 10^9)} = 6.66 \times 10^{-4} s$
- Global;CPI =  $\frac{TotalTime \times ClockRate}{InstructionCount}$ 
  - $CPI(P_1) = \frac{(10.4 \times 10^{-4}) \times (2.5 \times 10^9)}{10^6} = 2.6$
  - $CPI(P_2) = \frac{(6.66 \times 10^{-4}) \times (3.0 \times 10^9)}{10^6} = 2.0$

(b) The clock cycles required in both bases:

- Clock Cycles = Instruction Count x CPI
  - Clock Cycles( $P_1$ ) =  $(10^5 \times 1) + (2 \times 10^5 \times 2) + (5 \times 10^5 \times 3) + (2 \times 10^5 \times 3) = 26 \times 10^5$
  - Clock Cycles( $P_2$ ) =  $(10^5 \times 2) + (2 \times 10^5 \times 2) + (5 \times 10^5 \times 2) + (2 \times 10^5 \times 2) = 20 \times 10^5$

3. Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler **A** results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 seconds, while compiler **B** results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 seconds.

- (a) **Find** the average CPI for each program given that the processor has a clock cycle time of 1 ns.  
 (b) Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, **how much faster** is the clock of the processor running compiler **A**'s code versus the clock of the processor running compiler **B**'s code?  
 (c) A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. **What** is the speedup of using this new compiler versus using compiler **A** or **B** on the original processor?

**Solution of Question #3:**

(a) The average CPI for each program:

- $CPI = \frac{T_{exec} \times f}{No.Instr}$
- Compiler A CPI =  $\frac{1.1 \times 10^9}{10^9} = 1.1$
- Compiler B CPI =  $\frac{1.5 \times 10^9}{1.2 \times 10^9} = 1.25$

(b) Clock speed of processor running compiler A relative to processor running compiler B:

- $\frac{f_B}{f_A} = \left( \frac{No.Instr(B) \times CPI(B)}{No.Instr(A) \times CPI(A)} \right) = 1.37$

(c) Speedup of using new compiler:

- $\frac{T_A}{T_{new}} = 1.67$
- $\frac{T_B}{T_{new}} = 2.27$

4. You have been recently recruited by a company to speed up their applications. Suppose you were given an application that consists of 50% floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions. The application is currently running on a desktop and you propose to use FPGAs to speedup their applications. The FPGA can be attached to the desktop where the bottlenecks are mapped into hardware. Assume the synchronization (communication) between the processor and the FPGA is negligible.

- (a) Management wants the application to run 2 times faster. You can make the divide run at most 5 times faster and the multiply run at most 8 times faster. **Can you** meet management's goal by making only one improvement, and which one?
- (b) If you make both the multiply and divide improvements, **what** is the speed of the improved machine relative to the original machine.

**Solution of Question #4:**

(a) No you cannot meet the management goal by making only one improvement, below is the proof:

- Speedup of Multiply Alone =  $\frac{1}{(1-0.5)+0.5/8} = \frac{1}{0.5+0.0625} = \frac{1}{0.5625} = 1.77$
- Speedup of Divide Alone =  $\frac{1}{(1-0.2)+0.2/5} = \frac{1}{0.8+0.04} = \frac{1}{0.84} = 1.1904$

(b) If we make both the multiply and divide improvements, then the speed of the improved machine relative to the original machine would be:

- Speedup (Multiply & Divide) =  $\frac{1}{(1-0.7)+0.5/8+0.2/5} = \frac{1}{0.3+0.0625+0.04} = \frac{1}{0.4025} = 2.48$
- Speedup with infinite number of resources =  $\frac{1}{(1-0.7)+0.7/\infty} = \frac{1}{0.3} = 3.33$