Lab 1: Logic Gates

ITI 1100 B - Digital Systems

Winter 2019

School of Electrical Engineering and Computer Science

University of Ottawa

Course Coordinator: Aziz Abdesselam

Teaching Assistants: Mitchell

Group: B2

Group Members:

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Objectives

- Construct simple combinational logic circuits from a schematic.
- Experimentally determine the functional operation of simple combinational logic circuits.
- Identify equivalent logic gates to those produced by various circuit configurations from the resulting truth table.
- Connect various gates together to create simple logic functions.
- Analyse combinational logic circuits and predict their operation.
- Construct and test more complex combinational logic circuits.

Equipment and components

- Quartus II 13.0 Service-Pack 1
- Altera DE2-115 card

Circuit Diagrams

Figure 1: Two chip logic circuit diagram (Figure 5.1.2 of Lab Manual)

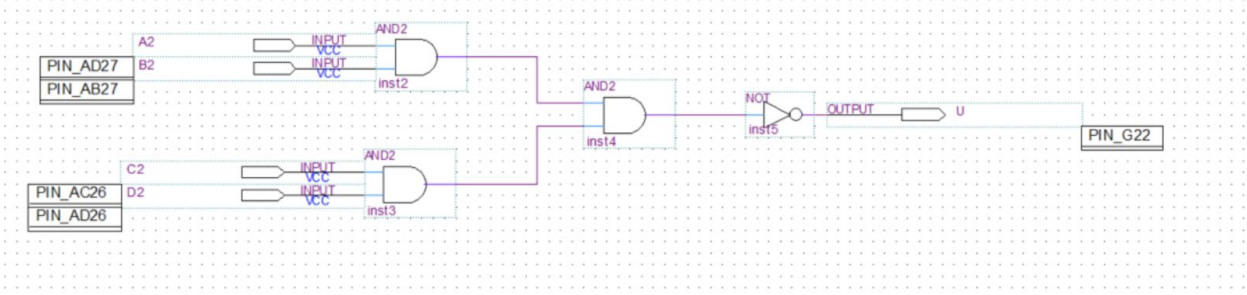


Figure 2: Three chip logic circuit diagram (Figure 5.1.3 of Lab Manual)

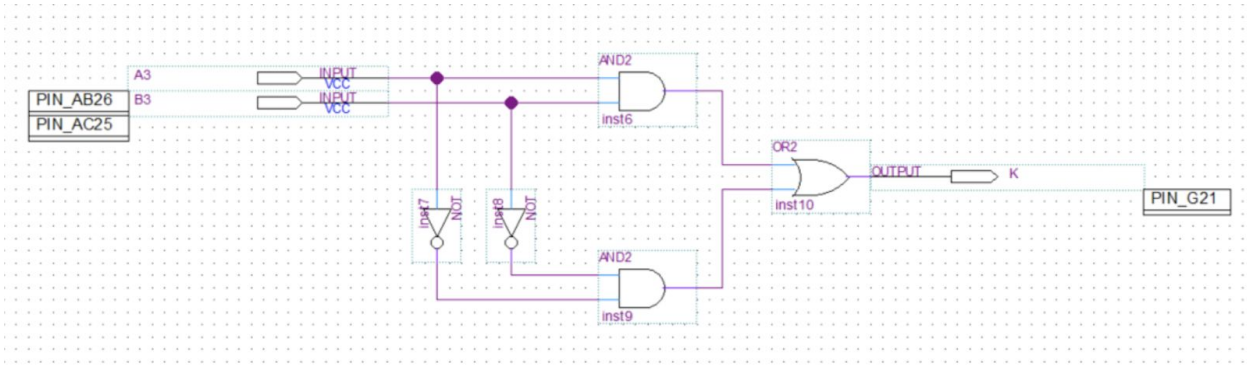


Figure 3: OR Circuit Diagram (5.1.7 from lab manual)

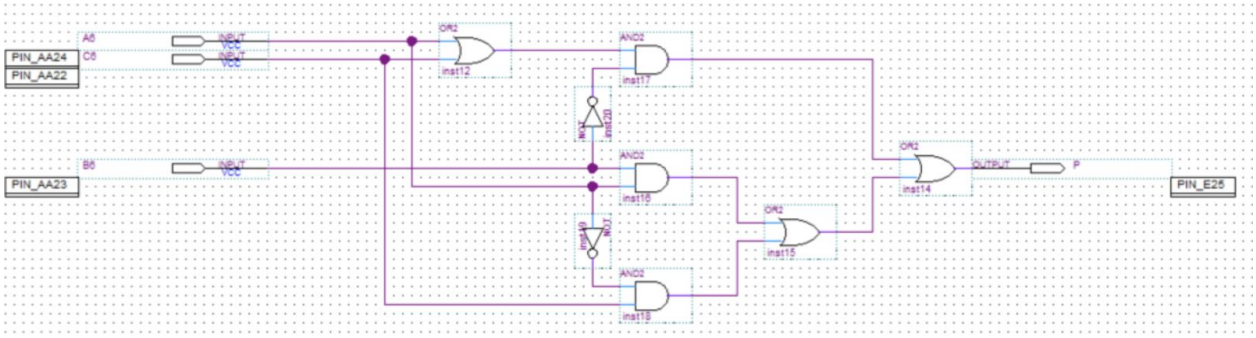
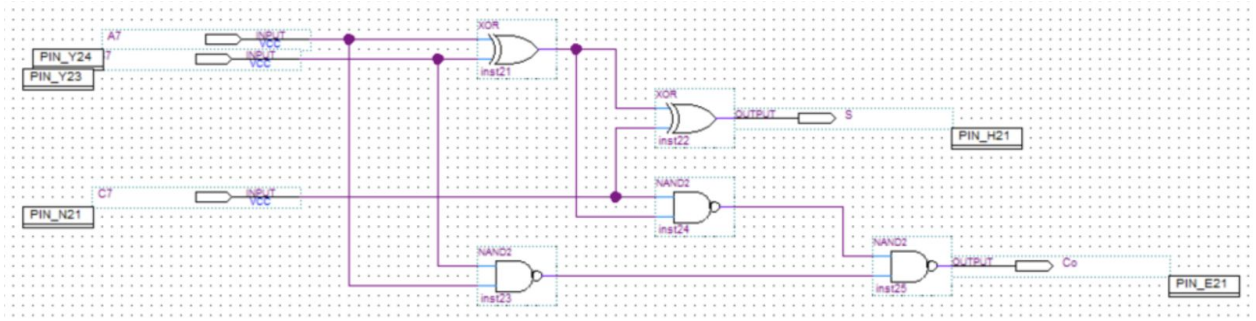


Figure 4: Multiple output circuit diagram (5.1.8 from lab manual)



Experimental Data and Data Processing

Two Chip Logic Circuit (5.1.2)

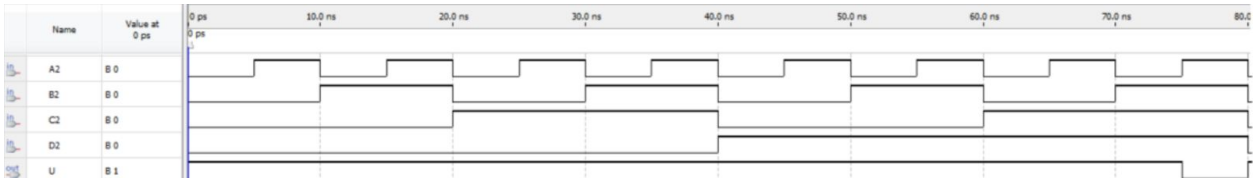


Figure 5: Simulation output of a two logic chip circuit

Three Chip Logic Circuit (5.1.3)

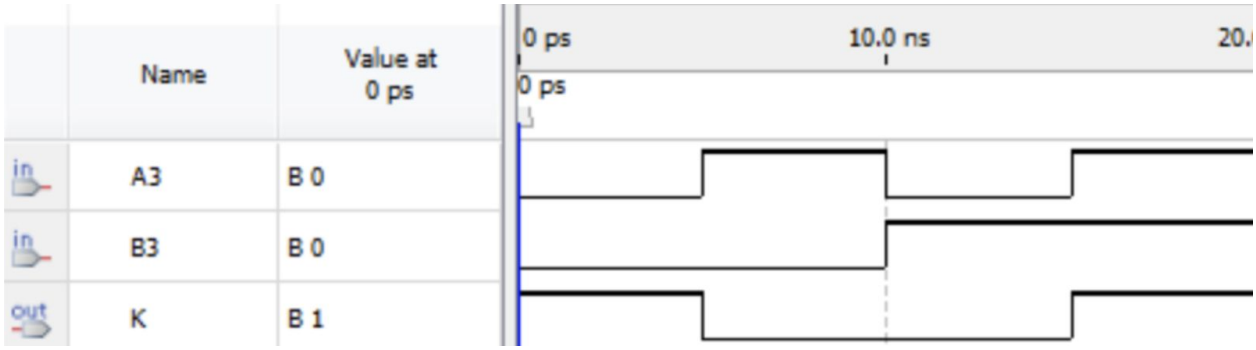


Figure 6: Simulation output of a three chip logic circuit

OR Circuit (5.1.7)

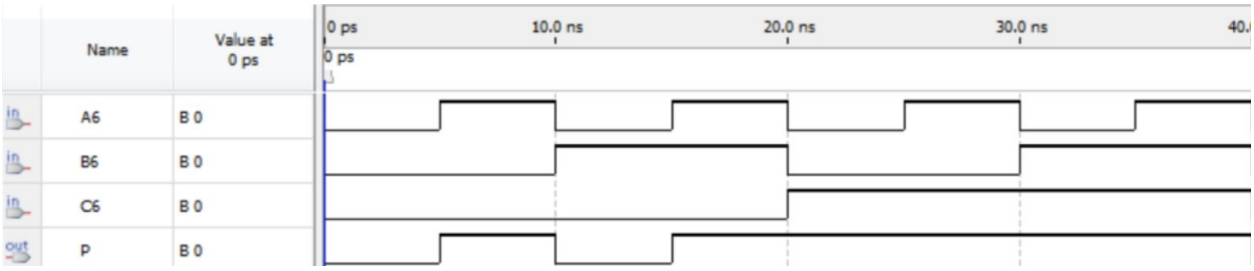


Figure 7: Simulation output of a OR circuit

Multiple Output Circuit (5.1.8)

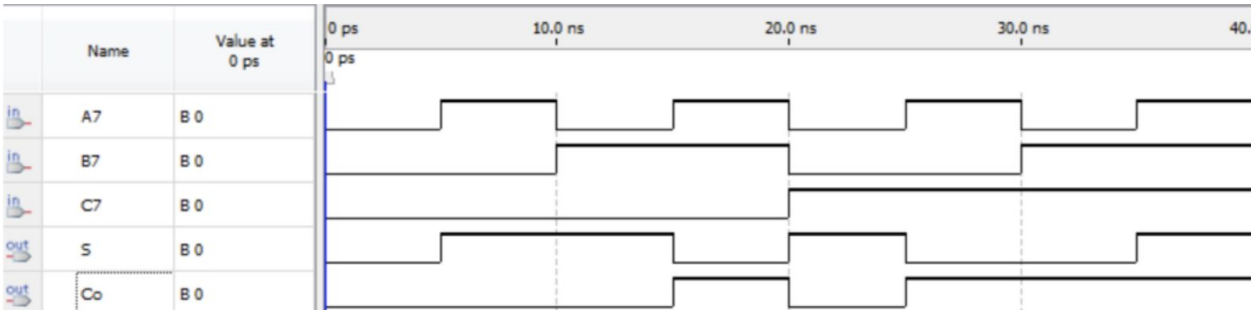


Figure 8: Simulation output of a multiple output circuit

Table 1: Data from Altera DE2-115 card

C7	B7	A7	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Comparison of Theoretical Data and Experimental Data

Table 2: Two Chip Logic Circuit (5.1.2)

A	B	C	D	Expected	Actual
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	1
1	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0

The expected results and the actual results were identical for circuit 5.1.2

Table 3: Three Chip Logic Circuit (5.1.3)

A	B	Expected	Actual
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

The expected results and the actual results were identical for circuit 5.1.3

Table 4: OR Circuit (5.1.7)

A	B	C	Expected	Actual
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

The expected results and the actual results were identical for circuit 5.1.7

Table 5: Multiple Output Circuit (5.1.8)

A	B	C	Expected Co	Expected S	Actual Co	Actual S
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	1	1	1

The expected results and the actual results were identical for circuit 5.1.8

Discussion & Conclusions

For this lab, four logic circuits were built and simulates on the Quartus II software. The circuits were created in a block diagram using different types of gates, and different numbers of inputs and outputs. Pins were assigned to the components in order to obtain the truth values of these circuits. For figure 5.1.8, the truth values were observed off the Altera card, while all four were simulated on the by using the simulation waves on Quartus.

The experimental data from the pre-lab was determined from truth tables and boolean algebra. The experimental truth values gathered from the pre-lab were all identical to the given outputs of each simulation of the circuits which was to be expected. For the Altera card, switches and buttons were assigned to their respective input pins and lights for the outputs pins in the Quartus software. The truth values were gathered by flipping the switches on the Altera card to see if the red lights would turn on or off. No major problems were faced during this experiment besides small human errors which were later corrected.

Appendix

Cameron Powers 3006632311
Hilary Johnson 3006699521

Lab 1 Pre Lab

5.1.1

$(A+B)+C$

A	B	C	(A+B)	(A+B)+C
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

5.1.2

$[(AB)(CD)]' = U$

A	B	C	D	U
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

5.1.3

$AB+(A'B') = K$

A	B	K
0	0	1
0	0	0
0	1	0
1	1	1

5.1.5

$A \oplus B = L$

A	B	L
0	0	0
0	1	1
1	0	1
1	1	0

5.1.7

$P = (A+C)B' + (BA+A'C)$

C	B	A	P
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

5.1.6

$V = C(DB+DB') = CD$

C	D	CD
0	0	0
0	1	0
1	0	0
1	1	1

5.1.8

$A'B'C + AB = C_0 \quad (A \oplus B)C = S$

A	B	C	S	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1