Lab 1 ITI1100

Digital Systems I (University of Ottawa)

Objectives:

The main objectives of this laboratory were:

- To build simple logic circuits using diagrams;
- To experimentally determine how the logic circuits that were built functioned;
- To identify common logic functions that were produced by various circuit configurations by their corresponding truth tables;
- To create simple logic functions using various logic gates;
- To analyse and predict the operations of combinational logic circuits;
- To construct and test more complex combinational logic circuits.

The sub- objectives of this laboratory was:

- To gain the required skills to use QUARTUS II to create logic circuits;

Throughout the laboratory, the validity of the various logic gates was being tested. They were tested to see if they functioned according to the rules learned in class. Another rule that was being verified was how the Altera UP-1 circuit board registers the input values.

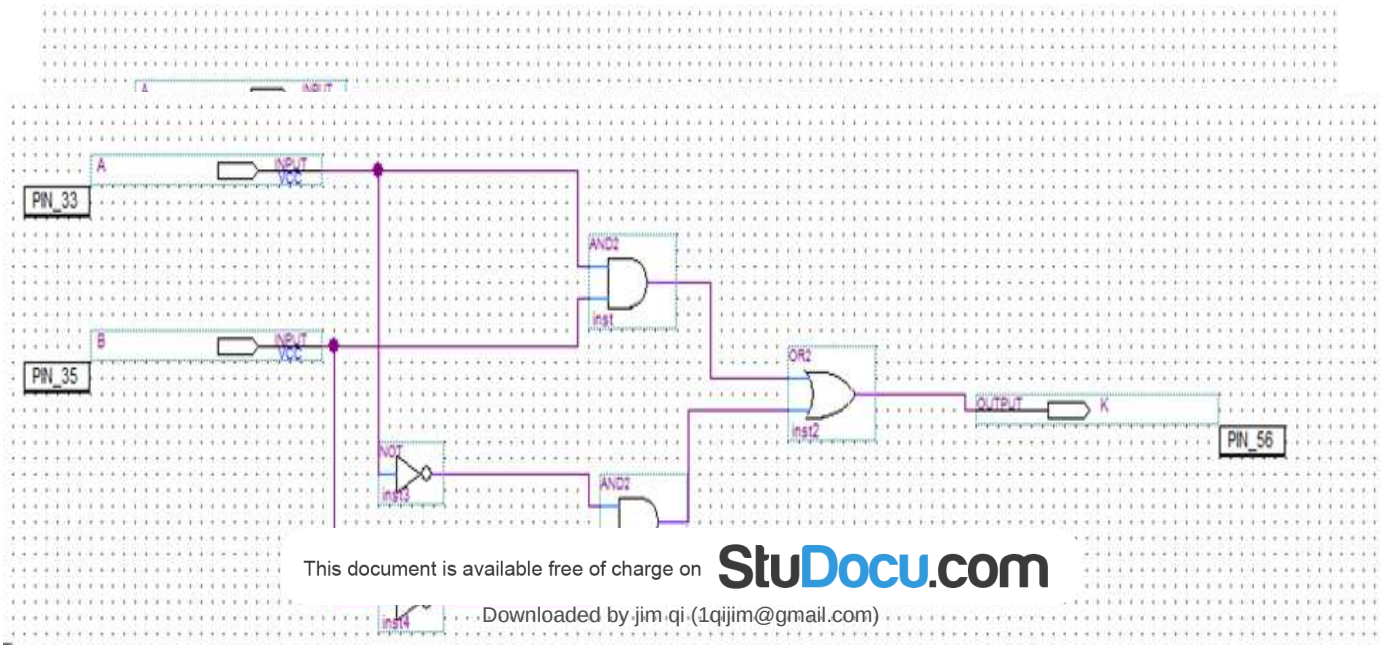
Equipment and Components Used:

- QUARTUS II Web Edition 9
- Altera UP-1 circuit board
- AC Adapter, minimum output: 9VDC, 250mA
- #22 Solid-core wires
- A Dell PC with Lenovo desktop screen

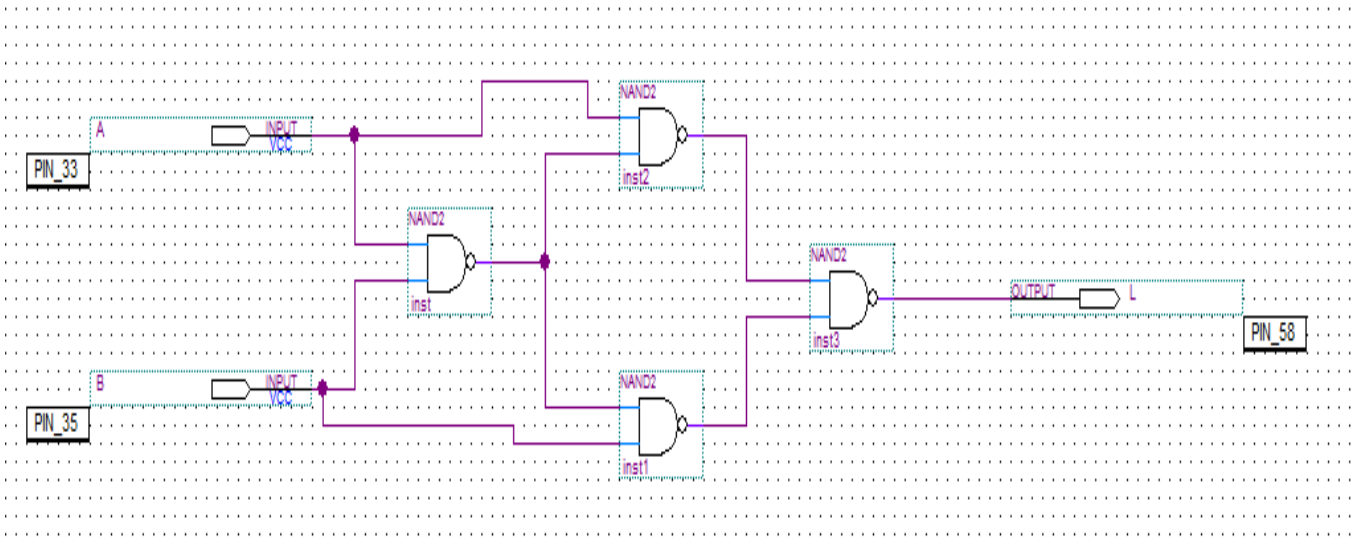
Circuit Diagrams:

The following diagrams are the schematic designs that were created during the lab, with the help of the QUARTUS design software:

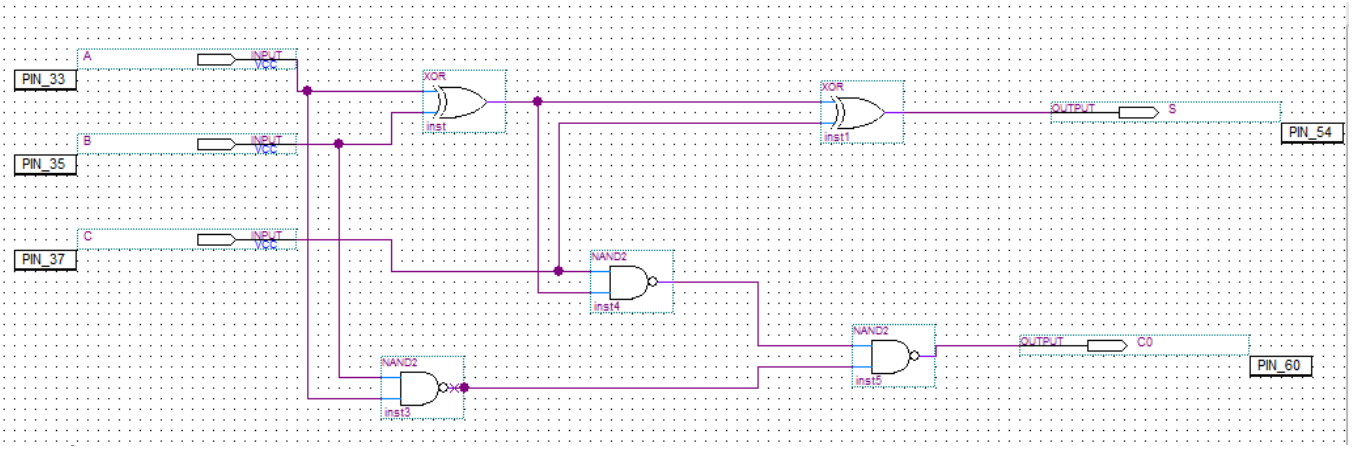
6.1.1 R = (A +B) +C



6.1.5 L = [(AB)'A] + [(AB)'B]



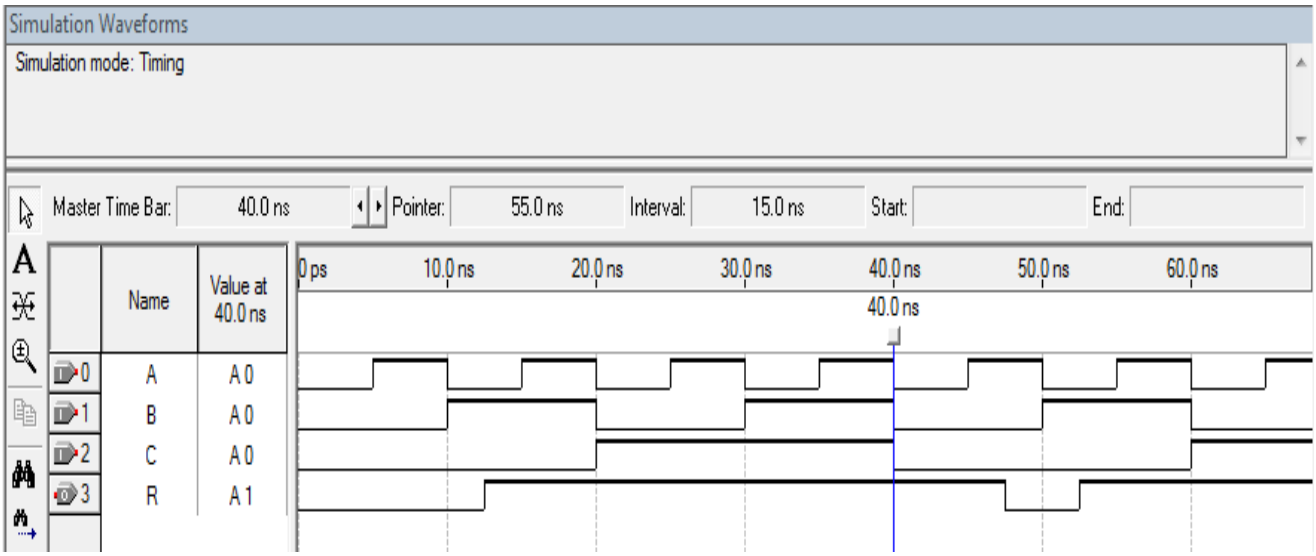
6.1.8 $S = (A \oplus B) \oplus C;\ C_o = (A \oplus B)C + (AB)$



The following diagrams are the simulation outputs and the truth tables that corresponded with schematic designs above. These were also created during the lab, with the help of the QUARTUS design software (for the simulation outputs):

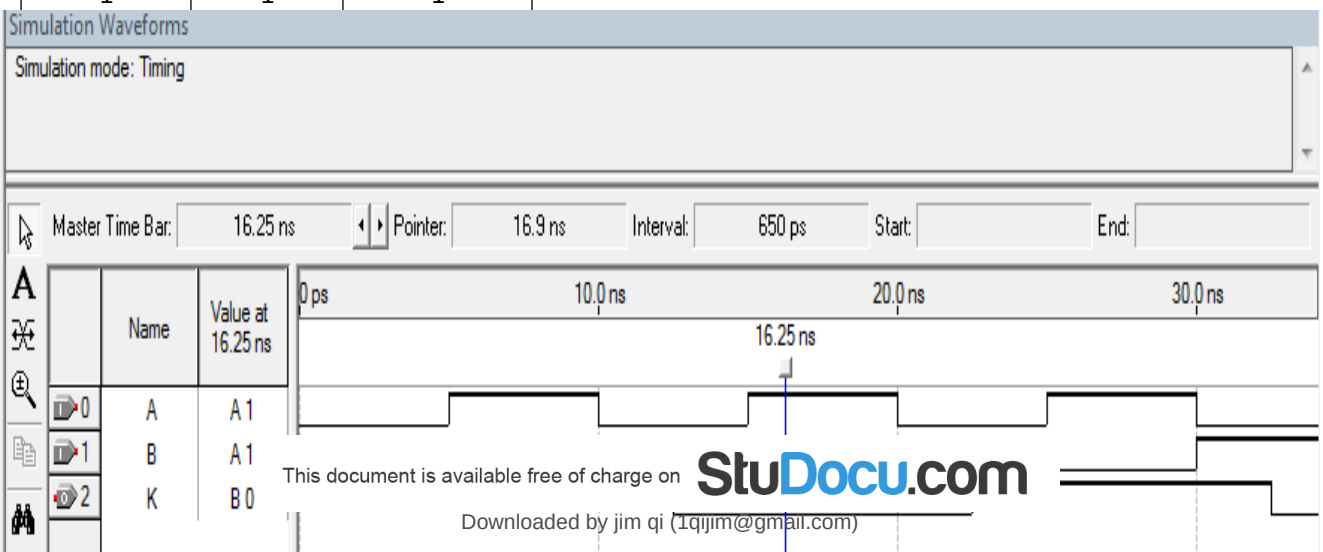
6.1.1 R = (A +B) +C

A	B	C	R
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	1
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0



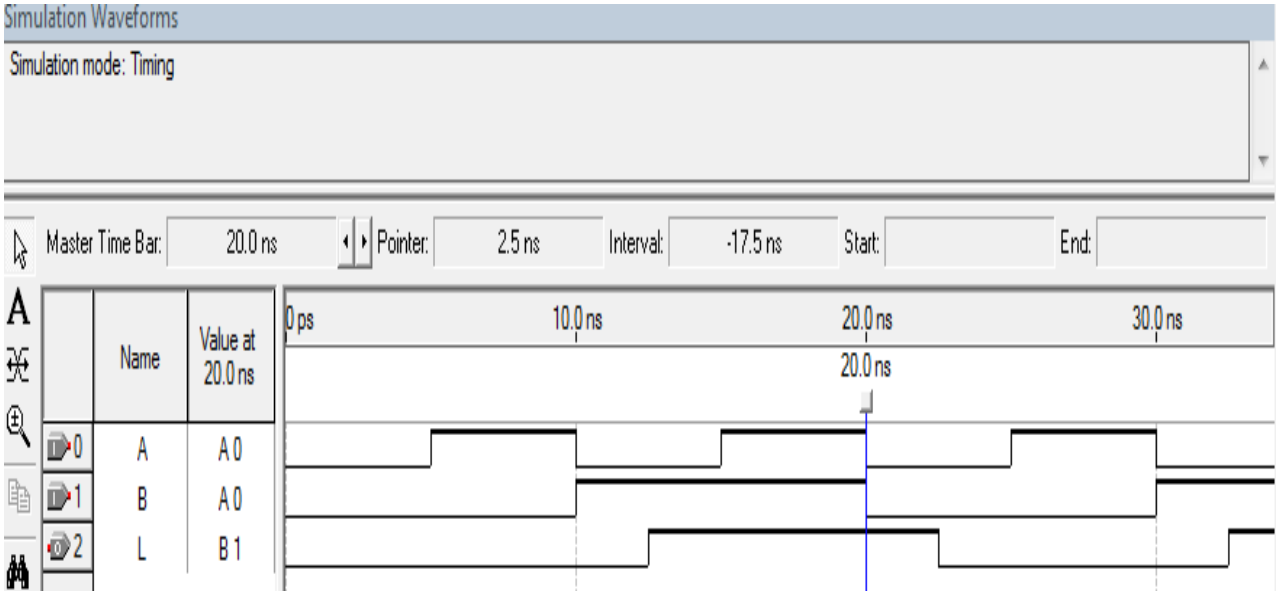
6.1.3 K = (AB) + (A'B')

A	B	K
1	1	1



6.1.5 L = [(AB)'A] + [(AB)'B]

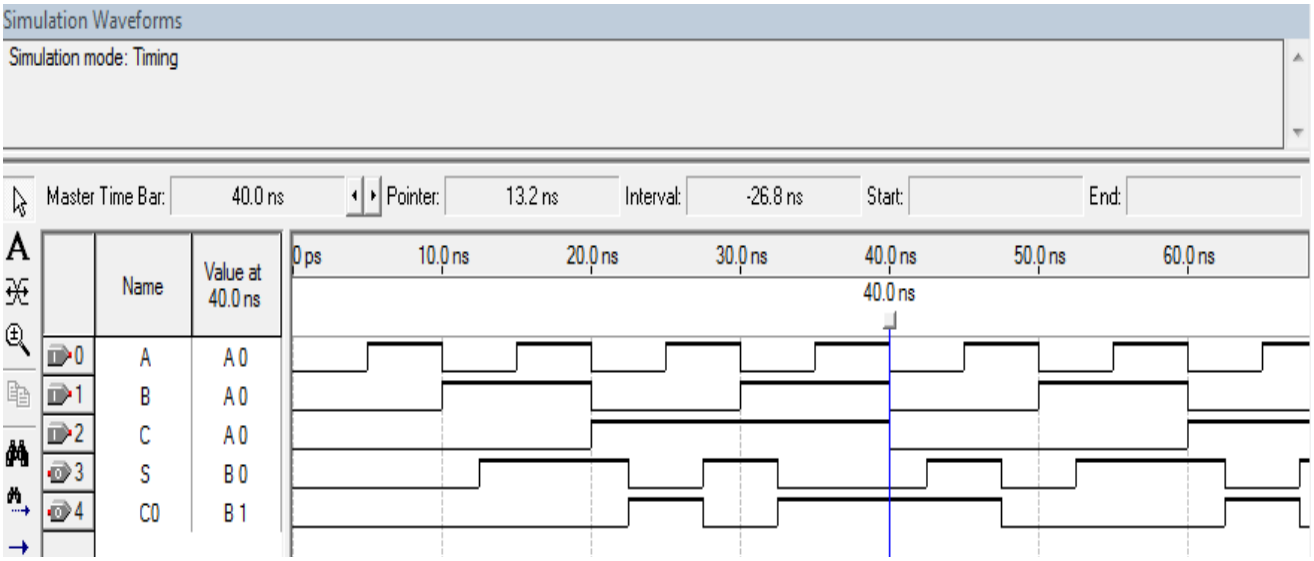
A	B	L
1	1	0
1	0	1
0	1	1
0	0	0



6.1.8 $S = (A \oplus B) \oplus C$

$C_o = (A \oplus B)C + (AB)$

A	B	C	S	C_0
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0



Comparison of Expected and Experimental Data:

The following truth tables represent the experimental data (on the left) and the expected data (on the right). They are being compared to see if the data collected matched the theoretical data. The data shows that both the experimental and the expected data matched for all circuits tested. The truth tables are:

6.1.1 R = (A +B) +C

Experimental

A	B	C	R
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	1
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0

Expected

A	B	C	R
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	1
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0

6.1.3 K = (AB) + (A'B')

Experimental

A	B	K
1	1	1
1	0	0
0	1	0
0	0	1

Expected

A	B	K
1	1	1
1	0	0
0	1	0
0	0	1

6.1.5 L = [(AB)'A] + [(AB)'B]

Experimental

A	B	L
1	1	0
1	0	1
0	1	1
0	0	0

Expected

A	B	L
1	1	0
1	0	1
0	1	1
0	0	0

6.1.8 $S = (A \oplus B) \oplus C$

$C_o = (A \oplus B)C + (AB)$

Experimental

A	B	C	S	C_0
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

Expected

A	B	C	S	C_0
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

Discussion and Conclusion:

During the experiment, there were many things that were taken note when it comes to the QUARTUS II software, the Altera UP-1 circuit board and the general procedure of the lab. One thing that was learned was how to operate, detect the results of the circuit board. When inputting the inputs into the circuit board, there were two options for its output. When the MAX7128's LED light flashed red, the output of the circuit board is false or 0. If there is no light, then the output is true or 1. While operating the MAX7128's DIP SPST switches, if the switch is up, it is equivalent to 1 or true. If the switch is pressed down than the input is false or 0.

As shown above, the experimental data and expected data are identical. This means that the logical circuits created were built correctly and gave the outputs that were predicted. Since the experimental results are identical to the expected results, it was found that the logic gates function as expected.

All the main objectives of the lab were met. The schematics were implemented in QUARTUS II and used to make the desired logic circuits. They were then tested to determine their functionality and their outputs were record and compared to the expected data. Some minor sources of that could have resulted in error during the lab were: Placing wires in the improper pin and forgetting to re-compile the project after every step in the procedure.

If the wire was not in its assigned pin on the circuit board, then the corresponding input value would not register, which would result in a set of data that did not reflect the circuit. Forgetting to compile after every step causes the downloaded circuit to potentially lack the necessary information to function as expected. For example, if one forgot to compile after assigning pins, then the uploaded circuit would not have any of the correct input or output values.