CEG2136 Computer Architecture I
CEG2536 Architecture des ordinateurs I

uOttawa

NAME / ID#

Quiz 1
Fall 2015

Even

Q1. The next figure shows the state diagram of a logic circuit which has a unique one-bit external input x. 25 points

1. Start off by deriving the state table of the circuit. Then, assuming that JK flip-flops are to be used in the implementation, extend the state table with the excitation table of the circuit.
2. Find simplified expressions for each flip-flop inputs.

SOLUTION:

1. 13 points Map the FSM logic diagram to State table.

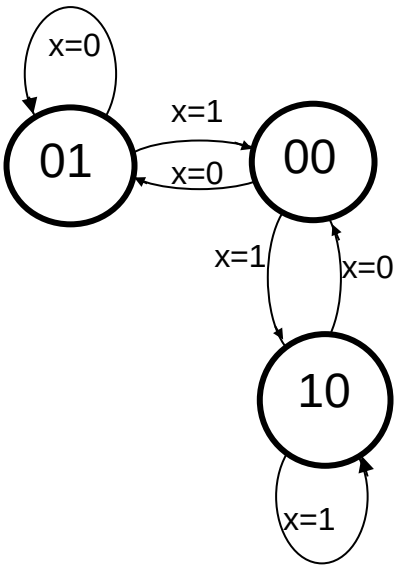
To find the excitation table, fill the J and K columns using:

A) the "copy & paste recipe:"

[1] J = next state if **present state is 0**
[2] J = don't care (x) if ***present state is 1***
[3] K = don't care (x) if **present state is 0**
[4] K = complement of the next state if present state is 1

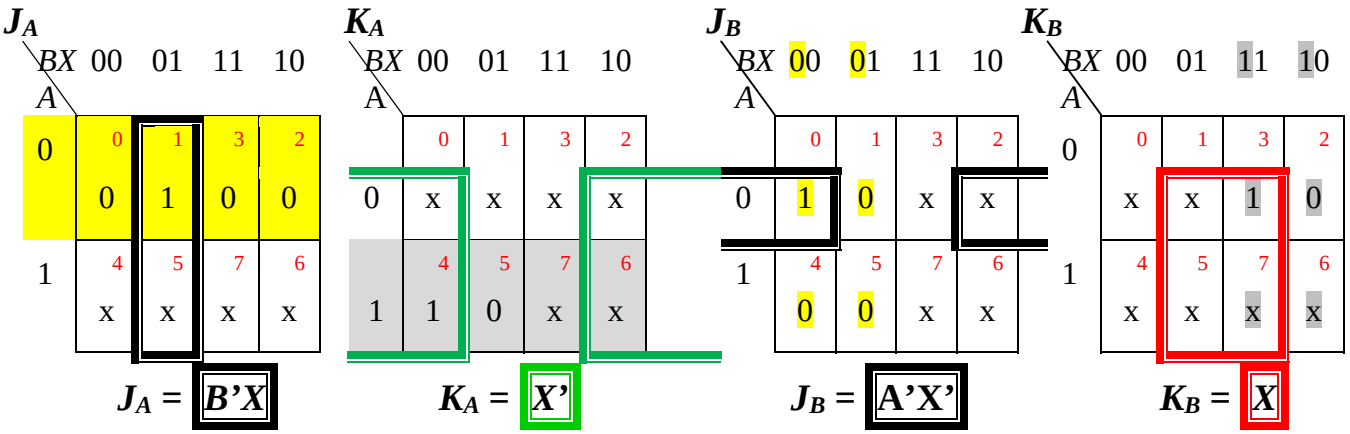
… or B) The JK FF Excitation Table, i.e.:

	if $Q^n = 0$	if $Q^n = 1$
J =	[1] Q^{n+1}	[2] x
K =	[3] x	[4] $(Q^{n+1})'$



	A^n	B^n	X	A^{n+1}	B^{n+1}	J_A	K_A	J_B	K_B
(0)	0	0	0	0	1	0	×	1	×
(1)	0	0	1	1	0	1	×	0	×
(2)	0	1	0	0	1	0	×	×	0
(3)	0	1	1	0	0	0	×	×	1
(4)	1	0	0	0	0	×	1	0	×
(5)	1	0	1	1	0	×	0	0	×
(6)	1	1	0	×	×	×	×	×	×
(7)	1	1	1	×	×	×	×	×	×

2. 12 points Find simplified expressions for each flip-flop inputs



OR

$J_1 = X\,Q_0'$

$Q_1\,Q_0$ / X	00	01	11	10
0	0	0	x	x
1	1	0	x	x

$K_1 = X'$

$Q_1\,Q_0$ / X	00	01	11	10
0	x	x	x	1
1	x	x	x	0

$J_0 = X'\,Q_1'$

$Q_1\,Q_0$ / X	00	01	11	10
0	1	x	x	0
1	0	x	x	0

$K_0 = X$

$Q_1\,Q_0$ / X	00	01	11	10
0	x	0	x	x
1	x	1	x	x

P2. 25 points Design a 3-bit shift right register which has a data input *Serial In* and a control input "*Sh*" (shift). The operation of the sequential circuit is described in the functional Table 1. Design the sequential circuit using three D flip-flops.

(P2.1.) 6 pts Provide the *equations for the next state variables* of the D flip-flops $\{Q_i^{n+1},\ i = [0, 1, 2]\}$

(P2.2.) 13 pts Draw the logic diagram of the circuit that you designed; explain your work.

(P2.3.) 6 pts Design a D flip-flop using a T flip-flop; draw the logic diagram of your designed D FF.

(P2.4.)

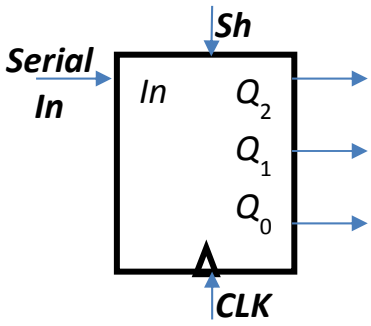
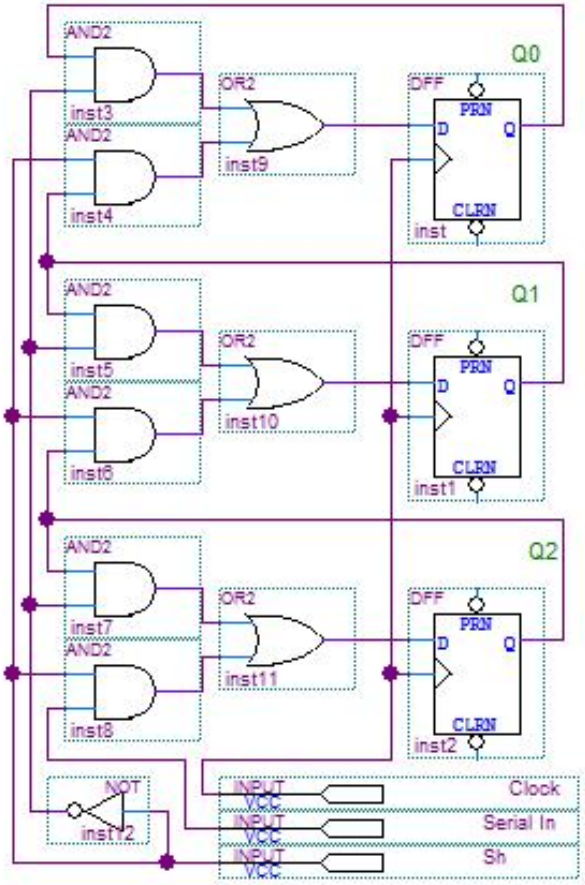


Table 1.

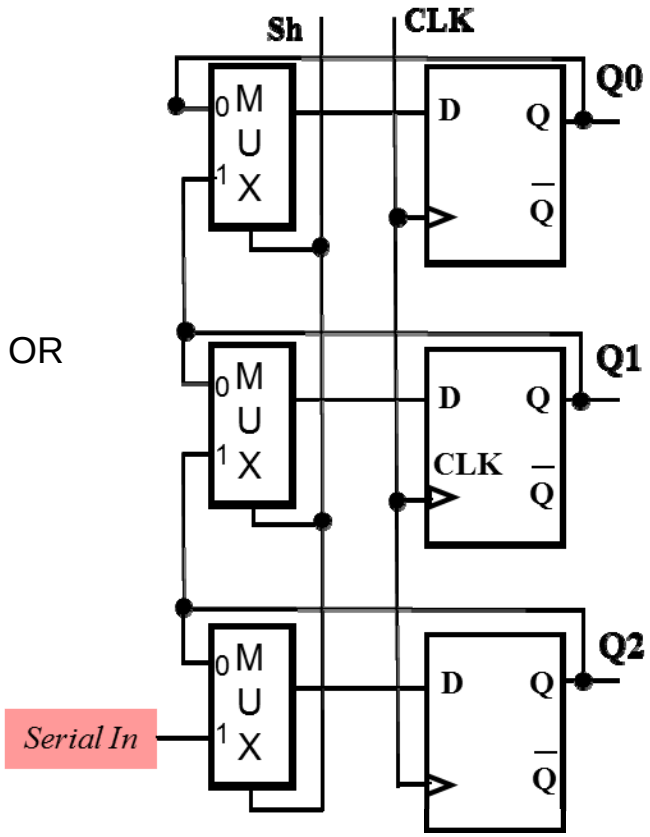
Sh	**Function**	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	*Preserve* (hold) present *state*	Q_2^n	Q_1^n	Q_0^n
1	*Shift Right*	***Serial In***	Q_2^n	Q_1^n

$$Q_2^{n+1} = Sh'\,Q_2^n + Sh \cdot Serial\ In$$
$$Q_1^{n+1} = Sh'\,Q_1^n + Sh \cdot Q_2^n$$
$$Q_0^{n+1} = Sh'\,Q_0^n + Sh \cdot Q_1^n$$

(P2.2.) Draw the logic diagram of the circuit that you designed. 13 pts



OR



(P2.3) 6 pts Design a D flip-flop using a T flip-flop; draw the logic diagram of your designed D FF

Q^n	D	Q^{n+1}	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

$$T = \overline{Q^n} \cdot D + Q^n \cdot \overline{D}$$

$$T = Q^n \oplus D$$