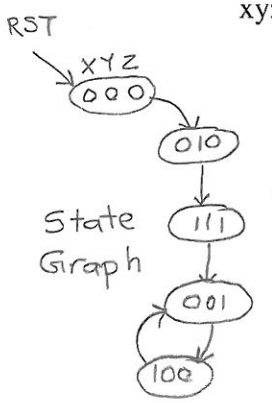
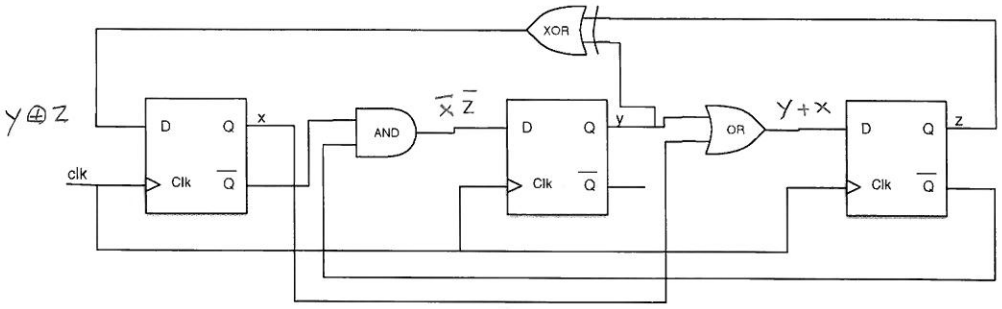
ELEC 2607 ('18) **Assignment 3** 30 Marks

1. Plot the timing diagram for the following circuit for 6 clk cycles. Assume that initially xyz=000. Plot the clk, x, y, and z signals. 6 marks

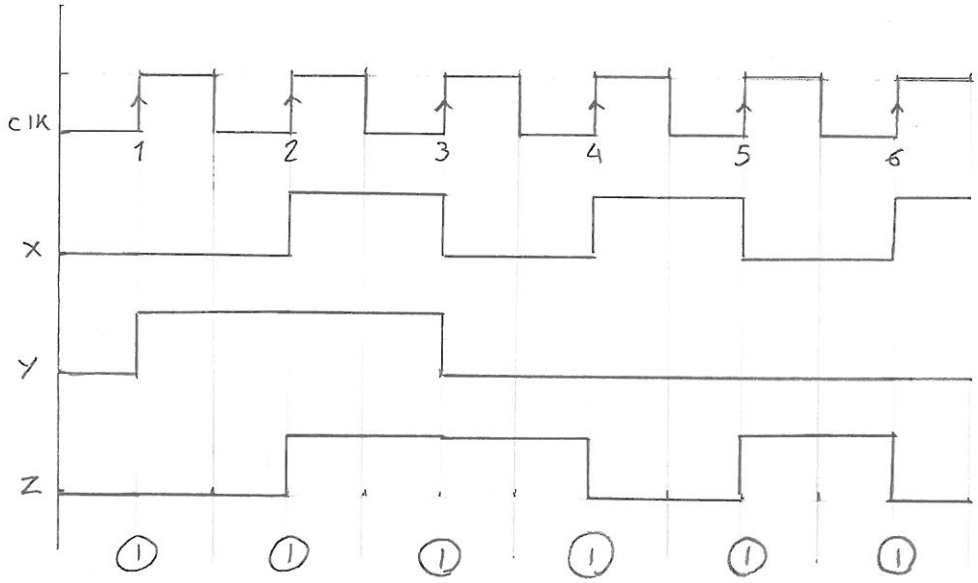




$x^+ = y \oplus z$

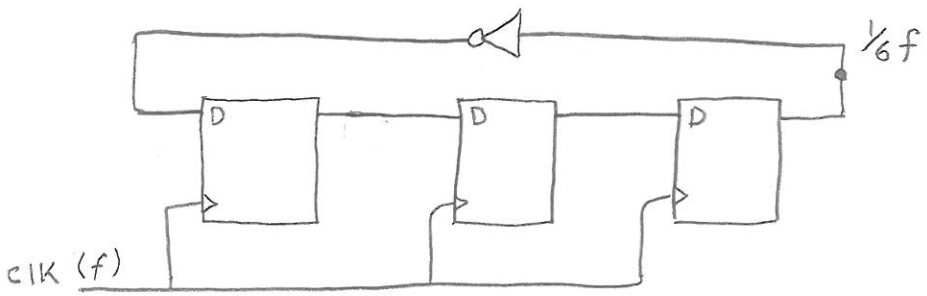
$y^+ = \bar{x}\,\bar{z}$

$z^+ = y + x$



clk edge	x	y	z	
	0	0	0	→ start
1	0	1	0	
2	1	1	1	
3	0	0	1	
4	1	0	0	
5	0	0	1	
6	1	0	0	

2. Design a circuit made of rising-edge-triggered flip-flops and inverter(s) such that its output has one-sixth (1/6) of the clock frequency. Verify your design by a timing diagram. The timing diagram should include the clk signal and the outputs of the flip-flops and logic gates. 3 marks



3. Design a circuit that outputs prime numbers between 0 and 10 in ascending order and repeats. Try to use the minimum number of flip-flops possible in your design. Show your state-graph, state-table, next-state and output equations, and the final circuit. 7 marks

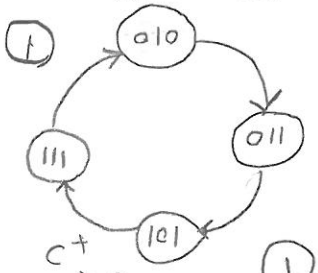
prime numbers: 2, 3, 5, 7

⇒ we need 4 states

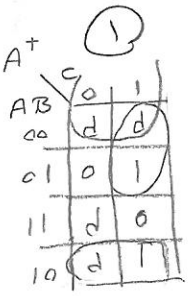
(1)

state ABC	next state A^+ B^+ C^+
0 0 0	d d d
0 0 1	d d d
0 1 1	1 0 1
0 1 0	0 1 1
1 0 0	d d d
1 0 1	1 1 1
1 1 1	0 1 0
1 1 0	d d d

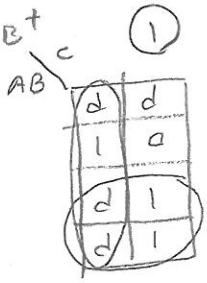
ABC = $Q_2 Q_1 Q_0$



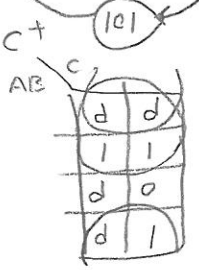
(1)



(1)



(1)



(1)

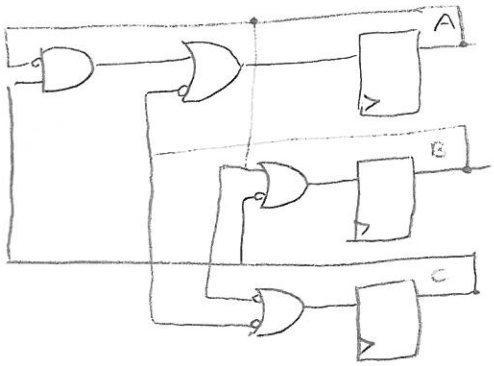
$A^+ = \bar{B} + \bar{A}C$

$B^+ = \bar{C} + A$

$C^+ = \bar{\bar{A}} + \bar{B}$

(1)

uses 3 FlipFlops + 4 logic gates



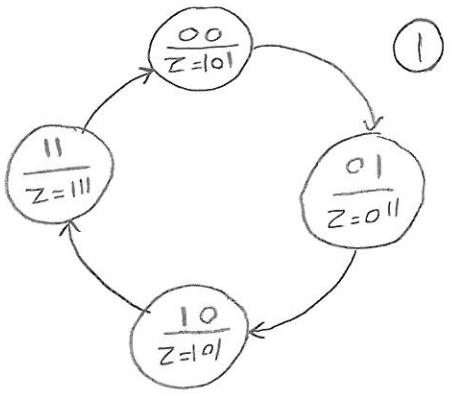
(1)

Q3. Alternative Solution

In the previouse solution the state variables of the FSM were the outputs of the counter as well. Here, we assume that the outputs are produced by the state variables.

(1)

State $Q_1 Q_0$	Next state $Q_1^+ Q_0^+$	output $Z_2 Z_1 Z_0$
0 0	0 1	0 1 0
0 1	1 0	0 1 1
1 0	1 1	1 0 1
1 1	0 0	1 1 1

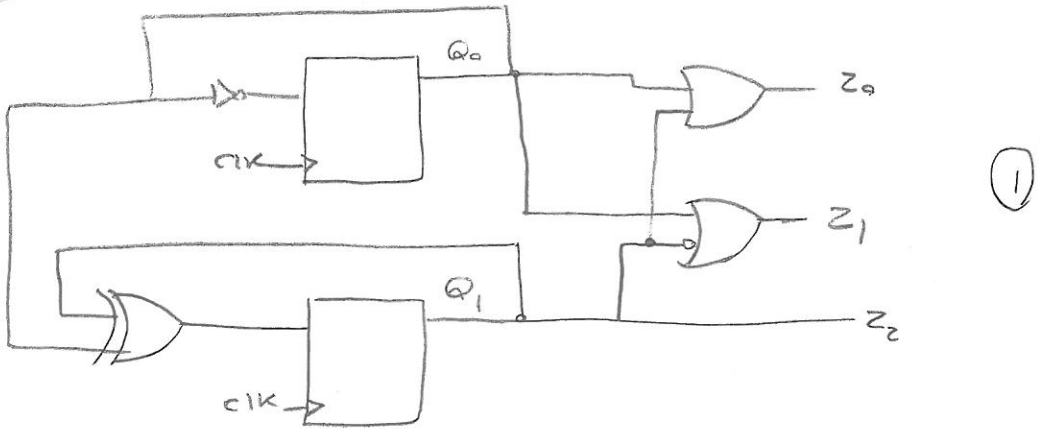


(1)

(1) (1) (1)

$Q_0^+ = \overline{Q_0}$ $Q_1^+ = Q_1 \oplus Q_0$ $Z_0 = Q_1 + Q_0$ $Z_1 = \overline{Q_1} + Q_0$ $Z_2 = Q_1$

(1)



(1)

uses 2 Flipflops + 3 Logic gates

This is more efficient.

4. Design and draw the state-graph of an FSM that detects the input sequence '11011' including overlaps. The sequence appears at the input from left to right. Suggest two different designs and compare them by listing the advantage and disadvantage of each. For both designs provide a state diagram, state-table, K-Maps, equations, and the circuit. 14 marks

See the solution on next pages

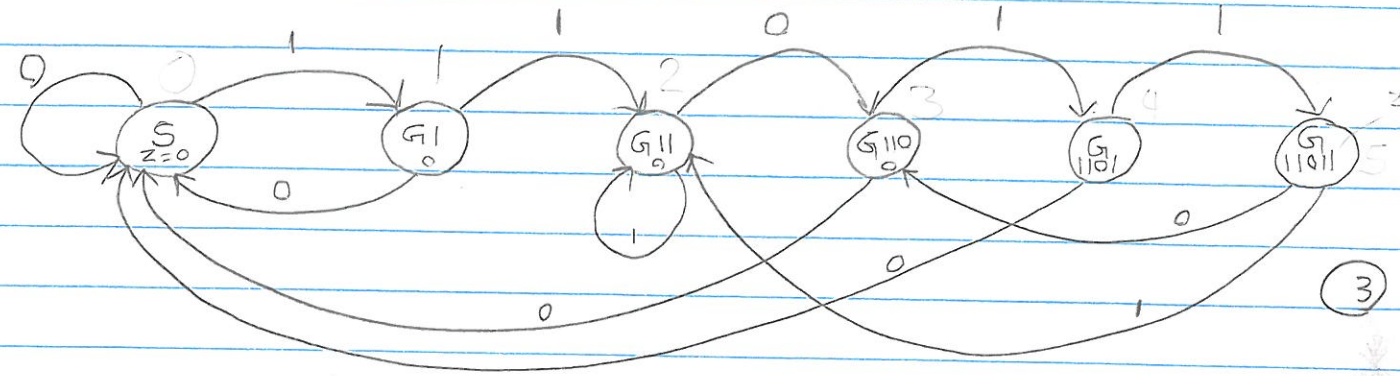
- Comparison

criteria	Moore	Mealy
# of gates	12	9
# of F/F	3	3
output glitch	no	Yes
short pulses	no	Yes
response	slower	faster

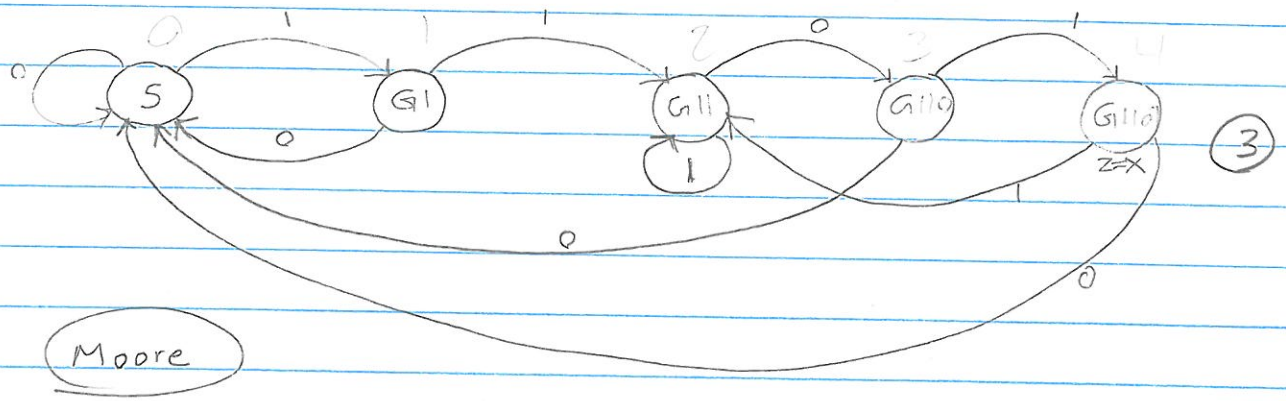
Mealy circuit design is more efficient / faster but less reliable. (2)

Q4.

Moore FSM Graph ↓



Mealy FSM Graph ↓



Moore

	X=0		X=1		
$Q_2Q_1Q_0$	$D_2D_1D_0$		$D_2D_1D_0$		Z
000	000		001		0
001	000		010		0
011	000		100		0
010	011		010		0
100	000		101		0
101	011		010		1
111	d d d		d d d		d
110	d d d		d d d		d

2

½ For each K-map

D_0

Q_1Q_0 \ Q_2X	00	01	11	10
00	0	1	1	0
01	0	0	0	1
11	0	0	d	d
10	1	0	d	d

$D_0 = \bar{Q}_1\bar{Q}_0X + Q_2\bar{X}Q_0 + Q_1\bar{Q}_0\bar{X}$

D_1

Q_1Q_0 \ Q_2X	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	0	0	d	d
10	1	1	d	d

$D_1 = \bar{Q}_1Q_0X + Q_0Q_2 + Q_1\bar{Q}_0$

D_2

Q_1Q_0 \ Q_2X	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	0	1	1	d
10	0	0	d	d

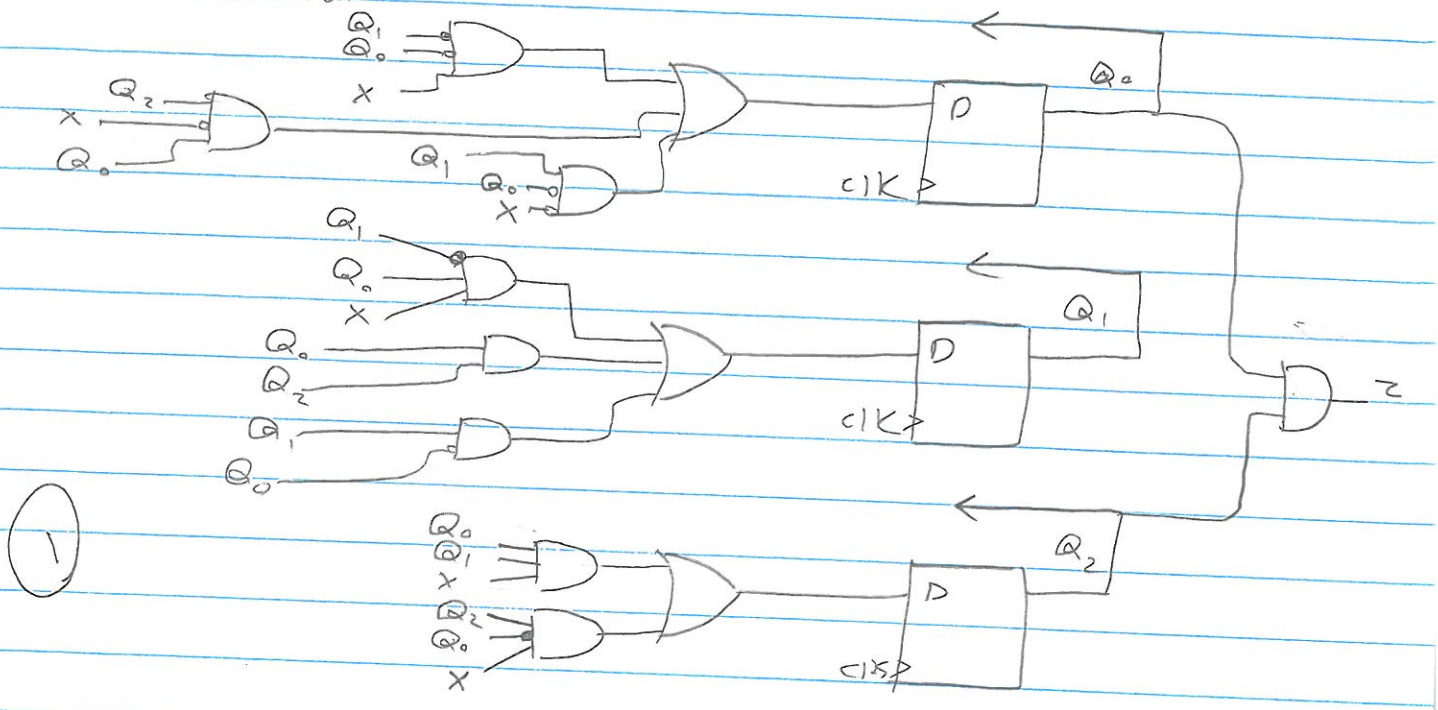
$D_2 = Q_1Q_0X + \bar{Q}_0Q_2X$

Z

Q_1Q_0 \ Q_2	0	1
00	0	0
01	0	1
11	0	d
10	0	d

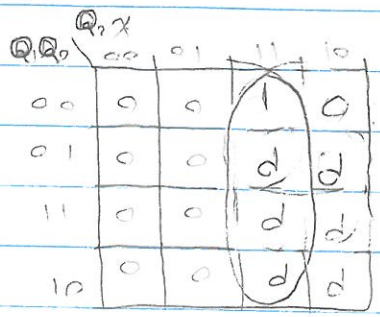
$Z = Q_2Q_0$

Moore Circuit

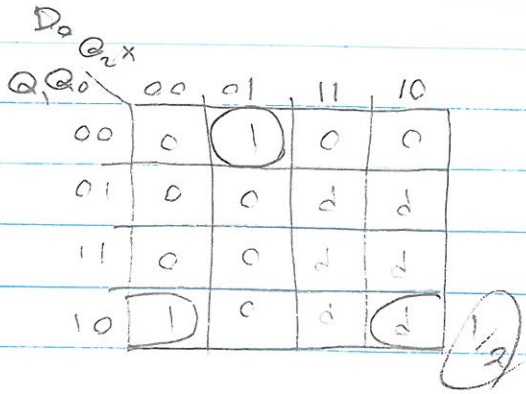


Mealy

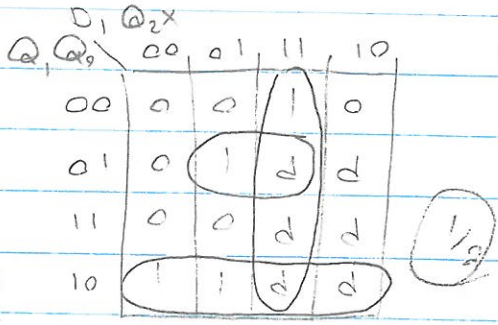
State $Q_2 Q_1 Q_0$	next state $X=0$ $D_2 D_1 D_0$	next state $X=1$ $D_2 D_1 D_0$	output $X=0$ Z	output $X=1$ Z
0 0 0	0 0 0	0 0 1	0	0
0 0 1	0 0 0	0 1 0	0	0
0 1 1	0 0 0	1 0 0	0	0
0 1 0	0 1 1	0 1 0	0	0
1 0 0	0 0 0	0 1 0	0	1
1 0 1	d d d	d d d	d	d
1 1 1	d d d	d d d	d	d
1 1 0	d d d	d d d	d	d



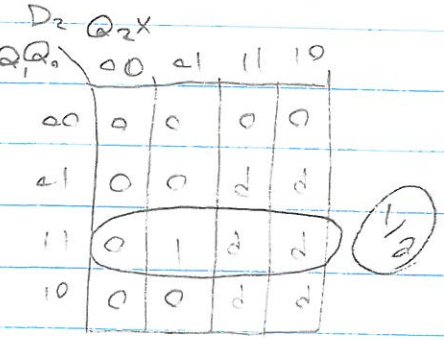
$Z = Q_2 X$ (1/2)



(1/2)



(1/2)

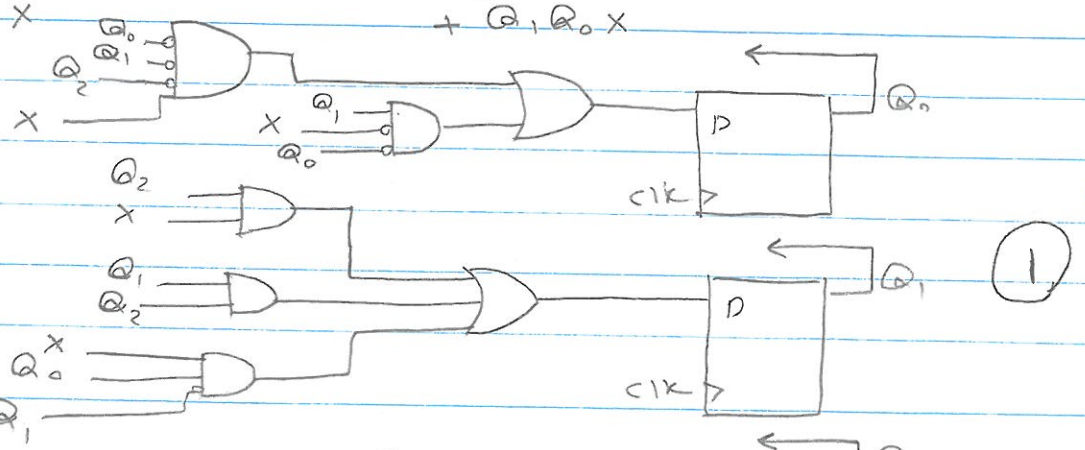


(1/2)

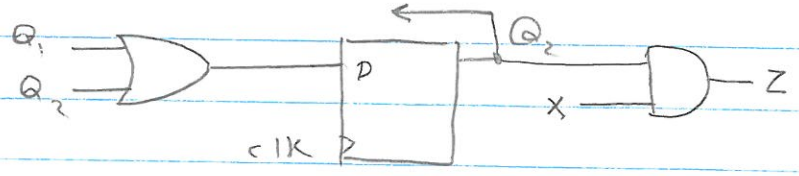
$D_0 = \bar{Q}_1 \bar{Q}_0 \bar{Q}_2 X + Q_1 \bar{Q}_0 \bar{X}$

$D_1 = Q_2 X + Q_1 Q_0 + \bar{Q}_1 Q_0 X$

$D_2 = Q_1 Q_2$



(1)



Mealy Circuit