Université d'Ottawa
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uOttawa
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University of Ottawa
Faculty of Engineering

School of Information
Technology and Engineering

ITI11001X-Digital Systems I (Summer 2008)

Student Name (Please print)_____

Student Number_____

Examiner: Abdul Al-Dhaher

Date: July 18, 2008
Time: 3 hours

Instructions:

- Answer ALL questions.
- This is a close-book examination, no lecture notes or book is allowed. Calculator is allowed
- Use the provided space to answer the following questions. If more space is needed, use the back of the page.
- Show all your calculations to obtain full marks.
- Calculators are allowed.

Question #	Mark
1	
2	
2	
4	
5	

Total	

Question 1 (15 marks)
Part A (5 marks)
Given on the following unsigned numbers:

A = 125
B = 1800

(i) Use 9's complement to perform:

A - B

B – A

(ii) Use 10's complement to perform

A - B
B – A

Question 1 Part B (10 marks)

Given $A = (12.5)_8$ and $B = (2.5)_{16}$. Convert these numbers into Binary use necessary number of bits and perform the following operations:

(i) Use 1's complement to perform the following operation

A – B

B – A

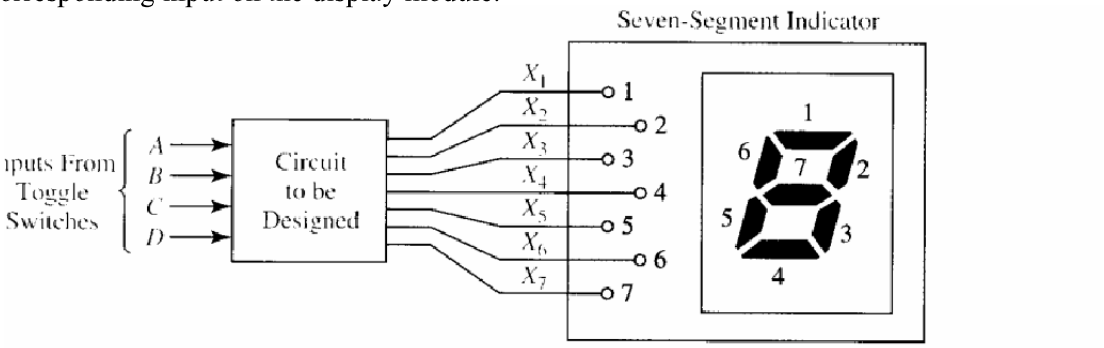
(ii) Use 2's complement to perform the following operation

A – B

B – A

Question 2: (20 marks)

The seven-segment indicator (shown in the figure) can be used to display any of the decimal digits 0 through 9. For example "1" is displayed by lighting segment 2 and 3 and "8" by lighting all seven segments. A segment is lighted when logic 1 is applied to the corresponding input on the display module.



Design an excess-3 code convertor to derive a seven segment indicator. The four inputs to the converter circuit (A, B, C, D in the figure) represent an execess-3 coded decimal digit. Assume that only input combination representing the digit 0 through 9 can occur as inputs, so the six unused combinations are don't cares. Design your circuit using only 2-, 3- and 4-input NAND gates and inverter. Try to minimize the number of gates and inverter required. The variables A, B, C and D are available from toggle switches.

Use 6 (not b) for 6. Use 9 (not q) for 9.

Question 3 (15 marks)

Question 3 part A (8 marks):
Realize (develop) the circuit for full adder using 3-to-8 line decoder with:

(a) Two OR gates
(b) Two NOR gates

(i) Write the truth table
(ii) Write the simplified (using K-map) expression for the outputs
(iii) Draw the circuits

Question 3 part B (7 marks):
Derive the logic equations for a 4-to-2 priority encoder. Write the truth table first and show the highest and lowest priority inputs. Use K-map to simplify the expressions.

Question 4 (15 marks)

Design a sequential circuit with two JK flip-flops A and B and two inputs E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.

(i) Give a table that shows:
   a. the input values
   b. the states (present and next) for the JK flip-flops
   c. the JK flip-flop inputs

(ii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the JK flip-flops.

(iii) Draw the circuit

Question 5 (35 marks)

Question 5 Part A (15 marks):

Design asynchronous (ripple) counter, up count counter, with a modulo-13 using D flip-flop:

(i) Build the state diagram
(ii) Draw the logic circuit

Question 5 Part B (20 marks):
Design synchronize downward decade counter which counts in the sequence:

0000, 1001, 1000, 0111, 0110, 0101, 0100, 0011, 0010, 0001, 0000, 1001 and repeat.

Use J-K flip-flops

i. Show the state table together with the inputs to the JK flip-flops
ii. Write the simplified logic expression for the inputs to the flip-flops
iii. Draw the state diagram
iv. Draw the circuit
v. Draw complete state diagram for the counter showing what happen when the counter is started in each of the unused states.