Question	Max Marks	Score
1	10	
2	20	
3	25	
4	25	
5	20	
Total	100	

CARLETON UNIVERSITY

FINAL
EXAMINATION
April 17, 2007

Duration: 3 hours

Department name and course number: Electronics ELEC-2507 (A,B,C)

Course Instructor(s): Q-J Zhang, A. Steele, M. Shams Number of students: 130

AUTHORIZED MEMORANDA:

NON-PROGRAMMABLE CALCULATOR

Students MUST count the number of pages in this examination paper before beginning to write, and report any discrepancies immediately to a proctor. **This question paper has 20 pages**.

This examination question paper MAY NOT be taken from the examination room.

This exam consists of 5 questions, which should be answered on this exam paper in the space provided. Attempt all questions. Marks allocated to each question are indicated (total marks = 100).

Note: The solution must be clearly indicated. Multiple solutions or solutions that are not clearly identified, will be marked incorrect. Using approximate relations (unless they are given below or specified in a question) is not accepted. Clearly state all assumptions made. **Clearly mark the units for all final answers**. **Clearly indicate axis/units for any graphs**. **SHOW YOUR WORK!**

Diode:

Forward current: $I_D \approx I_S\left(e^{V_D/nV_T}\right)$

Small signal resistance: $r_d = \dfrac{nV_T}{I_D}$

$V_T = \dfrac{kT}{q} = 25\,mV$ at room temperature

Bipolar Transistor:

Active mode operation: $V_{BE} = 0.7V$

Saturation mode operation: $V_{CEsat} = 0.2V$

$i_C = \beta i_B \quad i_C = \alpha i_E \quad i_E = i_B + i_C$

$g_m = \dfrac{I_C}{V_T} \quad r_\pi = \dfrac{\beta}{g_m} \quad r_o = \dfrac{V_A}{I_C}$

$r_e = \dfrac{\alpha}{g_m} = \dfrac{r_\pi}{\beta+1} \quad \alpha = \dfrac{\beta}{\beta+1}$

Operational Amplifier:

$V_o = A(V_+ - V_-)$; $R_i = \infty$; $R_o = 0$

MOSFET:

$\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m, $g_m = 2 I_D / V_{ov}$;

$I_{DS} = k'\dfrac{W}{L}\left[(V_{GS}-V_t)V_{DS} - \dfrac{V_{DS}^2}{2}\right]$;

$I_{DS,sat} = k'\dfrac{W}{L}\dfrac{(V_{GS}-V_t)^2}{2}(1+\lambda V_{DS})$;

$k' = \mu C_{ox}$; $K = k'\dfrac{W}{L}$

$V_{OV} = V_{GS} - V_t$

$g_{mb} = \chi g_m$

$g_m = k'\dfrac{W}{L}(V_{GS}-V_t) = \sqrt{2k'\dfrac{W}{L}I_{DS}}$

$r_{DS,triode} = \left[k'\dfrac{W}{L}(V_{GS}-V_t)\right]^{-1}$; $r_o = \dfrac{V_A}{I_D}$

Q1: Answer the following by filling in the corresponding circles with your selection *a, b, c or d*

(10 marks).

i. Assuming the diodes are ideal, what are the voltage V and the current I for the circuit shown in Fig. 1.1?

a) V= -1 V, I = 2 mA
b) V= -1 V, I = 1 mA
c) V= 1 V, I= 2 mA
d) V= 1 V, I= 1 mA

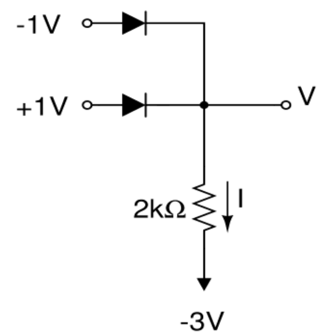


Fig. 1.1. See question 1 i.

ii. D1, in Fig. 1.2, is a 1N5234, which is a silicon zener diode with a V_z = 6.2V. What is the best estimate of the voltage V_o?

a) 6.2 V
b) 0 V
c) 5.5V
d) 5 V

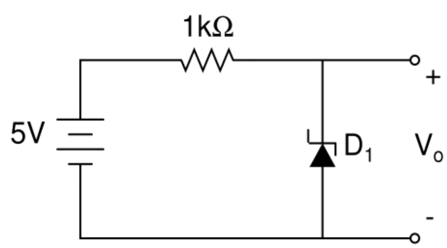


Fig. 1.2. See question 1 ii.

iii. Fig. 1.3 shows the bipolar junction transistor characteristic curves, for different base currents, (collector current vs collector emitter voltage). What are regions I and II known as?

a) I is saturation, II is active
b) I is cut-off, II is saturation
c) I is active, II is saturation
d) I is cut-ff, II is active

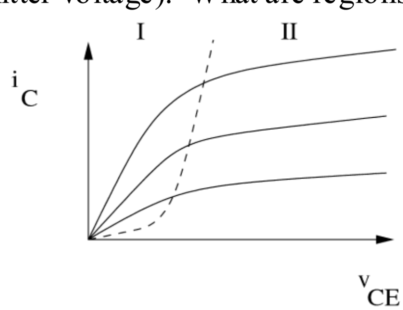
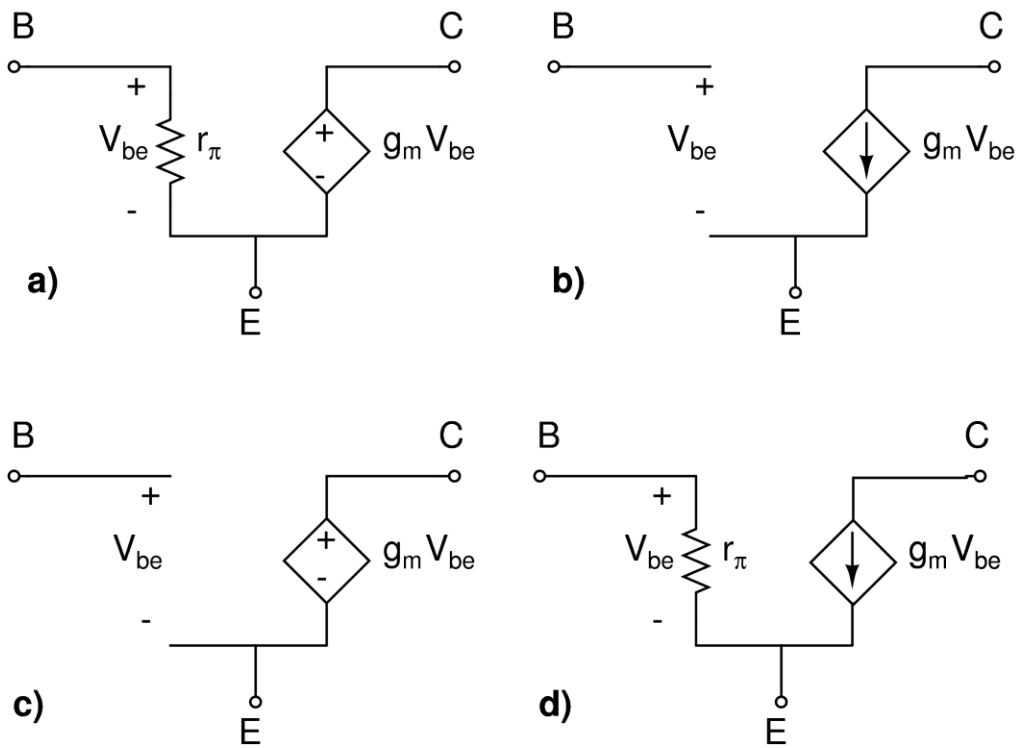


Fig. 1.3. See question 1 iii.

iv. What is the correct version of the hybrid π model for the bipolar junction trnasistor?



v. The circuit in Fig. 1.4 is known as what type of circuit?
  a) An inverting amplifier
  b) A miller integrator
  c) A differentiator
  d) A voltage follower

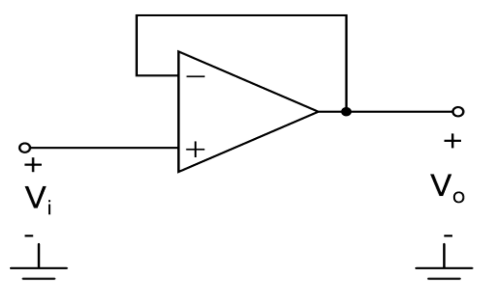


Fig. 1.4. See question 1 v.

vi. Which of the following statements is true about the *ideal* operational amplifier?
  a) The open loop gain and the output impedance are infinite
  e) The device bandwidth and the output impedance are infinite
  f) The device bandwidth and the input impedance are infinite
  g) The input and output impedances are infinite

vii. What is the gain, V_o/V_{in}, for the circuit in Fig. 1.5?
  a) 5
  b) -5
  c) -1/5
  d) 6

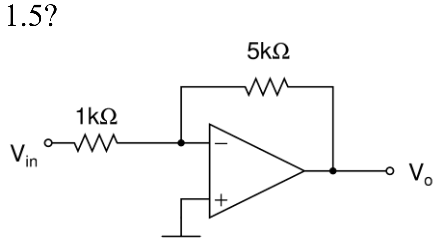


Fig. 1.5. See question 1 vii

viii. The MOSFET in Fig. 1.6 has the following parameters $k_n = 200$ µA/V^2, $V_t = 0.6$ V, $W = 4$µm and $L = 0.8$ µm. What is the closest value of R, to set I_D to 100 µA and what will be V_D?

a) R = 40 kΩ, V_D = 0 V
b) R = 30 kΩ, V_D = 1.05 V
c) R = 36 kΩ, V_D = 0.92 V
d) R = 14 kΩ, V_D = 2.6 V

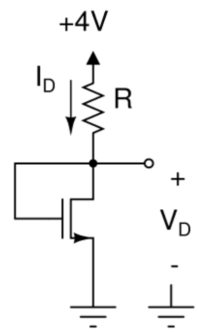


Fig. 1.6. See question 1 viii

ix. For a MOSFET what is region x, as marked on the characteristic curves in Fig. 1.7?

a) Triode region
b) Cut-off region
c) Active region
d) Saturation region

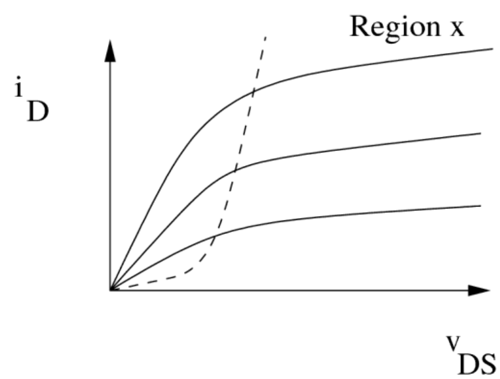
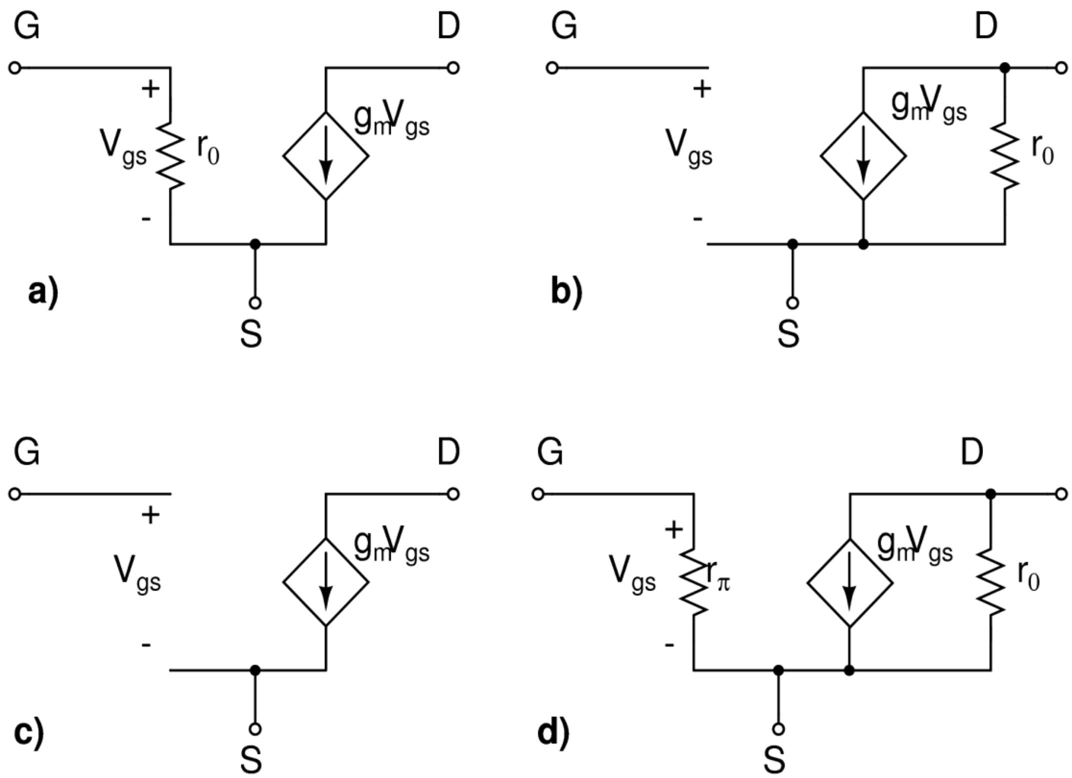


Fig. 1.7. See question 1 ix.

x. What is the small signal model equivalent circuit for a MOSFET with *channel length modulation*?


G
D
S
V_{gs}
r_0
$g_m V_{gs}$
r_π
a)
b)
c)
d)

Q2: Diodes

a) The circuit has been designed in Fig. 2.1, with diodes having forward voltages of 0.7V.

i. If V_A = -2V V_B = 3V, V_C = 5V and V_D = 0.5V, what will be the output at Vx and the current I? If voltage V_A, V_B, V_C and V_D could only be 0V or 5V this circuit could be used as a logic gate. What type of gate would it be? **(4 Marks)**

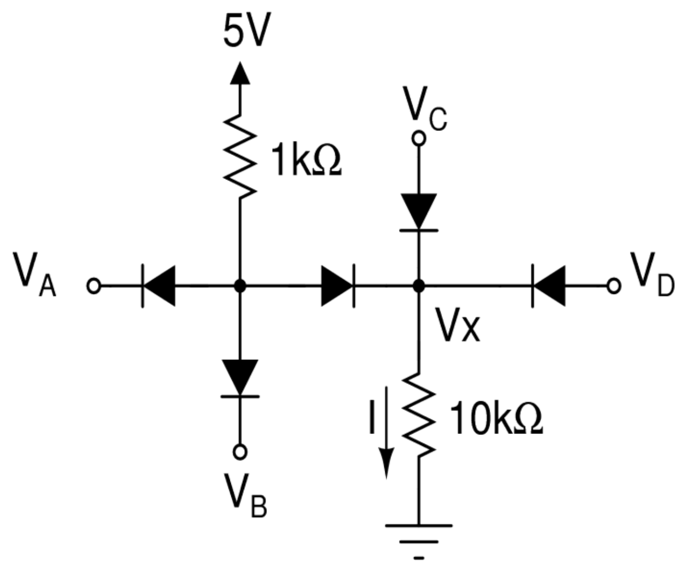


Fig. 2.1. See question 2 a).

V_x = ________

I = ________

Logic Gate Type = __________________

b) Design limiter circuits using only diodes and 10kΩ resistors to provide an output signal limited to the specified ranges (given below). Assume a constant-voltage drop model for the diodes, with
V_D = 0.7 V.

i. Output specification: -0.7 V and above.

(2 marks)

ii. Output specification: -2.1 V and above.

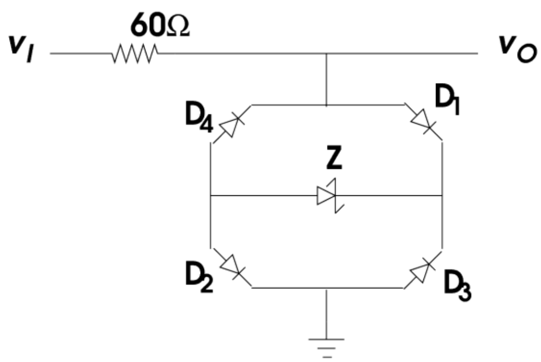
(2 marks)

iii. Output specification: ±1.4 V.

(2marks)

c) Sketch and clearly label the transfer characteristics $\frac{v_o}{v_I}$ of the circuit in Fig. 2.2 for $-15V \le v_I \le +15V$. Assume that the diodes can be represented by a piecewise-linear model with V_{D0} = 0.7V and r_D = 20 Ω. For the zener diode, a zener voltage of 8.2 V is measured at a current of 10 mA and r_z = 20 Ω. Assume a piecewise-linear model for the zener diode as well.

(6 marks)



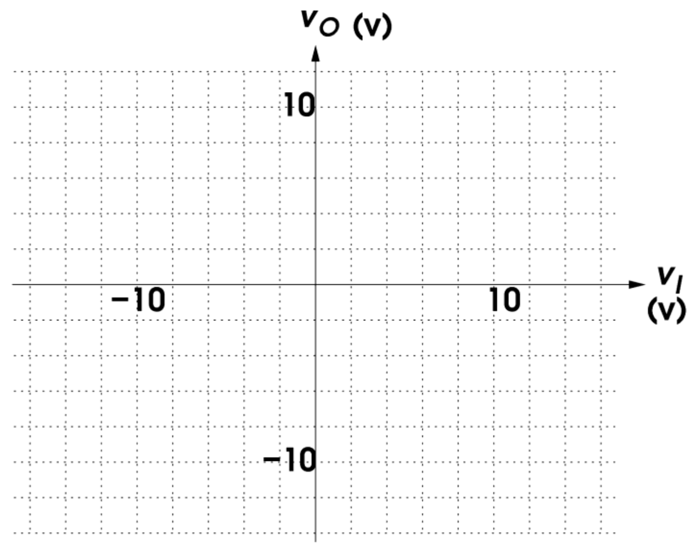


Fig. 2.2. See question 2 c).

d) Using diodes and capacitors design clamper circuits for a -10V to 10V peak to peak square wave input, v_I, to satisfy the following output specifications. Assume that the time constant of the circuit are much larger than the cycle time (period) of the input wave form. Assume ideal diode models.

i. Output specification: $0V \leq v_o \leq 20V$

(2 marks)

ii. Output specification: $-20V \leq v_o \leq 0V$

(2 marks)

Q3: MOSFET

An NMOS transistor has the following specifications: $k_n'\frac{W}{L}$ = 1 mA/V^2 , V_A = 50 V, V_t = 1V, t_{ox} = 10 nm and μ_n = 500 cm^2/Vs.

a) What is the gate oxide capacitance, C_{ox}, in pF/ μ_nm^2?

(1 mark)

C_{ox},________________

b) What is the device transconductance, k_n', in F/Vs?

(1 mark)

k_n'_________________

c) If the channel length L is 0.1 μm, what is the channel width, *W*, in μm? Sketch the structure of the physical device showing t_{ox}, *L*, *W* and the four terminals G, D, S and B.

(3 marks)

*W*_________________

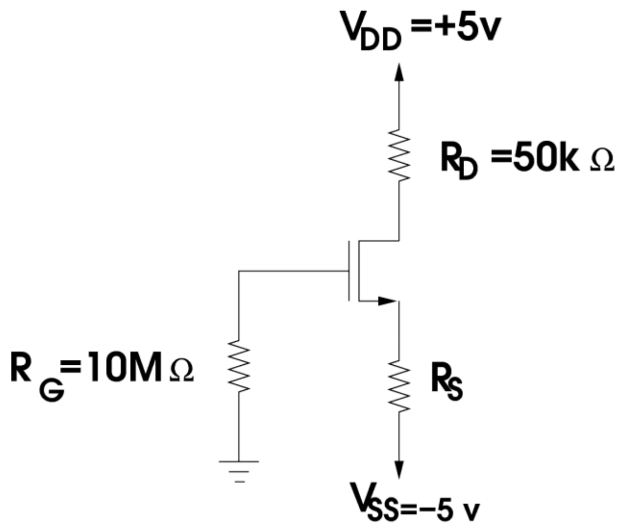


Fig 3.1. See question 3 h) and i)

d) Using the configuration in Fig. 3.1, we would like to bias the transistor to obtain g_m =1 mA/V and r_o = 500 kΩ . Find the current I_D and terminal voltages V_G , V_D and V_S.

(3 marks)

V_G__________________, V_D_________________and V_S_____________________

e) What value of R_S should be chosen?

(1 mark)

R_S_____________________

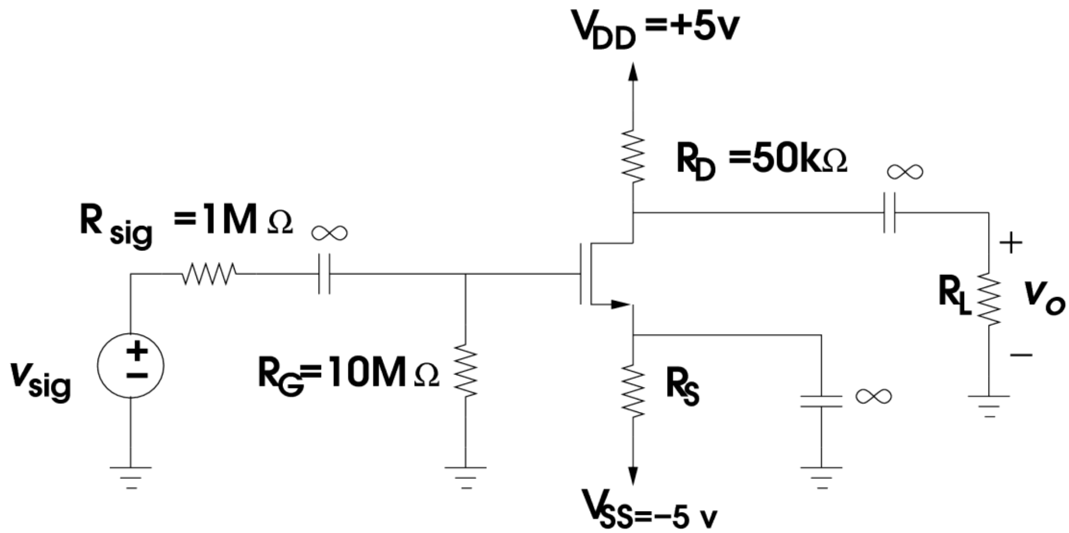


Fig. 3.2. See question 3 f) onwards.

Now, we are going to build a small-signal amplifier operating at the specified bias in part d). The configuration is shown in Fig. 3.2

f) What is this amplifier called and why?

(1 mark)

g) Draw the equivalent small signal hybrid-π model of the circuit.

(2 marks)

h) Show that the overall open-circuit (R_L = ∞) gain of the circuit is given by

$G_{v0} = \frac{-R_G}{R_G + R_{sig}} g_m (r_o \; R_D)$ and calculate this gain.

(3 marks)

G_{v0} ________________________

i) What value of R_L do you choose to obtain an overall gain G_v of 10 V/V

(2 marks)

R_L ________________________

j) Find the input resistance R_{in} and output resistance R_{out}.

(3 marks)

R_{in} ____________________ R_{out} ____________________*t*

k) What are the maximum positive and negative swings at the output?

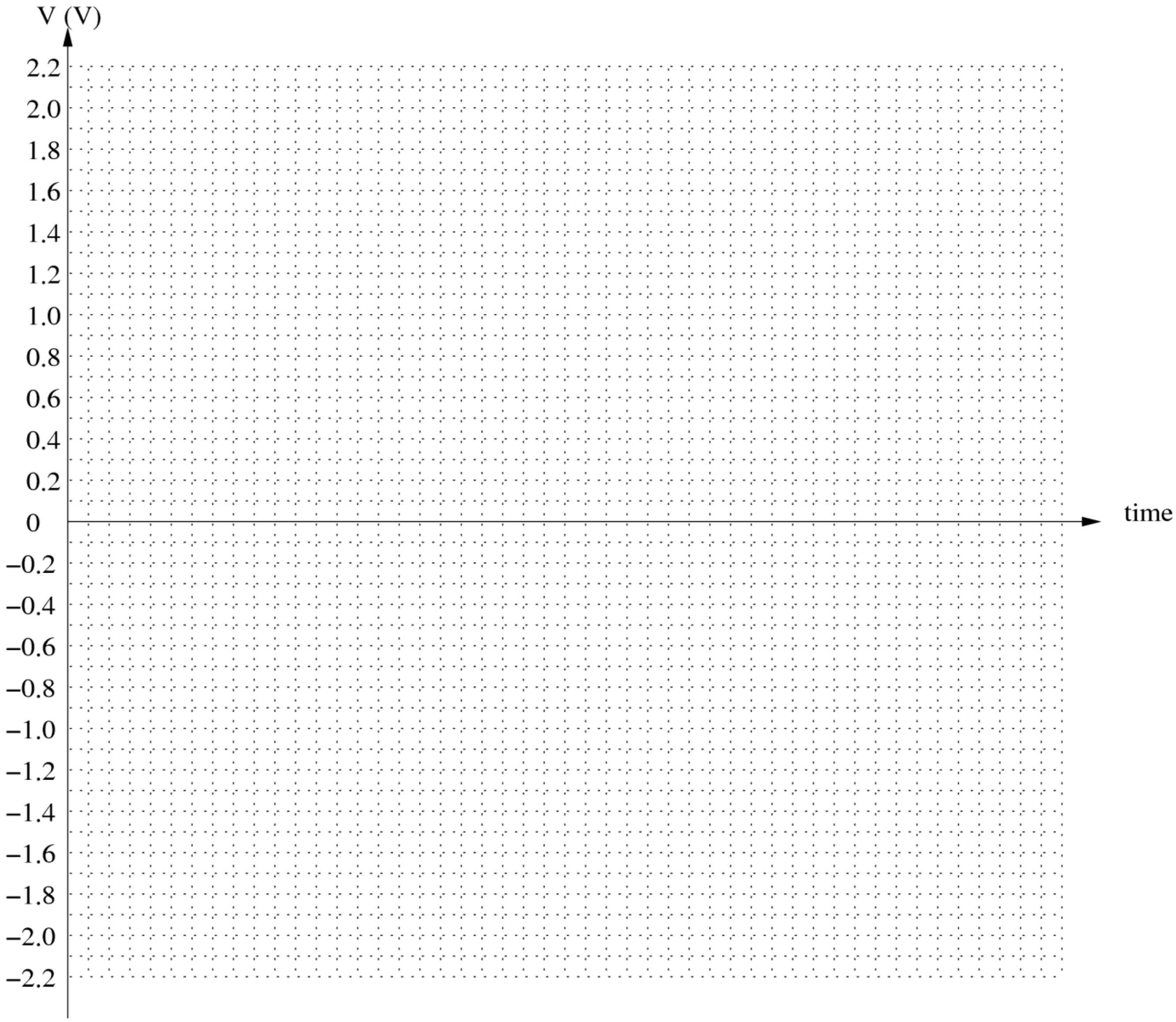
(2 marks)

Max positive swing ____________________________

Max negative swing ____________________________

l) If the v_{sig} is a 0.4V peak to peak sinusoidal signal, show the "total" instantaneous input signal at the gate and the "total" instantaneous output signal at the drain by plotting the waveforms on the graph (next page).

(3 marks)


V (V)
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1.0
−1.2
−1.4
−1.6
−1.8
−2.0
−2.2
time

Q4: BJT

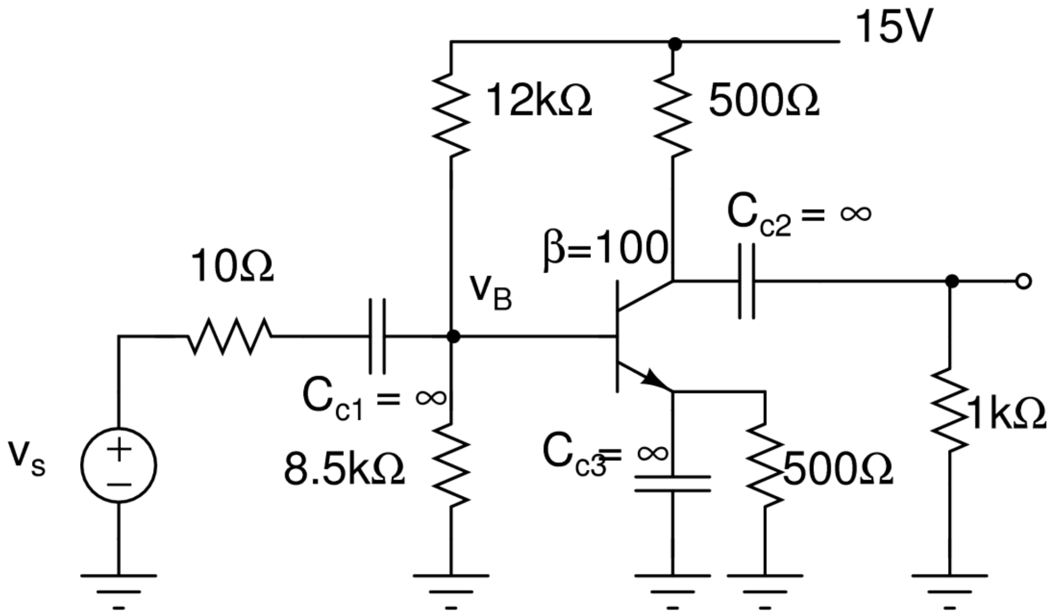


Fig 4.1. See question 4.

a) For the BJT amplifier circuit shown in Fig. 4.1:

i. Draw the DC equivalent circuit that can be used for calculating DC voltages and currents

(3 marks)

ii. Assuming room temperature, determine values for V_B, V_C, I_B, and I_C (Where V_B etc. have their usual meaning):

(7 marks)

V_C=_________

V_B=_________

I_B=_________

I_C=_________

b)

i. The BJT in figure 4.1 had an early voltage of 200V. Compute parameters $\mathbf{r_\pi}$, $\mathbf{g_m}$, **and** $\mathbf{r_o}$,

(3 marks)

g_m=_________

r_o=________

r_π =_________

ii. Draw the small signal A. C. equivalent circuit based on parameters calculated above in 4 b) **(use the hybrid π model).**

(5 marks)

iii. Find the input resistance R_i

(2 marks)

R_i=_________

iv. Find the intermediate voltage gain, $A_{v1} = v_i/v_s$, where v_i is the small-signal voltage between the base and the ground.

(1 mark)

A_{v1}=________

v. Find the intermediate voltage gain $A_{v2} = v_o/v_i$.

(3 marks)

A_{v2}=_________

vi. Find the overall voltage gain, $A_v=v_o/v_s$.

(1 mark)

A_v=________

Q5. Operational Amplifier

a) Using an ideal operational amplifier, you have been asked to design an integrator which has an input resistance of $50k\Omega$ and a time constant of 10^{-2} s.

i. Draw and clearly label the circuit. Calculate any necessary values of individual components and mark those on the circuit.

(5 marks)

ii. Determine the gain of the circuit at 10 rad/s and 1000 rad/s.

(2 marks)

iii. At what angular frequency is the gain magnitude one?

(1 mark)

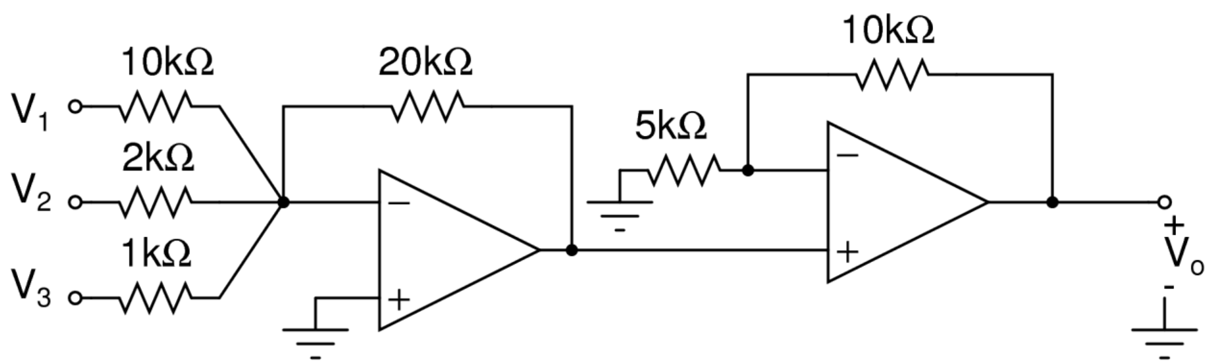


Figure 5.1

b) A student designs a circuit, shown in Fig. 5.1, with the intention that it carries out the following mathematical operation.

$$V_o = \left(4V_1 + 20V_2 + 40V_3\right)$$

However, it is noticed that this is not the response of the circuit.

i. Analyze the circuit in Fig. 5.1 and determine the actual mathematical response for V_o in terms of the input V_1, V_2 and V_3.

(5 marks)

V_o = ____

ii. If V_1 = 10 mV , V_2 = 1 mV and V_3 = 5 mV what will be the output, V_o of the circuit if each operational amplifier has a supply voltage of ±15V?

(2 marks)

V_o = ____________________________

iii. If V_1 = V_2 = 1 V and V_3 = 0, with the same supply voltage of ±15V, comment on the output you would expect to see at V_o?

(2 marks)

iv. Design and draw a circuit that would produce the originally required output,

$$V_o = (4V_1 + 20V_2 + 40V_3)$$

(3 marks)

END