Université d'Ottawa
Faculté de génie

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et de génie électrique

uOttawa

L'Université canadienne
Canada's university

University of Ottawa
Faculty of Engineering

School of Electrical Engineering
and Computer Science

CEG2136: Computer Architecture I / CEG2536: Architecture des Ordinateurs I

MIDTERM EXAMINATION / Duration: 1 hour and 30 minutes
Professors: Voicu Groza, Sawsan Abdul-Majid and Michel Saydé

- Closed book exam. All electronic devices including calculators are not allowed.
- If in doubt how to interpret a question, make an assumption and elaborate your solution based on this hypothesis. Explain all your assumptions and well define the symbols used.

Question 1 (**20 points**) Give full marking for correct results (highlighted below), even though no explanations would be provided

A. Express -18.125 in floating point in accordance with the Standard IEEE 754 (32 bits). Show the:

a- Binary value:

2	$-(10010.001)_2$	or 2's compl	**1** 01101.111	or Sign magnitude	**1** 10010.001

b- Normalized value:

2 $(1.0010001)_2$ $(x10^{100})_2$ or $(1.0010001)_2$ x 2^4

c- Mantissa:

2 $(0010001)_2$

d- Exponent:

3 $(10000011)_2$ = $(131)_{10}$ = 127+4

e- Content of the 32-bit register in binary

3 1100 0001 1001 0001 0000 0000 0000 0000

f- Content of the 32-bit register in hexadecimal

2 C1910000

B. 2 pts For ODD Parity error detection, which one(s) of the following four sequences will trigger an error detection?

a- 1011011100110 1 pt
b- 0111010101101 1 pt (a and b)
c- 1001100110110
d- 0110011001101

C. 2 pts What is the range of representable numbers for signed numbers in a 9-bit register?

a- 0 to 511
b- -512 to 511
c- -256 to 255
d- 0 to 512

D. 2 pts For the negative number $(-12.75)_{10}$, which one of the following binary numbers is its representation in signed magnitude format in a 10-bit register?

a- 11110011.00
b- 10001100.11
c- 11110011.01
d- 00001100.11

Question 2 (**14 points**)

A. List the truth table of three – variable exclusive-OR (XOR) function, where X is the output, and A, B, and C are the inputs 8 pts = 1 pt for each row

A	B	C	X	
0	0	0	0	1 pt
0	0	1	1	1 pt
0	1	0	1	1 pt
0	1	1	0	1 pt
1	0	0	1	1 pt
1	0	1	0	1 pt
1	1	0	0	1 pt
1	1	1	1	1 pt

B. 4 pts Complete the following statements:

1: 2 pts Logic functions can be represented by:

…0.5 pt …Logic (Boolean) expressions, ……0.5 pt …truth tables ……………………

…0.5 pt ……………K-maps……….. and …0.5 pt logic diagrams (schematics)……

2: 2 pts ………Prime Implicant……………….. is an implicant which cannot be totally covered by another implicant.

C. 2 pts In a real practical combinational circuit, the output is (give 2 points for any of the two highlighted answers):

1- Time-dependent and does only depend on the circuit's input

2-Time-independent and does only depend on the circuit's input (1 or 2)

3- Time –independent and does not depend on the circuit's input

Question 3 (30 points)

8-bit registers are used in this question to store numbers expressed in 2’s complement representation.

(a) 12 pts Convert the following signed numbers to binary using 2’s complement representation.

A = $(+70)_{10}$	2		0	1	0	0	0	1	1	0
B = $(-70)_{10}$	4		1	0	1	1	1	0	1	0
C = $(+80)_{10}$	2		0	1	0	1	0	0	0	0
D = $(-80)_{10}$	4		1	0	1	1	0	0	0	0

(b) 12 pts Perform the following arithmetic operations in signed-2’s complement representation, keeping in mind that the results are represented with 8 bits too; show operations and results (including intermediary steps), both in binary and in decimal.

Y = A + C
6

	Cy8	Cy7	Cy6	Cy5	Cy4	Cy3	Cy2	Cy1	Cy0			
Cy	1	0	0	0	0	0	0					
A		0	1	0	0	0	1	1	0		+70	
C		0	1	0	1	0	0	0	0		+80	
Y	4	1	0	0	1	0	1	1	0		+150	2

Z = C + D
6

	Cy8	Cy7	Cy6	Cy5	Cy4	Cy3	Cy2	Cy1	Cy0			
Cy	1	1	1	1	0	0	0	0				
C		0	1	0	1	0	0	0	0		+80	
D		1	0	1	1	0	0	0	0		-80	
Z	4	0	0	0	0	0	0	0	0		0	2

(c) 6 pts Is there any overflow in Y and/or Z 2 pts? Justify your answer 2 pts. How would a computer detect overflows in these operations? 2 pts

Yes, there is overflow in Y 1 pt, since the sum Y is out of range: +150 > 127 (max >0 with 8 bits); also we obtained a negative sign bit from the addition of 2 positive numbers!? 1 pt.

No overflow in Z 1 pt since we added two numbers with different signs, and, of course, the result Z = 0 is in the range of signed numbers with 8 bits [-128, +127] 1 pt.

Overflow Detection Expressions:

1. if (SgnA=SgnB) ≠ SgnS ➔ Overflow = (SgnA’·SgnB’·SignS +SgnA·SgnB·SgnS’) 1 pt.
2. if the carry bits TO & FROM the sign bit are different
   $(Cy_8 \cdot Cy'_7 + Cy'_8 \cdot Cy_7) = (Cy_8 \oplus Cy_7)$ 1 pt

Question 4 (**36 points**)

1. **20 points** Design a one-digit BCD counter using four T flip-flops and any kind of logic gates that you may need.
   a. Provide the excitation table of the BCD counter and the equations of the inputs of the T flip-flops (T_3, T_2, T_1 and T_0).

10pts	1/2	1/2	1/2	1/2	1pt	1pt	1pt	1pt	1pt	1pt	1pt	1pt
	Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	1
2	0	0	1	0	0	0	1	1	0	0	0	1
3	0	0	1	1	0	1	0	0	0	1	1	1
4	0	1	0	0	0	1	0	1	0	0	0	1
5	0	1	0	1	0	1	1	0	0	0	1	1
6	0	1	1	0	0	1	1	1	0	0	0	1
7	0	1	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	1	0	0	1	0	0	0	1
9	1	0	0	1	0	0	0	0	1	0	0	1
10	1	0	1	0	x/0	x/0	x/0	x/0	x/1	x/0	x/1	x/0
11	1	0	1	1	x/0	x/0	x/0	x/0	x/1	x/0	x/1	x/1
12	1	1	0	0	x/0	x/0	x/0	x/0	x/1	x/1	x/0	x/0
13	1	1	0	1	x/0	x/0	x/0	x/0	x/1	x/1	x/0	x/1
14	1	1	1	0	x/0	x/0	x/0	x/0	x/1	x/1	x/1	x/0
15	1	1	1	1	x/0	x/0	x/0	x/0	x/1	x/1	x/1	x/1

if not BCD, give 5 pts not 10 pts — 5pts

Using don't care states for
10, 11, 12, 13, 14, 15

$T_0 = 1$ 1pt

$T_1 = Q'_3 \cdot Q_0$ 1pt

$T_2 = Q_1 \cdot Q_0$ 1pt

$T_3 = Q_3 \cdot Q_0 + \boxed{Q_2 \cdot Q_1 \cdot Q_0}$ 2pts

Or, if return to 0000 from any of
the states 10, 11, 12, 13, 14, 15

$T_0 =$

$T_1 = Q'_3 \cdot Q_0 + Q_3 \cdot Q_1$

$T_2 = Q_3' \cdot Q_1 \cdot Q_0 + Q_3 \cdot Q_2$

$T_3 = Q_3 \cdot Q_0 + \boxed{Q_2 \cdot Q_1 \cdot Q_0} + Q_3 \cdot Q_2 + \boxed{Q_3 \cdot Q_1}$

T_3

$Q_1 Q_0$ $Q_3 Q_2$	00	01	11	10
00	0 0	1 0	3 0	2 0
01	4 0	5 0	7 1	6 0
11	12 x	13 x	15 x	14 x
10	8 0	9 1	11 x	10 x

T_2

$Q_1 Q_0$ $Q_3 Q_2$	00	01	11	10
00	0 0	1 0	3 1	2 0
01	4 0	5 0	7 1	6 0
11	12 x	13 x	15 x	14 x
10	8 0	9 0	11 x	10 x

T_1

$Q_1 Q_0$ $Q_3 Q_2$	00	01	11	10
00	0 0	1 1	3 1	2 0
01	4 0	5 1	7 1	6 0
11	12 x	13 x	15 x	14 x
10	8 0	9 0	11 x	10 x

$Q_1 Q_0$ $Q_3 Q_2$	00	01	11	10
00	0 0	1 0	3 0	2 0
01	4 0	5 0	7 1	6 0
11	12 1	13 1	15 1	14 1
10	8 0	9 1	11 1	10 1

$Q_1 Q_0$ $Q_3 Q_2$	00	01	11	10
00	0 0	1 0	3 1	2 0
01	4 0	5 0	7 1	6 0
11	12 1	13 1	15 1	14 1
10	8 0	9 0	11 0	10 0

$Q_1 Q_0$ $Q_3 Q_2$	00	01	11	10
00	0 0	1 1	3 1	2 0
01	4 0	5 1	7 1	6 0
11	12 0	13 0	15 1	14 1
10	8 0	9 0	11 1	10 1

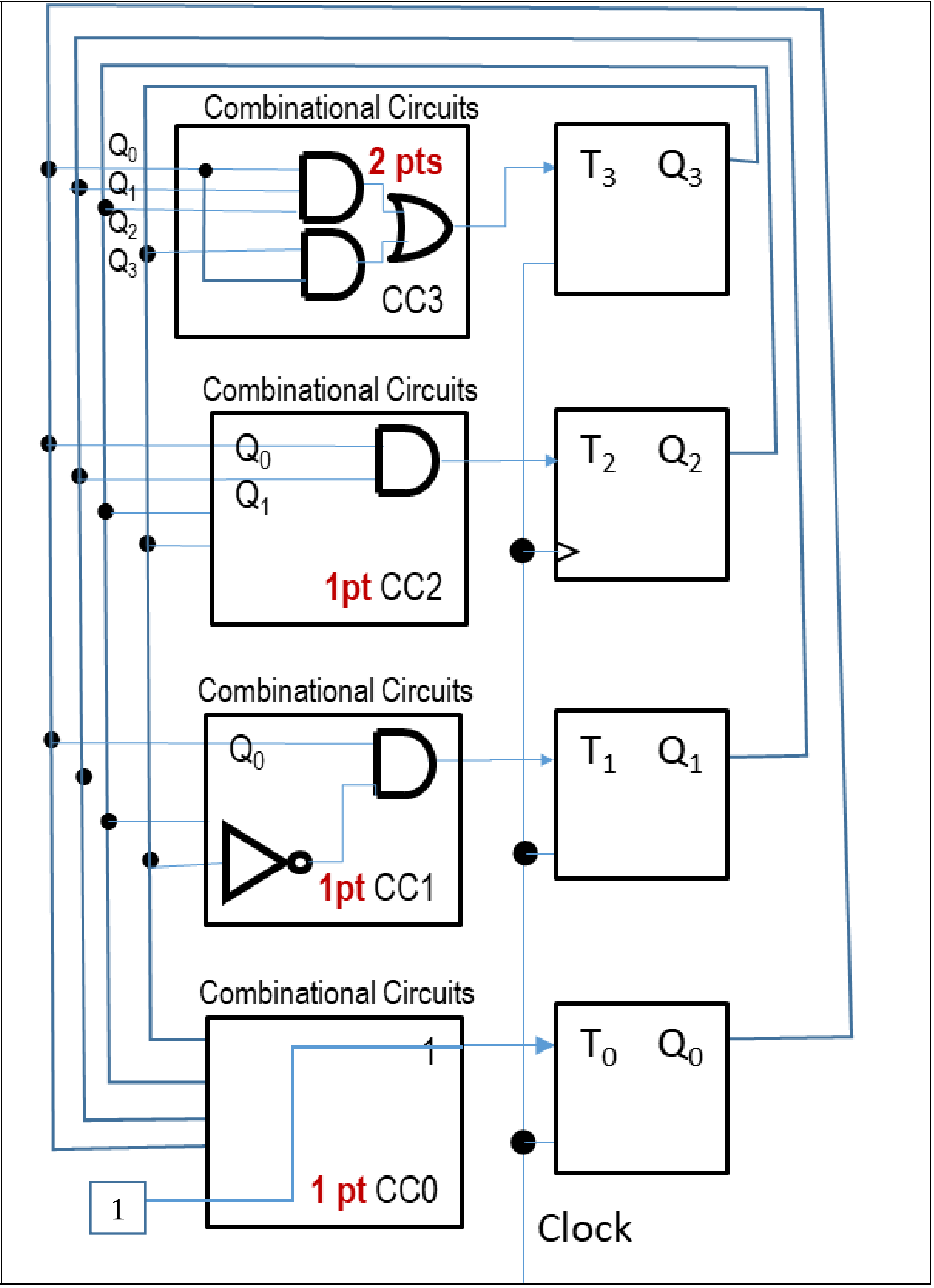
5pts Draw the combinational circuits that implement the excitation equations of the T flip-flops inside the corresponding boxes CC0, CC1, CC2 and CC3.

$T3 = Q3 \cdot Q1' \cdot Q0 + Q2 \cdot Q1 \cdot Q0$

$T2 = Q1 \cdot Q0$

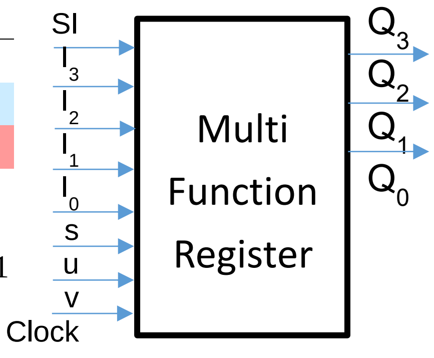
$T1 = Q'3 \cdot Q0$

$T0 = 1$



2. 16 points Design a 4-bit multifunction register whose operation is described in the following table, where s, u and v are three control bits. Using the proper digital components (encoders, decoders, multiplexers, etc.), logic gates, and T flip-flops, draw a detailed diagram of the logic circuit of the register.

	s	u	v	Operation
2 pts	0	0	0	No change = stores current state
2 pts	0	0	1	Synchronous reset/clear (0 ➔ $Q_3Q_2Q_1Q_0$)
4 pts	0	1	0	Shift left
4 pts	0	1	1	Parallel loading external inputs $I_3I_2I_1I_0$➔ $Q_3Q_2Q_1Q_0$
4 pts	1	x	x	BCD counter - here you can reuse the block diagrams CC0, CC1, CC2 and CC3 that you obtained above in 4-1 (no need to redesign them again)



suv = 000

Function	Transition (next state) Equations	Excitation Equations T_i
Store register's content	$Q_i\ (n+1) = Q_i\ (n)$; $i= \{0,1,2,3\}$	$T_i = 0$; $i = \{0,1,2,3\}$ 2 pts

suv = 001

Present state	*Next state*	T excitation
$Q_i(n)$	$Q_i(n+1)$	T_i
0	0	0
1	0	1
0	0	0
1	0	1

$T_i = Q_i$; $i = \{0,1,2,3\}$ 2 pts

suv = 010 Left shift (register's *serial input* is connected to an external input *SI*)

Using the excitation table of the T-FF:

Present state		*Next state*	T excitation
$Q_i(n)$	$Q_{i-1}(n)$	$Q_i^+ = Q_i(n+1)$	T_i
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

$T_i = Q_i \oplus Q_{i-1}$; $i = 1,2,3$ 3 pts3

$T_0 = Q_0 \oplus SI$ 1 pt3

… or using the excitation equation of the T-FF

Transition Equations:
$Q_i\ (n+1) = Q_{i-1}\ (n)$; $i=1,2,3$
$Q_0\ (n+1) = SI$

Excitation equation of T-FF:
$T_i = Q_i^n \cdot \overline{Q_i^{n+1}} + Q_i^{n+1} \cdot \overline{Q_i^n}$; $i = 1, 2,3$
But since $Q_i^{n+1} = Q_{i-1}^n$
➔ $T_i = Q_i^n \cdot \overline{Q_{i-1}^n} + Q_{i-1}^n \cdot \overline{Q_i^n}$; $i = 1,2,3$

… or, starting from the basics:

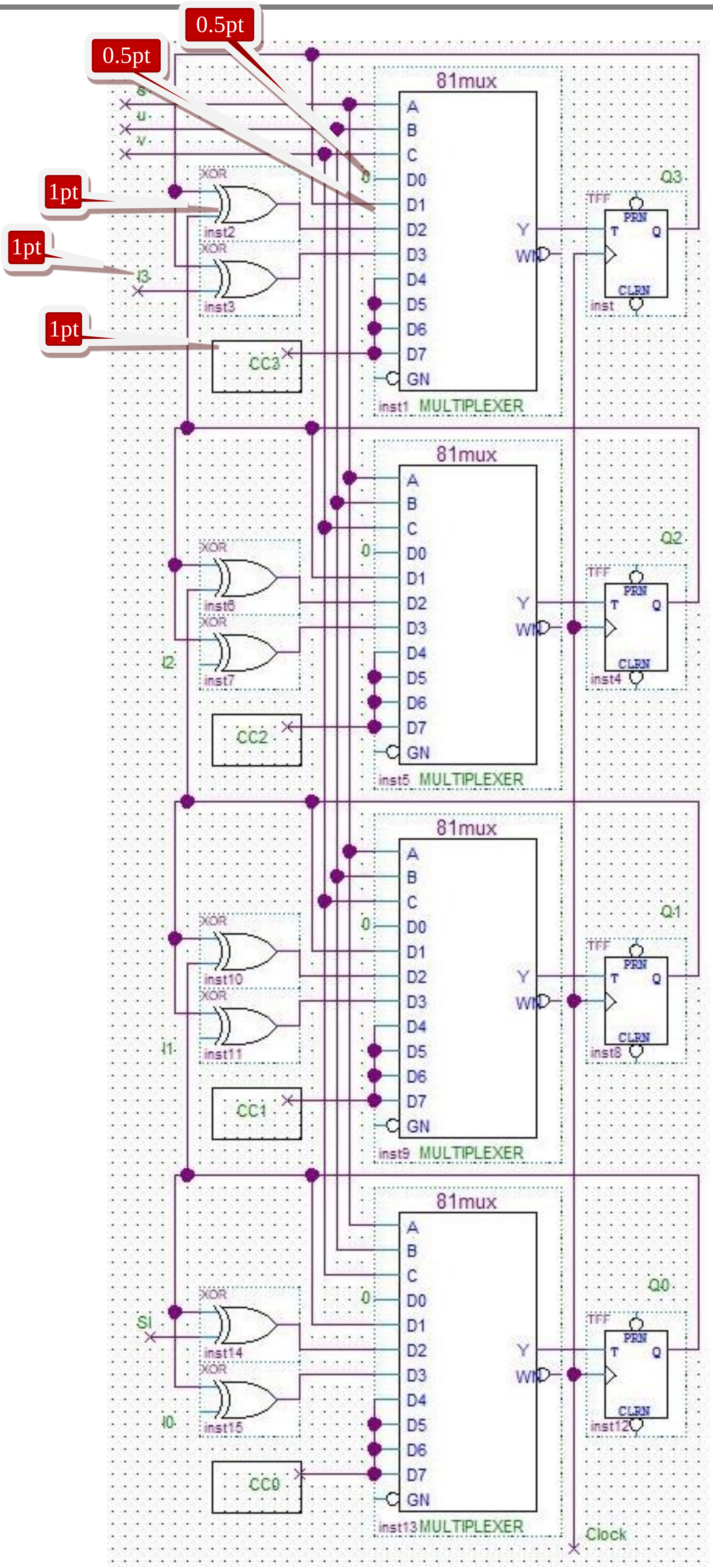
if $Q_i(n) = Q_{i-1}(n) \Rightarrow T_i = 0$;
if $Q_i(n) \neq Q_{i-1}(n) \Rightarrow T_i = 1$;
i.e., $T_i = Q_i \oplus Q_{i-1}$, $i = 1,2,3$;
$T_0 = Q_0 \oplus SI$

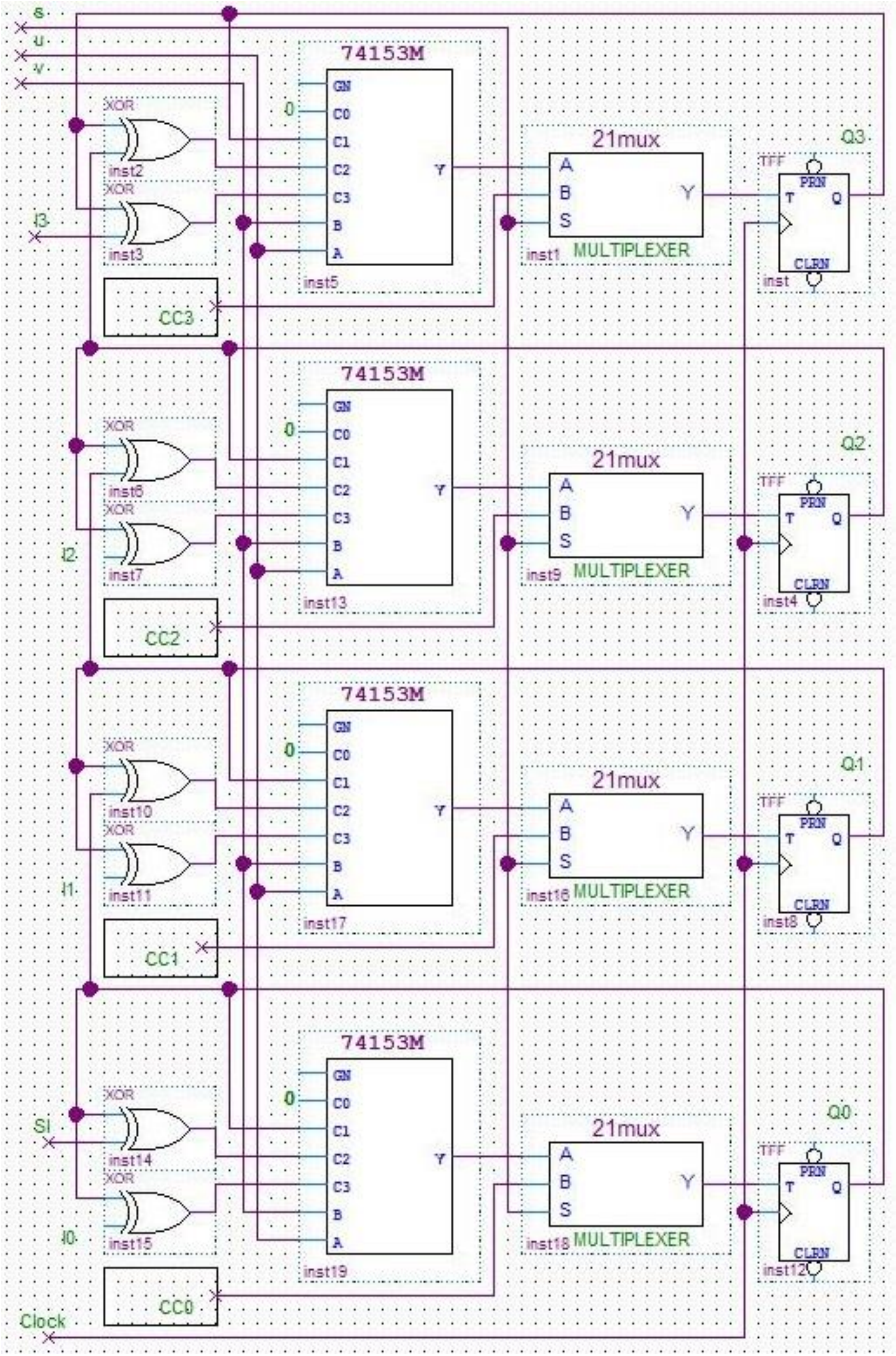
suv = 011 Parallel loading external inputs $I_3I_2I_1I_0$➔ $Q_3Q_2Q_1Q_0$

Pr.state	*Input*	*Next state*	T excitation
$Q_i(n)$	I_i	$Q_i^+ = Q_i(n+1)$	T_i
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

$T_i = Q_i \oplus I_i$; $i = 0,1,2,3$ 4 pts

All points will be given even if only the correct schematics is provided. If the schematics or part of it is not drawn, ONLY half of the missing part's points will be given for the correct equations.

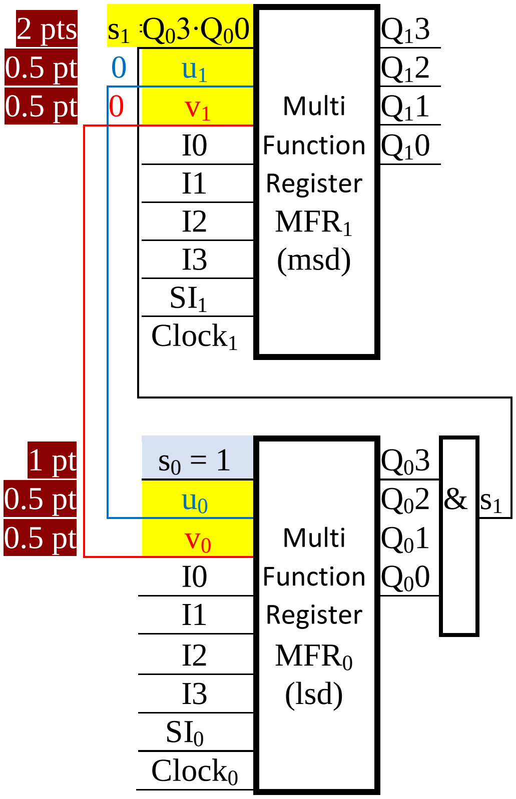

0.5pt
0.5pt
1pt
1pt
1pt
s
u
v
I3
I2
I1
I0
SI
XOR
inst2
inst3
inst6
inst7
inst10
inst11
inst14
inst15
CC3
CC2
CC1
CC0
81mux
A
B
C
0
D0
D1
D2
D3
D4
D5
D6
D7
GN
Y
WN
inst1 MULTIPLEXER
inst5 MULTIPLEXER
inst9 MULTIPLEXER
inst13 MULTIPLEXER
TFF
PRN
T
Q
CLRN
inst
inst4
inst8
inst12
Q3
Q2
Q1
Q0
Clock


s
u
v
I3
I2
I1
I0
SI
Clock
XOR
inst2
inst3
inst6
inst7
inst10
inst11
inst14
inst15
CC3
CC2
CC1
CC0
74153M
GN
C0
C1
C2
C3
B
A
Y
0
inst5
inst13
inst17
inst19
21mux
A
B
S
Y
MULTIPLEXER
inst1
inst9
inst16
inst18
TFF
PRN
T
Q
CLRN
inst
inst4
inst8
inst12
Q3
Q2
Q1
Q0

3. (5 pts bonus question) Draw the block diagram of a two-digit BCD counter built with two 4-bit multifunction registers that you have designed above and which can count to 99_{10}.

The counter is formed of 2 Multi-function Registers (MFR_1 and MFR_0). For the BCD counting mode, both **u** and **v** are don't care (uv = xx); as the counting operation is controlled by **s** only. MFR_0 (lsd) is programmed to count every clock, i.e., $s_0 = 1$, while MFR_1 should store the current digit (s_1 u_1 v_1 = 0 0 0). After MFR_0 count reaches 9 = 1001_2, MFR_1 has to be incremented $s_1 = 1$.

	M	F	R	1	MFR_1^+				MFR_0^+			
	Q_03	Q_02	Q_01	Q_00	(msd)	s1	u1	v1	(lsd)	s_0	u_0	v_0
0	0	0	0	0	No change	0	0	0	Count up	1	x	x
1	0	0	0	1	No change	0	0	0	Count up	1	x	x
2	0	0	1	0	No change	0	0	0	Count up	1	x	x
3	0	0	1	1	No change	0	0	0	Count up	1	x	x
4	0	1	0	0	No change	0	0	0	Count up	1	x	x
5	0	1	0	1	No change	0	0	0	Count up	1	x	x
6	0	1	1	0	No change	0	0	0	Count up	1	x	x
7	0	1	1	1	No change	0	0	0	Count up	1	x	x
8	1	0	0	0	No change	0	0	0	Count up	1	x	x
9	1	0	0	1	Count up	1	x	x	Count up	1	x	x
10	1	0	1	0	x	x	x	x	x	x	x	x
11	1	0	1	1	x	x	x	x	x	x	x	x
12	1	1	0	0	x	x	x	x	x	x	x	x
13	1	1	0	1	x	x	x	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x	x	x	x
15	1	1	1	1	x	x	x	x	x	x	x	x



s_1

$Q_03\ Q_02$ \ $Q_01\ Q_00$	00	01	11	10
00	0 0	1 0	3 0	2 0
01	4 0	5 0	7 0	6 0
11	12 x	13 x	15 x	14 x
10	8 0	9 1	11 x	10 xd

$s_1 = Q_03 \cdot Q_00$

$u_1 = 0$

$v_1 = 0$

- All 5 pts will be given for correct diagram, regardless of providing explanations with state table or equations
- Equivalently 2 points will be given for $Q_03 \cdot Q_0$ driving Clock 1 directly, rather than s_1