Ryerson University
Department of Computer Science
CPS213 – Computer Organization I
Fall 2015
Midterm
November 06, 6:15PM - Duration: 70 minutes
No Aids Allowed.

Version: 1

Family Name: _____ Given Name: _____

Student #: _____

INSTRUCTIONS:

- Read the instructions on this sheet carefully.
- Fill in your name, student ID, and the exam Version (1) on your scantron.
- **Mark the correct answer on your scantron ONLY.**
- There is only one correct answer for each multiple choice question.
- There is a **penalty** of **0.25 mark** for each wrong answer.
- This is a closed book exam. Use of calculator or any other electronic device is not allowed.
- All bags must be placed at the front or back of the room.

Signature: _____

Part A: Short answer questions.

[1 Mark] 1. Convert the following decimal numbers into signed integer 32-bit representation (2's complement for negative numbers).

-66

A. 1000 0000 0000 0000 0000 0000 0011 1100
B. 1111 1111 1111 1111 1111 1111 1111 0010
C. 1111 1111 1111 1111 1111 1111 1011 1110
D. 1000 0000 0000 0000 0000 0000 0011 1011
E. none of these

[1 Mark] 2. Convert the following decimal numbers into signed integer 32-bit representation (2's complement for negative numbers).

81

A. 1000 0000 0000 0000 0000 0000 0101 1001
B. 0000 0000 0000 0000 0000 0000 0100 1000
C. 0000 0000 0000 0000 0000 0000 0101 0011
D. 0000 0000 0000 0000 0000 0000 0101 0001
E. none of these

[1 Mark] 3. Convert the following binary number (unsigned 32-bit integers) into decimal.

0000 0000 0010 0000 0000 0001 0001 1001

A. 281
B. 142
C. 35
D. 71
E. None of these

[1 mark] 4. Convert the decimal number 172 to hexadecimal:

A. A0
B. 67
C. AC
D. A7
E. None of the above

[1 mark] 5. In a 2-input AND gate, only one of the inputs is 1:

A. Cannot say anything about the output
B. The output is the same as the second input
C. The output is the same as the complement of the second input
D. The output is 1
E. None of the above

[1 mark] 6. In a 2-input XOR gate:

A. Only two outputs are 1
B. Only two outputs are 0
C. XOR is an odd function.
D. All of the above.
E. None of the above.

[1 mark] 7. The Boolean function f = a + b + c.a can be written as:

A. f = a.(1 + w')
B. f = 1
C. f = a + b
D. f = a.(1 . c) + b
E. None of the above

[1 mark] 8. Which one of the following is incorrect?

A. x + 0 = x
B. x.1 = x
C. x(x + y) = x
D. (x + y)' = x'. y'
E. None of the above

[1 mark] 9. Order of precedence in Boolean Algebra is:

A. NOT, (), AND, OR
B. (), NOT, OR, AND
C. (), NOT, AND, OR
D. NOT, (), OR, AND
E. None of the above

[1 marks] 10. The Boolean function (x + y) (x + y') is equal to:

A. xx + xy' + xy + yy' + 0
B. x + y
C. x + y'
D. x'
E. None of the above

[1 mark] 11. Which one of the all the followings is incorrect about minterms and Maxterms?

A. Are the same thing.
B. One is the complement of the other.
C. **n** literals have $\mathbf{2^n}$ minterms or Maxterm.
D. minterms are standard product.
E. None of the above

[1 mark] 12. Which one of the followings is incorrect?

A. Can build a 3-input AND gate out of two 2-input AND gates.
B. Can build a 3-input OR gate out of two 2-input OR gates.
C. Cannot build a 3-input NAND gate out of two 2-input NAND gates.
D. Cannot build a 3-input NOR gate out of two 2-input NOR gates.
E. None of the above

[1 marks] 13. In an 8-varibale K-map, two cells are identified as 1011 0010 and 1011 1010. Are these two cells adjacent?

A. Yes
B. No
C. Need to see the expression
D. Need to have the truth table
E. None of the above

[1 mark] 14. In an n-variable K-map, a grouping of 8 cells will always reduce the number of variables by:

A. 1
B. 2
C. 3
D. 4
E. None of the above

<u>Part B:</u> In this part, questions 15 to 19 are based on the following functions given below:

$F(x, y, z, w) = \prod (3, 7, 12, 13, 14)$

$d(x, y, z, w) = \Sigma (4, 5, 10, 11, 15)$

[2 marks] 15. To produce the product-of-the-sum (POS) for the above function, the don't cares given below must be treated as zeros:

A. 4, 11, 15
B. 4, 11
C. 11, 15
D. 4, 15
E. None of the above

[2 marks] 16. The POS for this function is:

A. $F(x, y, z, w) = (z' + w') (x' + y')$
B. $F(x, y, z, w) = (z + w) (x + y)$
C. $F(x, y, z, w) = (z' + w') (y' + z' + w) (x' + y')$
D. $F(x, y, z, w) = (x' + y' + z) (y' + z' + w)$
E. None of the above

[2 marks] 17. Knowing that $d(x, y, z, w) = \Sigma (4, 5, 10, 11, 15)$, the given function, $F(x, y, z, w)$, can be shown:

A. $\Sigma (1, 2, 4, 5, 6, 8, 9, 10, 14, 15)$
B. $\Sigma (0, 1, 2, 4, 5, 6, 8, 9, 10, 14, 15)$
C. $\Sigma (1, 2, 4, 5, 6, 8, 9)$
D. $\Sigma (0, 1, 2, 6, 8, 9)$
E. None of the above

[3 marks] 18. To produce the sum-of-the-product (SOP) for this function, the following don't cares must be treated as ones:

A. 4, 5, 10, 11
B. 4, 5
C. 4
D. 10, 11
E. None of the above

[2 marks] 19. The SOP for this function is:

A. $F(x, y, z, w) = y' w' + x' y' z' + x y' z'$
B. $F(x, y, z, w) = y' z' + z w'$
C. $F(x, y, z, w) = y' w' + x' z' + x y' z'$
D. $F(x, y, z, w) = x' w' + y' z'$
E. None of the above

<u>Part C</u>: In this part, questions 20 to 23 are based on the following function Boolean function:

$F(x, y, z) = x' y + x z + x' y z'$

[2 marks] 20. This function can be expressed in terms of its minterms as:

A. $F(x, y, z) = \Sigma (1, 2, 3, 5)$
B. $F(x, y, z) = \Sigma (2, 3, 5, 7)$
C. $F(x, y, z) = \Sigma (2, 3, 6, 7)$
D. $F(x, y, z) = \Sigma (2, 3, 4, 6)$
E. None of the above

[2 marks] 21. This function can be expressed in terms of its maxterms as:

A. $F(x, y, z) = \prod (0, 4, 6, 7)$
B. $F(x, y, z) = \prod (0, 1, 4, 6)$
C. $F(x, y, z) = \prod (0, 1, 4, 5)$
D. $F(x, y, z) = \prod (0, 1, 5, 7)$
E. None of the above

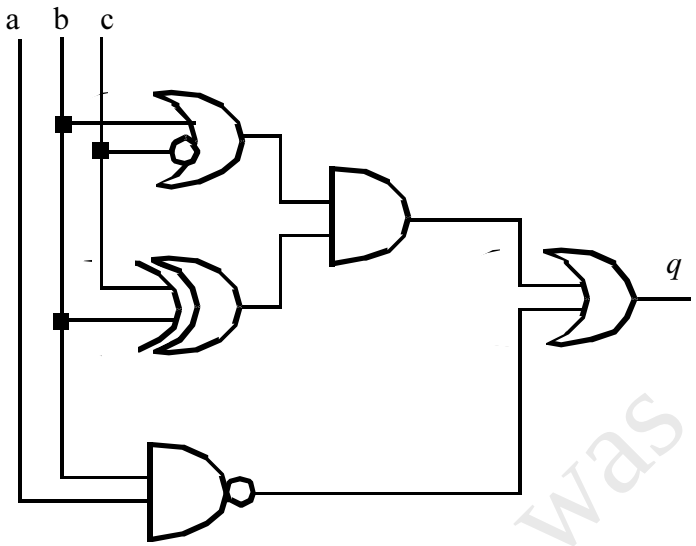
[4 marks] 22. Implement this function using a 4-to-1 MUX where the selection lines are x and y respectively. The MUX inputs (I_0-I_3) are:

A. 0, 1, z, z
B. 0, 1, z, z'
C. 0, 1, 0, 1
D. x', z, z, 1
E. None of the above

[2 marks] 23. Design this function using a 3 (I_0, I_1, I_2) to 8 (F_0, F_1, F_2, F_3, F_4, F_5, F_6, F_7) decoder and external gates.

A. AND (F_1, F_5), AND (F_3, F_5), then OR their results with F_2
B. OR (F_2, F_3), AND (F_4, F_6), then AND their results with F_1
C. AND (F_2, F_3, F_5, F_7)
D. OR (F_2, F_3, F_5, F_7)
E. None of the above

<u>Part D</u>: In this part, questions 24 to 30 are based on the following logic diagram.



[2 marks] 24. The output ***q*** can be expressed as:

A. $q = (a.b)' + (b'.c + b.c')$
B. $q = (a.b) + (b'.c' + b.c)$
C. $q = (a.b)' + (b'.c + b.c')(b'+ c')$
D. $q = (a+b)' + (b'.c + b.c') (b + c')$
E. None of the above

[3 marks] 25. Which one of the followings represent an alternative implementation of the above logic diagram.

Note: Complement of the literals are not available, i.e. ***x'***.

A. One NOR gate
B. Three 2-input NAND gates
C. Two 2-input NAND gates
D. One 3-input NAND gate
E. None of the above

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