LAB 5: Latches and Flip-Flops

ITI 1100 A – Digital Systems

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School of Engineering

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Lab Session 2

Group 13

Nick Allair: 8147249

Dhruv Pramod: 8285973

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Objectives

- Provide insight into the characteristics of several important latches and flip-flops
- Build latches and flip-flops from basic gates
- Provide insight to latching and edge triggering
- Test latches and flip-flops to understand their functionality

Equipment

- Quartus II Software
- Altera De2-115 board

Circuit Diagrams

Screenshot of Schematic Diagram 5.5 Part 1

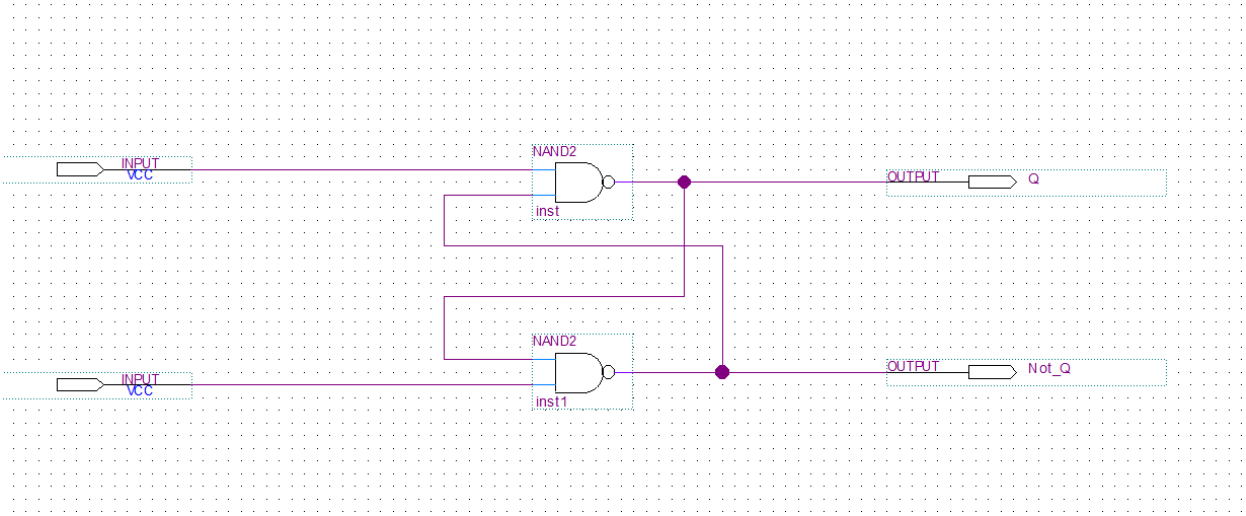

Figure 1: SR Latch build from two NAND gates

Screenshot of Schematic Diagrams 5.5 Part 2

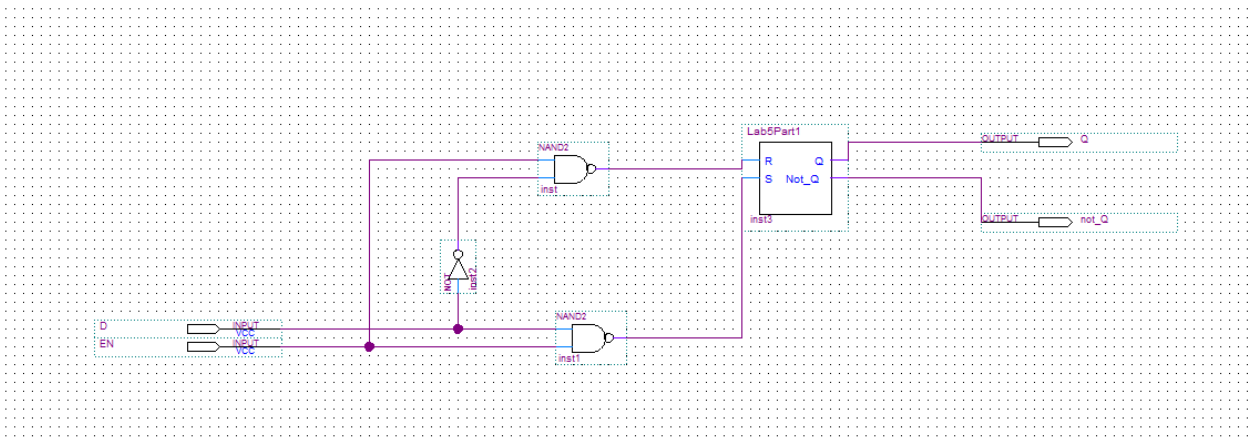

Figure 2: D Latch Circuit

Screenshot of Schematic Diagrams 5.5 Part 3

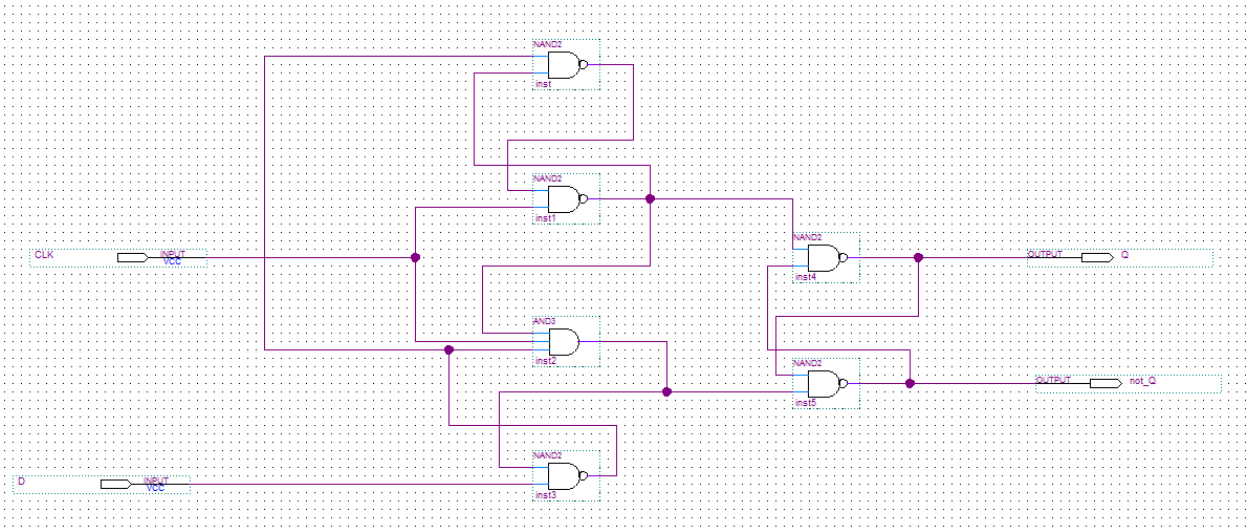

Figure 3: D Flip-Flop Circuit

Screenshot of Schematic Diagrams 5.5 Part 4

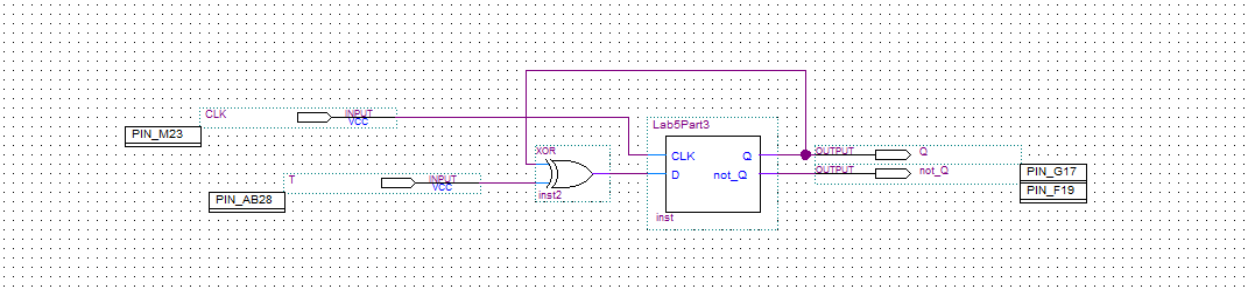

Figure 4: T Flip-Flop Circuit

Experiment Data and Data Processing

Screenshot of Simulation 5.5 Part 1

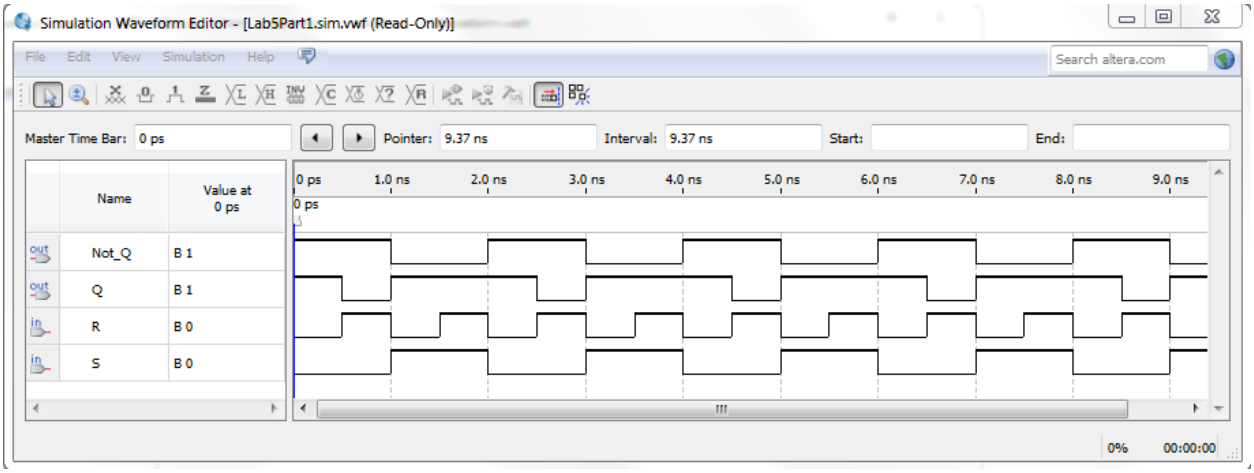

Figure 5: Simulation Output Waveform

Screenshot of Simulation 5.5 Part 2

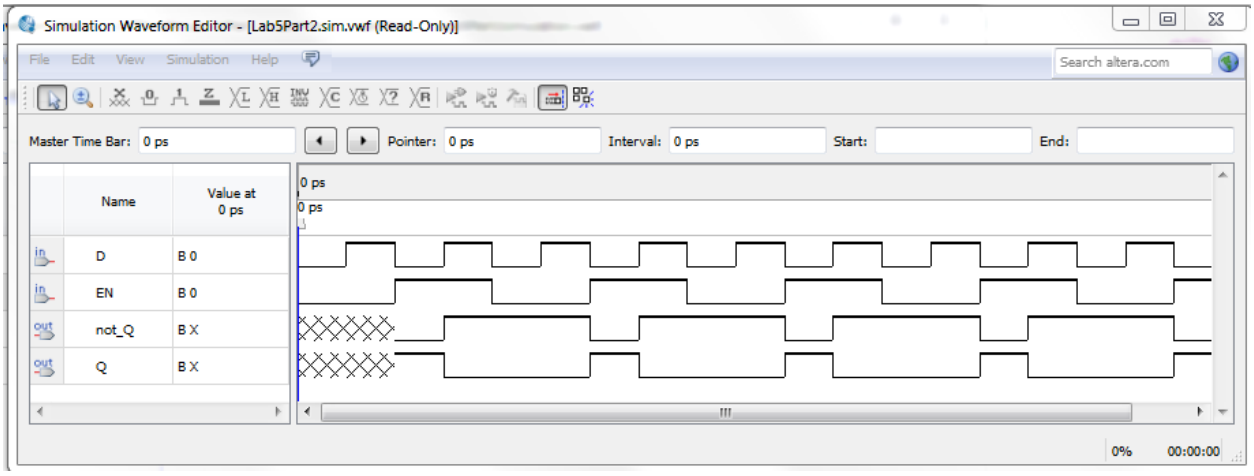

Figure 6: Simulation Output Waveform

Screenshot of Simulation 5.5 Part 3

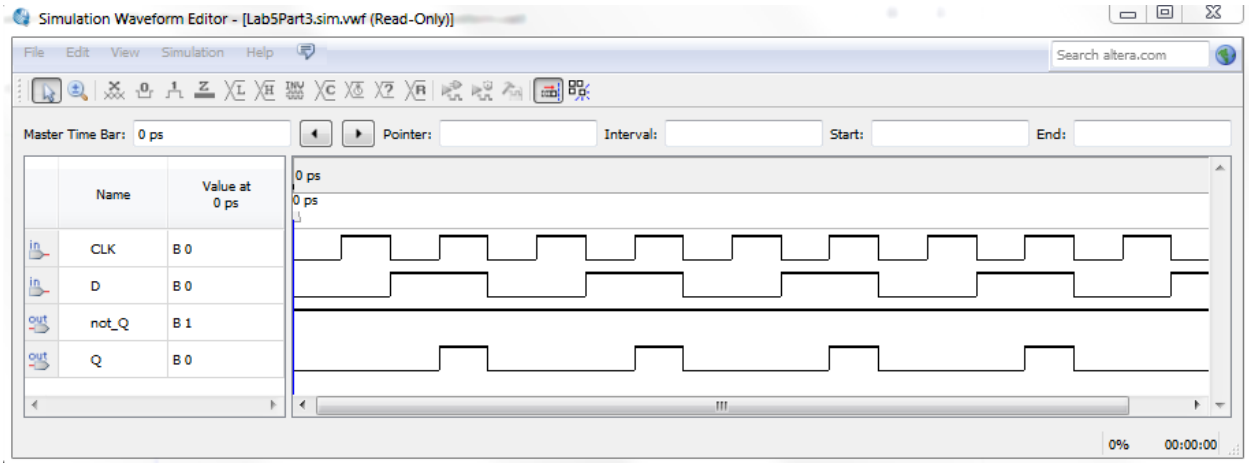

Figure 7: Simulation Output Waveform

Screenshot of Simulation 5.5 Part 4

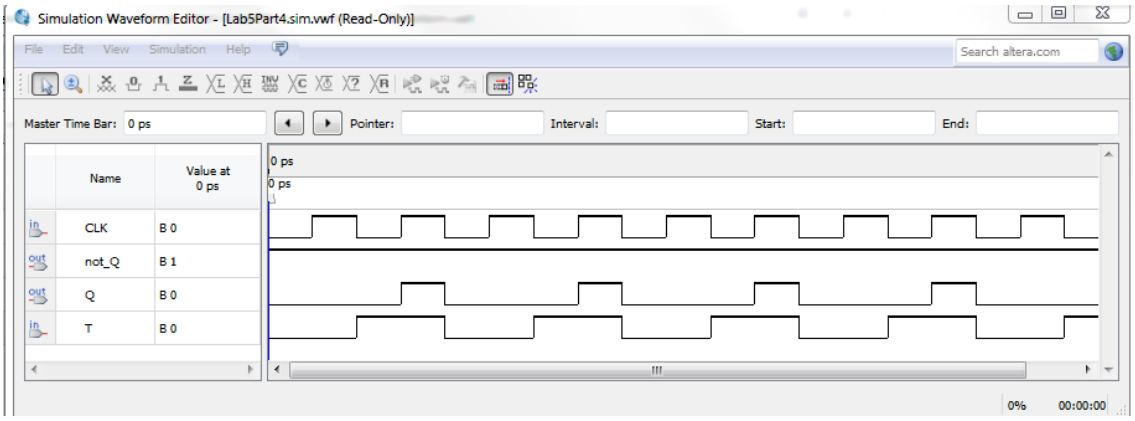

Figure 8: Simulation Output Waveform

Tables

Table 1: Experimental Data from Altera DE2-115 board 5.5 Part 1

Input From Switches/Buttons		Output From Board	
R	S	Q	Not_Q
0	0	1	1
1	0	0	1
0	1	1	0
1	1	1	0

Table 2: Experimental Data from Altera DE2-115 board 5.5 Part 2

Input From Switches/Buttons		Output From Board	
D	En	Q	Not_Q
0	0	/	/
1	0	/	/
0	1	1	0
1	1	0	1
0	0	0	1
1	0	0	0
0	1	1	0
1	1	0	1
0	0	0	1
1	0	0	1
0	1	1	0
1	1	0	1

Table 3: Experimental Data from Altera DE2-115 board 5.5 Part 3

Input From Switches/Buttons		Output From Board	
CLK	T	Q	Not_Q
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	1

Table 4: Experimental Data from Altera DE2-115 board 5.5 Part 4

Input From Switches/Buttons		Output From Board	
CLK	S	Q	Not Q
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	1

Discussion

Summary of Objectives

In lab 5 we studied sequential circuits. A sequential circuit is digital circuit whose output depends not only on the present combination of input, but also on the history of the circuit. Sequential circuit element is a basic memory element that can store 1 bit. There are two basic sequential circuits:

- The latch
- The flip-flop

The two types have on difference and that is that the condition under which the stored bit changes.

The first part consisted on the simplest sequential circuit element in the SR latch. It presents two asynchronous inputs (SET –that makes the device store a logic 1 and RESET – an input that makes the device store a logic 0) and two complementary outputs, Q and Q that are always in opposite logic states. The SR latch presents two stable states:

- SET or ON when Q =1 and Q = 0
- RESET or OFF when Q = 0 and Q =1

In the second part of the lab, we worked on the D Latch. This latch has two operating modes that are controlled by the ENABLE input. The latch stores the data that was present when EN was last active.

In part 3 of the lab, we worked on the D Flip-Flop. The flip-flop output changes when its CLOCK input detects an edge. The sequential circuit element is edge-sensitive.

Part 4 of the lab, we worked with a T Flip-Flop whose output toggles between HIGH and LOW on each clock pulse when input T is active. We constructed a T flip-flop can be constructed using a D Flip-Flop.

The Quartus software was successfully used by following the instructions in the lab manual and prior knowledge.

Overall the lab was successful as the main objectives were accomplished. Mainly:

- Build latches and flip-flops from basic gates
- Provide insight to latching and edge triggering
- Test latches and flip-flops to understand their functionality

Conclusion

The results outputted by the Altera board evidently indicated that the circuits were assembled and tested correctly and met the expected outputs. Therefore we can come to the conclusion that our knowledge of latches and flip-flops has depth and the Altera board was outputting precise results for the circuits constructed. The steps stated in the lab manual were correctly and chronologically followed to complete the lab with maximum efficiency and therefore the experiment outputted the best results.