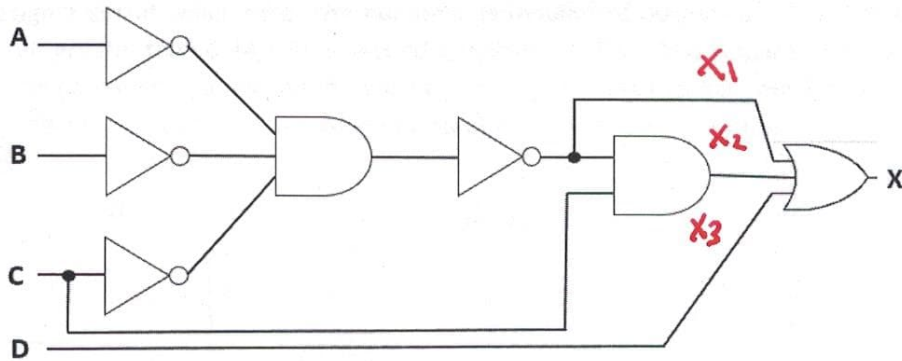


Question 1) (5 marks)

The following circuit is put forward from your design team. Having taken ELEC 2607 you know for a fact that the circuit can be greatly simplified.



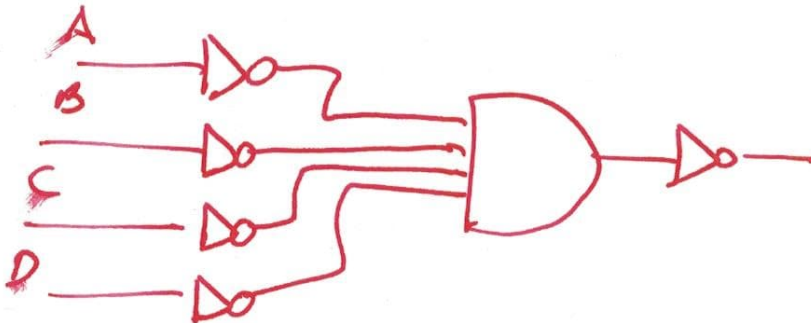
- a) Express the output X as the Boolean expression determined directly from the circuit. (Do not simplify or convert here. Just get the function for X as indicated by the combinational circuit.) (1 mark)

$$\begin{aligned}
 X_1 &= \overline{A} \overline{B} \overline{C} & F &= X_1 + X_2 + X_3 \\
 X_2 &= X_1 C & F &= \overline{A} \overline{B} \overline{C} + X_1 C + D \\
 X_3 &= D
 \end{aligned}$$

- b) Apply DeMorgan's theorem, Boolean algebra, ... and simplify your expression for X determined in part a). Indicate in the right-hand side the simplification rule(s) being used in EACH step. (2 marks)

$$\begin{aligned}
 F &= (A + B + C) + \overline{A} \overline{B} \overline{C} C + D && \text{DeM} \\
 F &= A + B + C + (A + B + C) C + D && \text{DeM} \\
 F &= A + B + C + D && \text{Simplification}
 \end{aligned}$$

- c) Draw the simplified circuit using only AND Gates and inverters. (2 marks)



Question 2) (5 marks)

Two 2 bit binary numbers expressed in two's complement form, $A = (A_1A_0)$, $B = (B_1B_0)$, are to be compared. You are to design a circuit which takes the numbers as inputs and outputs a "1" ($Z = 1$) if the decimal equivalent of A is greater than B, ($A > B$). A second output of "1" ($W = 1$) is required if A equals B, ($A = B$). You must use the Karnaugh map approach to solve this problem and express your Boolean expression in Sum of Product form. Draw your circuit using two level AND-OR implementation.

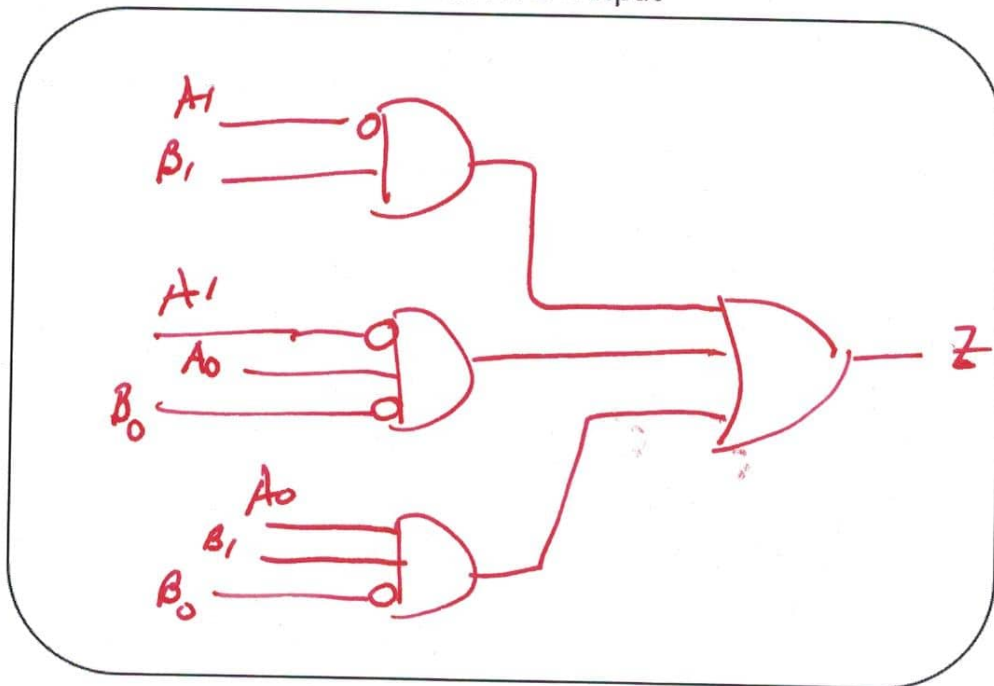
		B_1B_0		Z		
		00	01	11	10	
0	A_1A_0	00	0	0	1	1
	01	1	0	1	1	
1	A_1A_0	11	0	0	0	1
	10	0	0	0	0	
		0	1	-1	-2	

$$z = \bar{A}_1 B_1 + \bar{A}_1 A_0 \bar{B}_0 + A_0 B_1 \bar{B}_0$$

		B_1B_0		W	
		00	01	11	10
0	A_1A_0	00	1	0	0
	01	0	1	0	0
1	A_1A_0	11	0	1	0
	10	0	0	0	1

$$w = \bar{A}_1 \bar{A}_0 B_1 \bar{B}_0 + \bar{A}_1 A_0 B_1 \bar{B}_0 + A_1 A_0 B_1 + A_1 \bar{A}_0 B_1 \bar{B}_0$$

Your circuit for Z Output



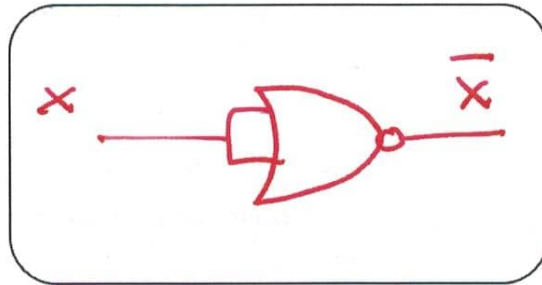
Question 3) (3 marks)

The NOR gate is considered as a universal gate in which all other gates can be constructed from.

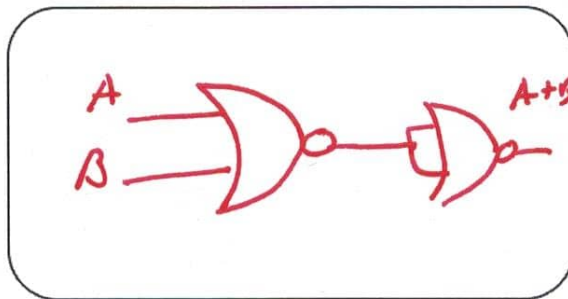
Using NOR gates only construct the following gates:

- i) Inverter (1 mark)
- ii) OR gate (1 marks)
- iii) AND Gate (1 marks)

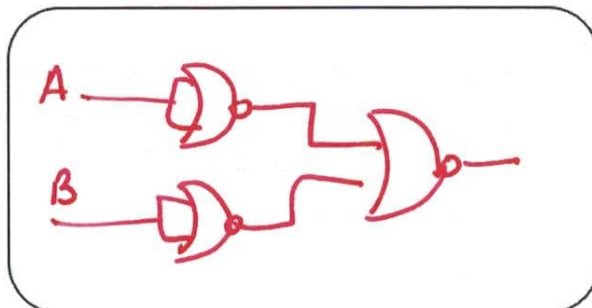
Your Inverter circuit here



Your OR gate circuit here



Your AND gate circuit here



Question 4) (4 marks)

- [1] a) Convert 29.85_{10} (decimal number) into its binary equivalent. Show your work. Place final answer in space provided. Maximum of 6 bits after the binary point.

$$\begin{array}{r} 1110 \\ \underline{1371429} \\ 2 \end{array} \cdot 85 \times 2 \mid 1.7$$

$$\begin{array}{r} .7 \times 2 \mid 1.4 \\ .4 \times 2 \mid 0.8 \\ .8 \times 2 \mid 1.6 \\ .6 \times 2 \mid 1.2 \\ .2 \times 2 \mid 0 \end{array}$$

$$\boxed{11101.110110}$$

$$0.110110 = 0.84375$$

- [1] b) Convert decimal 89_{10} to base 8 (octal). Show your work. Place final answer in space provided.

$$\begin{array}{r} 131 \\ \underline{01189} \\ 8 \end{array}$$

$$\boxed{131}$$

$$(131)_8 = (1 \times 8^2 + 3 \times 8^1 + 1 \times 8^0)_{10} = (89)_{10}$$

- [1] c) Use the least number of bits to perform the following addition in binary for the decimal equivalent $(7 + 3)$ using two's complement notation. Provide your answer in binary. Doing the math in decimal and then converting the final answer to binary gives no points.

$$7 + 3 = 10 \quad [7.5] \rightarrow \boxed{01010} \quad n=5 \leftarrow [0.25]$$

$$\begin{array}{r} 00111 \\ 00011 \\ \hline 01010 \quad (=10 \text{ decimal}) \end{array}$$

$n=4 \quad \text{range} = -8 \text{ to } +7$
 $n=5 \quad \quad \quad = -16 \text{ to } +15$

- [1] d) Use the least number of bits without overflow to perform the following subtraction in binary for the decimal equivalent $(-1 - 7)$ using two's complement addition. Provide your answer in binary. Doing the math in decimal and then converting the final answer to binary gives no points.

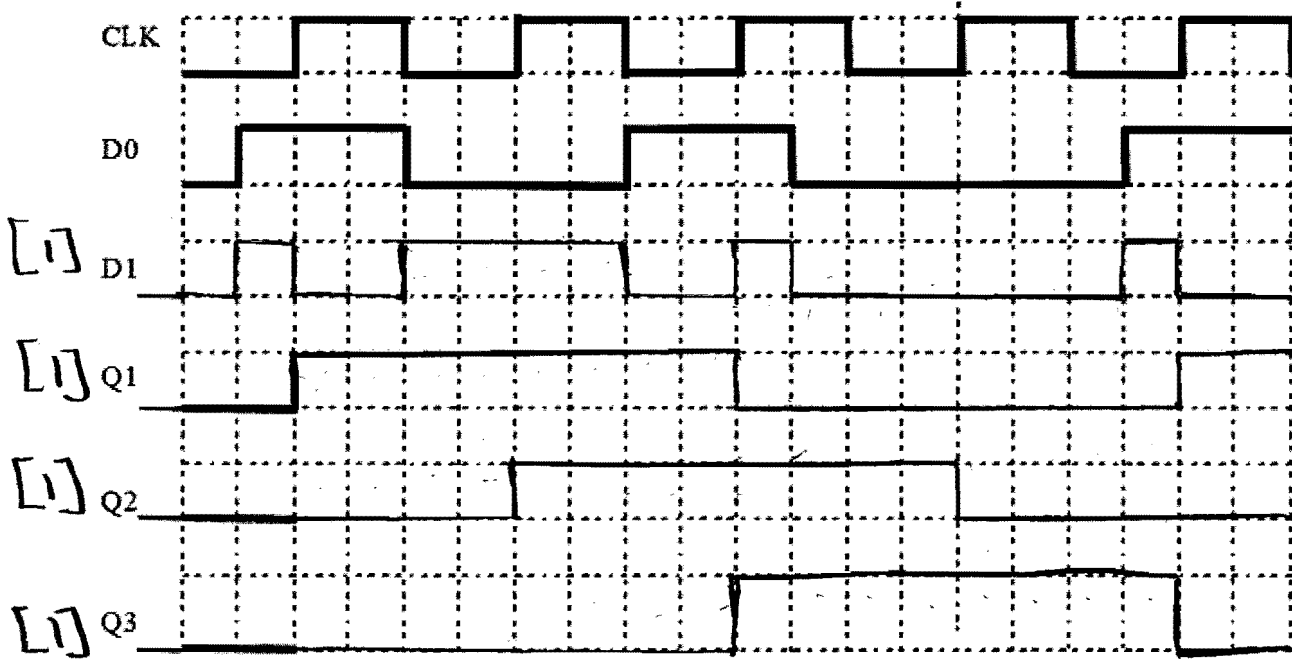
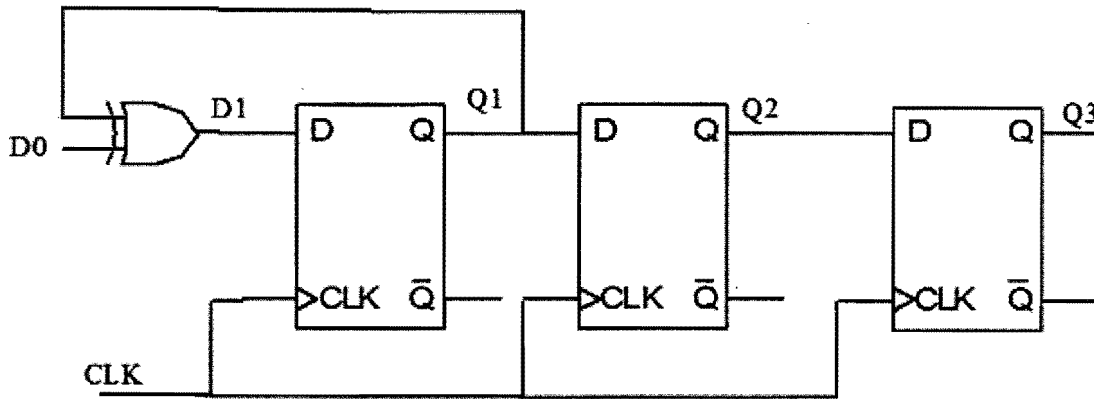
$$[7.5] \rightarrow \boxed{1000} \quad n=4 \leftarrow [0.25]$$

$$\begin{array}{r} 1111 \\ + 1001 \\ \hline 1000 \\ \rightarrow -8 \end{array}$$

$+1 = 0001$
 $-1 = 1111$
 $+7 = 0111$
 $-7 = 1001$

Question 5) (4 marks)

Complete the following timing diagram for D1, Q1, Q2 and Q3. Flip flop outputs are initially reset to zero as shown. Flip flops are rising edge triggered.

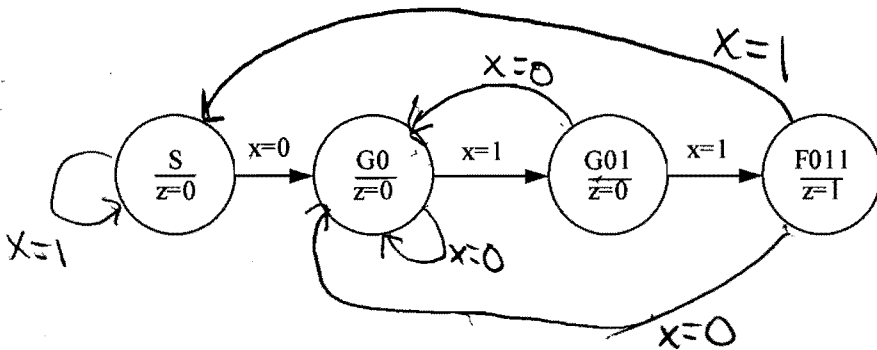


Total 8.5 marks

Question 6) [8 marks]

Complete the given state graph for a "011" non-overlapping sequence detector then complete the state table and implementation.

This is a Mealy / Moore machine. (circle correct answer)



5 x 1/2 = 2.5 marks

Present State	Next State		Output
	D ₁ D ₀ (x=0)	D ₁ D ₀ (x=1)	
Q ₁ Q ₀ S=00	01	00	0
G ₀ =01	01	11	0
G ₀₁ =11	01	10	0
F ₀₁₁ =10	01	00	1

[1]

Q ₁ Q ₀ \ X	0	1
00	0	0
01	0	1
11	0	1
10	0	0

D₁ = Q₀X

[1]

Q ₁ Q ₀ \ X	0	1
00	1	0
01	1	1
11	1	0
10	1	0

D₀ = $\bar{X} + \bar{Q}_1 Q_0$

[1]

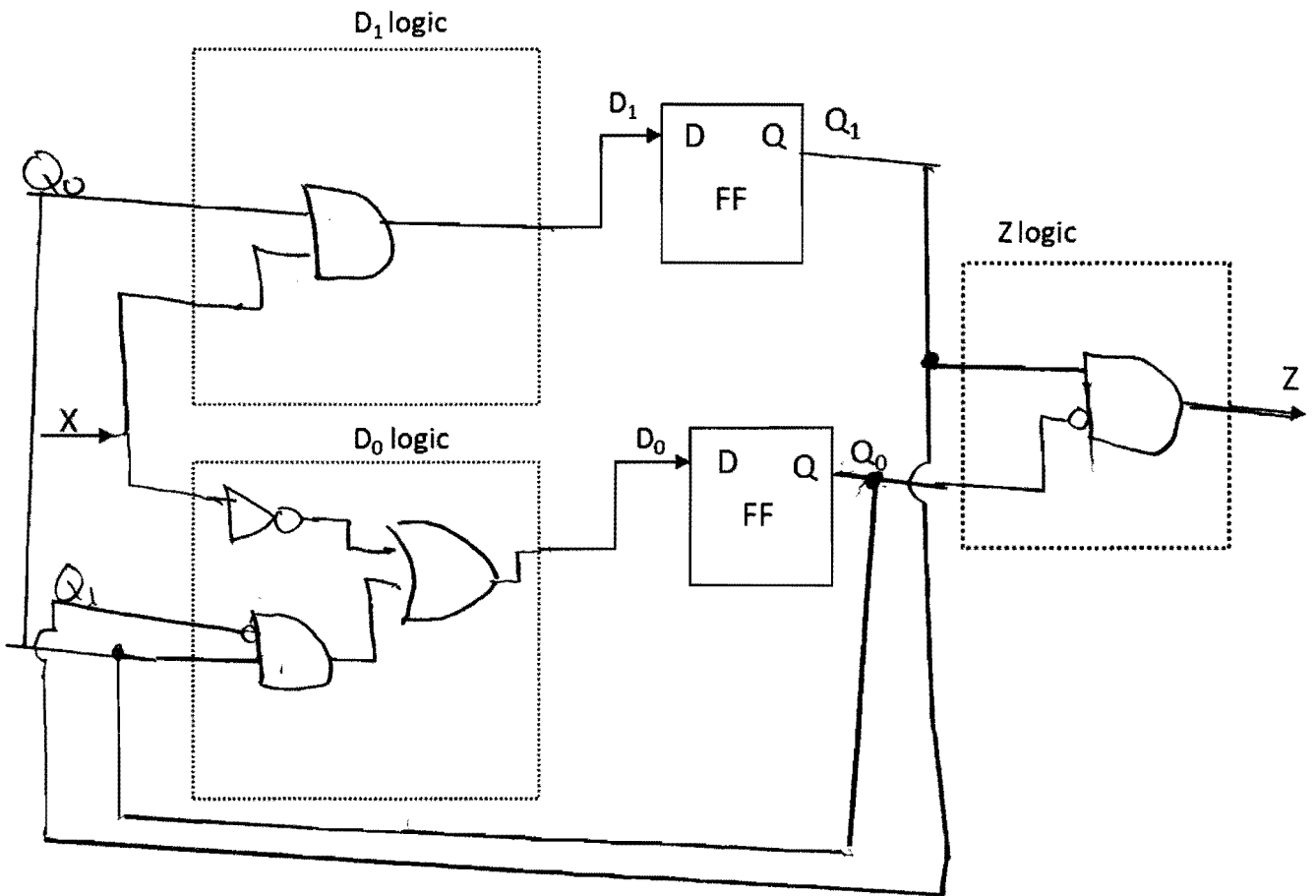
Q ₁ \ Q ₀	0	1
0	0	0
1	1	0

Z = Q₁Q₀

[1]

[1]

Complete the circuit for the "011" sequence detector. Clock and reset are assumed inputs and are not required. Clearly show all logic gates and wiring.



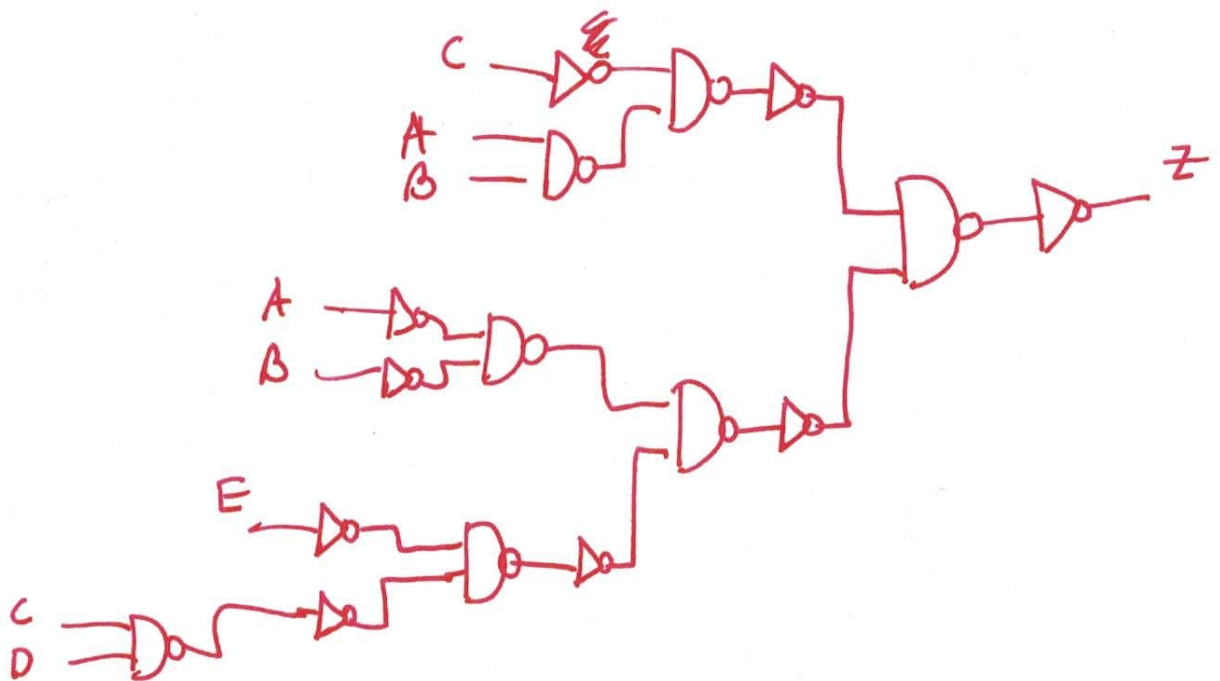
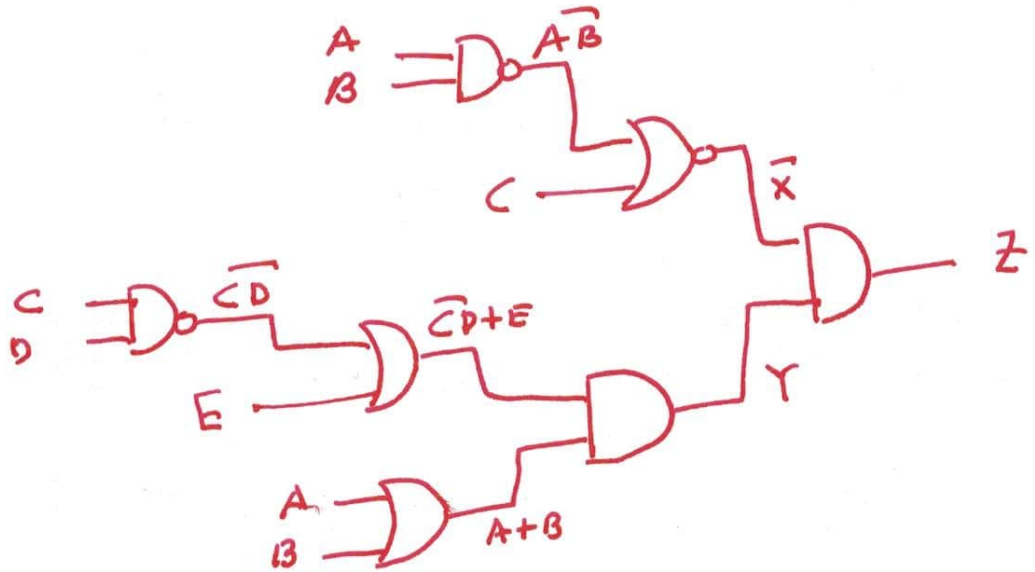
Question 7) (4 marks)

The following expressions are used to provide the final output (Z). Draw the circuit for the output Z as dictated by the expressions (Do not simplify expressions) (1 mark). THEN convert the circuit to its standard NAND gate representation. Inverters are allowed but gate inputs should have no bubbles.

$$X = \overline{AB} + C$$

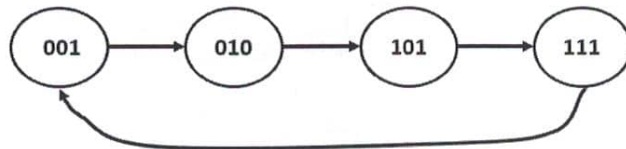
$$Y = (A + B)(\overline{CD} + E)$$

$$Z = \overline{XY}$$



Question 8) (7 marks)

A finite state machine (FSM) is characterized by the state diagram given below. The states of the "D" flip flops are designated as $Q_2 Q_1 Q_0$ (in that order). This is an irregular counter which counts $1 \rightarrow 2 \rightarrow 5 \rightarrow 7 \rightarrow 1$ and repeats forever. As a failsafe for your counter, all unused states should have next state 010. Fill in the state table for the counter (2 marks). From the table produce the Karnaugh maps for the flip-flop "D" inputs looping "1" in the map (3 marks). Draw the completed circuit using falling edge triggered "D" flip-flops. (2 marks)



Present State	Next State
Q_2, Q_1, Q_0	Q_2+, Q_1+, Q_0+
000	0 1 0
001	0 1 0
010	1 0 1
011	0 1 0
100	0 1 0
101	1 1 1
110	0 1 0
111	0 0 1

D_2

$D_2 = \bar{Q}_2 Q_1 \bar{Q}_0 + Q_2 \bar{Q}_1 Q_0$

D_1

$D_1 = \bar{Q}_1 + \bar{Q}_2 Q_0 + Q_2 \bar{Q}_0$

D_0

$D_0 = Q_2 \bar{Q}_0 + \bar{Q}_2 Q_1 \bar{Q}_0$

$$D_0 = Q_2 \bar{Q}_0 + \bar{Q}_2 Q_1 \bar{Q}_0$$

Question 8) continue answer here

