Carleton University

Department of Systems and Computer Engineering

SYSC 4507 Winter 2017

Computer Systems Architecture

Assignment # 2 Solution and marking guidelines for TAs

The assignment is marked out of 100 marks

1. **[60 marks]** Consider a set associative cache that can hold eight blocks of main memory in each set, a 17-bit tag field for each cache line, and has been designed for a 4 GByte main memory that is organized into 16-byte blocks. Assume that the word length is 1 byte.

a) **[10 marks]** This is a k-way set associative cache. What is k in this example?

Cache set can hold 8 blocks of main memory → 8 blocks/set. Therefore, k = 8

b) **[10 marks]** Draw a box to represent a memory address (as done in class), and divide the box into the fields that are relevant to the operation of this cache. Label each field, and clearly indicate the number of bits in each field.

Tag = 17 bits
16-byte blocks = 2^4 bytes/block → 4 word bits
4 GByte memory: = 2^32 Bytes → 32-bit addresses
set bits = 32 – 17 – 4 = 11 bits

Marking: 6 mark for diagram + labels
3 mark for "4" word bits
1 mark for set bits

c) **[10 marks]** What is the size (in bytes) of the cache?

8 blocks / set * 16 bytes / block = 2^3 * 2^4 bytes/ set = 2^7 bytes / set

2^11 sets * 2^7 bytes / set = 2^18 bytes = 256 KBytes

d) **[30 marks]** Suppose that the tag stored in line number 16 of the cache contains the hexadecimal value 3D (assume as many leading 0's as needed). State an address (in hexadecimal) that will cause a cache hit for the second word in line number 16 of the cache. Assume that cache line numbers start at 0 and are allocated to sets linearly. Assume that set 0 starts with cache line 0.

Set 0 contains lines 0 – 7
Set 1 contains lines 8 – 15
Set 2 contains line 16

Tag = 3D H = 11 1101 (17 bit binary value, leading 0's)
Set = 2 = 00000000010 (11 bit binary value)
Word bits won't matter to hit the line … assume word bits = 0000 binary (but could use any value)

Address: 11 1101 00000000010 0000 binary
Re-arrange as hex:
1 1110 1000 0000 0010 0000 binary = 1E8020 H

Marking: they need to state a binary address first, and then convert to hex

10 marks for word bits matching the answer given in b)
They can get this wrong and still get the remaining marks
10 mark for set & number of bits matches the answer given in b)
They can get this wrong and still get the remaining marks
5 marks for tag bits
5 marks for resulting binary address to hex address

2. **[40 marks]** Suppose there is a memory hierarchy in which the cache access time is 2 ns, main memory access time is 60 ns, and secondary storage access time is 12 ms. When a program is executed, it is found that 85% of the cache accesses result in hits, and 94% of the main memory accesses result in hits. What is the effective access time of the (complete) memory hierarchy for this program?

Solution:
Tc = 2 ns, Hc = 0.85, Tm = 60 ns, Hm = 0.94, Ts = 12ms
The average access time for main memory and secondary storage is :
TA = Hm*Tm + (1-Hm)*Ts

The effective access time of the complete memory hierarchy is :
= Hc*Tc + (1-Hc)*TA = 0.85*2ns + (0.15)*[0.94*60 ns + 0.06*12ms] = 108010.16 ns

Marking: **They might use the approach above, in which case:**

20 marks for main/secondary average access time
20 marks for cache/ (main/secondary) hierarchy

There are several ways to arrive at the answer … any way that makes sense is OK.
e.g. they might do all 3 levels at once.