

Concordia University Department of Software Engineering Winter 2015

SOEN 228 Practice Problem Set #2

These problems focus on design and implementation of combinational and sequential digital circuits, Boolean Minimization and binary representation of integers.

Problem 1) Design a four bit register with the following features:

- 1) The register can receive data in parallel (i.e. each flip flop in the register can receive a single bit (not the same bit) at the same time from an outside source).
- 2) The register can hold the data until otherwise required.
- 3) The register can shift the bits to the left (bit 1 moves to the location of bit zero, bit 2 moves to the location of bit 1 and bit 0 is lost).
- 4) The register can shift the bits to the right (bit 0 moves to the location of bit 1, bit 1 moves to the location of bit 2, the right most bit is lost).

You should use D-Flip flops and multiplexers in your design. Clearly label your nodes and components.

Problem 2) For each of the cases below design a circuit that will produce a true output if the bit sequence 1011 is entered:

- 1) In parallel (four input bits entered at the same time on four separate wires (e.g. inputs A, B, C and D))
- 2) In series (one input bit at a time, four time cycles to enter entire sequence). This will require a finite state machine (i.e. a sequential circuit) with input "In" and it will take four clock cycles to cover the entire sequence where one value of the sequence is read each clock cycle.

Problem 3) Use Boolean algebra to simplify the following expressions (obtain the minimum number of littorals)

- i) $\overline{AB}(AB + CD)$
- ii) $(A + B)(A + \overline{B})$
- iii) $AB + \overline{A}C + BC$
- iv) $(A + B)(\overline{A} + C)(B + C)$
- v) $A + \overline{A}B$

Problem 4)

An unknown component has the following truth table.

IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

The unknown component (the rectangular box in the circuit below) is part of a combinational logic circuit shown in Figure 1 which consists of one instance of this “mystery component” and a two input AND gate. The circuit has four inputs: MICK, KEITH, CHARLIE and BILL and one output STONES. (Shown below)

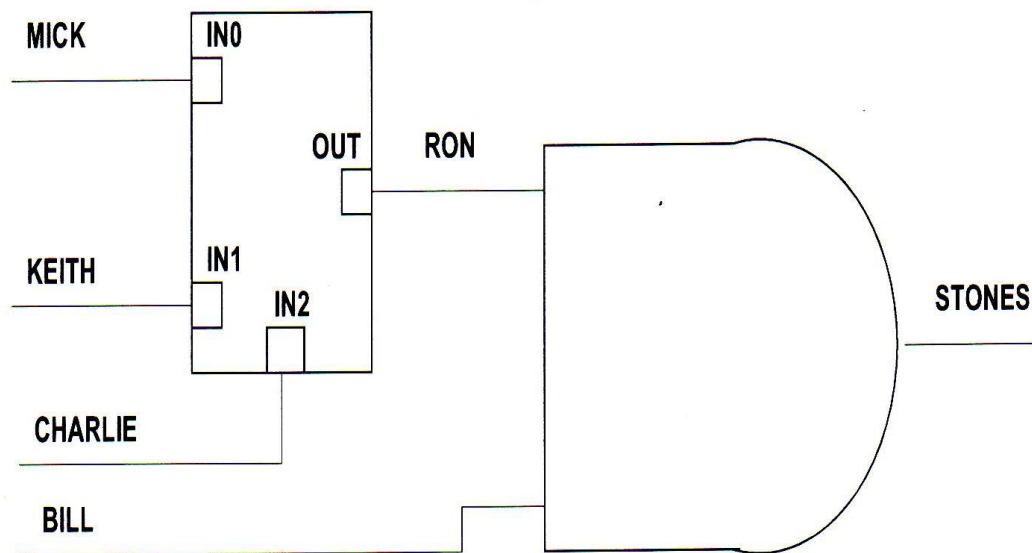


Figure 1: A circuit consisting of a “mystery component” with an AND gate.

You are to fill out the truth table below, where the response is based on the circuit in figure 1.

Truth Table for circuit in figure 1

MICK	KEITH	CHARLIE	BILL	RON	STONES
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0		
0	0	1	1		
0	1	0	0	0	
0	1	0	1	0	
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0		
1	1	1	1		

Problem 5)

Consider the circuit shown in the figure below which consists of a **positive edge triggered** flip-flop with selective load capability (identified as MICK) and a **level sensitive D-type latch** (labelled as KEITH). There is an input bus (consisting of a single wire) , an output bus, and two tri-state buffers. Complete the timing diagram which is included at the end of this question. Indicate in the provided timing diagram the behavior of the output of the flip-flop and the latch (q_mick and q_keith) as well as the behavior of the output bus between the indicated “start” and “end” times. Use the symbol “Z” to denote the state of the output bus when it is in the high-impedance (tri-state value). In the given diagram, it is assumed that the initial value of q_mick is logic ‘0’ and that the initial value of q_keith is logic ‘1’. Note also that the timing diagram intentionally contains a fatal design error. You are to explain in words the nature of this design

error. Use the word “FIRE” in the appropriate place in the timing diagram to indicate the state of the output bus at the interval in time during which the design error occurs.

