Question 1: **(15marks)**

Use Algebraic manipulation to proof that:

$$\bar{x}_1\bar{x}_3 + x_2x_3 + x_1\bar{x}_2 = \bar{x}_1x_2 + x_1x_3 + \bar{x}_2\bar{x}_3$$

Hint: proof that the truth table for LHS and RHS are equal.

Solution:

Using the fact that $x + \bar{x} = 1$ (Theorem 8*b*), we can manipulate the left-hand side as follows:

$$\begin{aligned}\text{LHS} &= \bar{x}_1\bar{x}_3 + x_2x_3 + x_1\bar{x}_2 \\ &= \bar{x}_1(x_2 + \bar{x}_2)\bar{x}_3 + (x_1 + \bar{x}_1)x_2x_3 + x_1\bar{x}_2(x_3 + \bar{x}_3) \\ &= \bar{x}_1x_2\bar{x}_3 + \bar{x}_1\bar{x}_2\bar{x}_3 + x_1x_2x_3 + \bar{x}_1x_2x_3 + x_1\bar{x}_2x_3 + x_1\bar{x}_2\bar{x}_3\end{aligned}$$

These product terms represent the minterms 2, 0, 7, 3, 5, and 4, respectively.

For the right-hand side we have

$$\begin{aligned}\text{RHS} &= \bar{x}_1x_2 + x_1x_3 + \bar{x}_2\bar{x}_3 \\ &= \bar{x}_1x_2(x_3 + \bar{x}_3) + x_1(x_2 + \bar{x}_2)x_3 + (x_1 + \bar{x}_1)\bar{x}_2\bar{x}_3 \\ &= \bar{x}_1x_2x_3 + \bar{x}_1x_2\bar{x}_3 + x_1x_2x_3 + x_1\bar{x}_2x_3 + x_1\bar{x}_2\bar{x}_3 + \bar{x}_1\bar{x}_2\bar{x}_3\end{aligned}$$

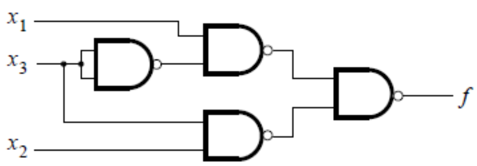
These product terms represent the minterms 3, 2, 7, 5, 4, and 0, respectively. Since both expressions specify the same minterms, they represent the same function; therefore, the equation is valid. Another way of representing this function is by $\sum m(0, 2, 3, 4, 5, 7)$.

Question 2: (15 marks)

Design the simplest circuit that implements the function f (x_1, x_2, x_3) = ∑ M (3,4,6,7) using NAND gates.

Solution:

The minimum-cost SOP expression for the function f(x1; x2; x3) = Pm(3; 4; 6; 7) is:
f = x1x3'+ x2x3
The corresponding circuit implemented using NAND gates is



Q3: (25 marks)

Consider the circuit in Figure 1 which implements functions f and g. What is the cost of this circuit, assuming that the input variables are available in both true and complemented forms? Redesign the circuit to implement the same functions, but at as low a cost as possible. What is the cost of your circuit.

Solution:

The cost of the circuit in Figure P4.2 is 11 gates and 30 inputs, for a total of 41. The functions implemented by the circuit can also be realized as

$$
\begin{aligned}
f &= \overline{x}_1\overline{x}_2\overline{x}_4 + x_2\overline{x}_3\overline{x}_4 + \overline{x}_1x_3x_4 + x_1x_4 \\
g &= \overline{x}_1\overline{x}_2\overline{x}_4 + x_2\overline{x}_3\overline{x}_4 + \overline{x}_1x_3x_4 + \overline{x}_2x_4 + x_3\overline{x}_4
\end{aligned}
$$

The first three product terms in f and g are the same; therefore, they can be shared. Then, the cost of Implementing f and g is 8 gates and 24 inputs, for a total of 32.

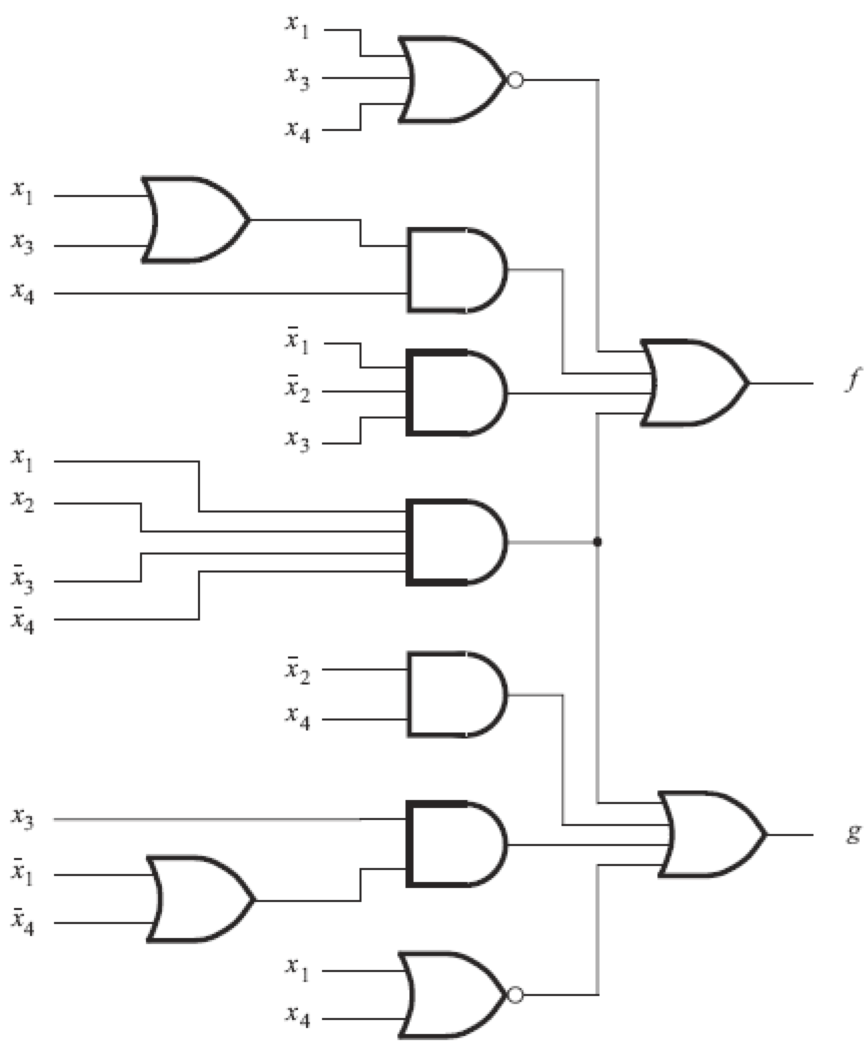


Fig 1

Q4: for the circuit shown in Fig 2, define f………………(20 marks)

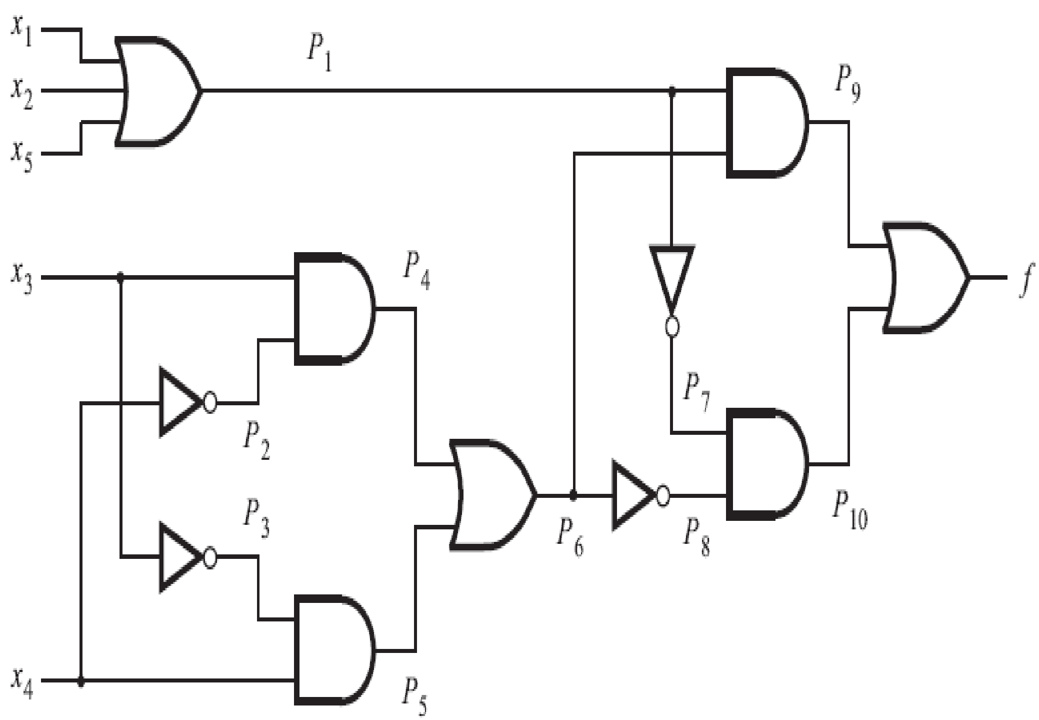


Fig 2

Solution:

$P9 = P1P6$
$P10 = P7P8$

We can derive *f* by tracing the circuit from the output towards the inputs as follows

$$
\begin{aligned}
f &= P_9 + P_{10} \\
&= P_1 P_6 + P_7 P_8 \\
&= (x_1 + x_2 + x_5)(P_4 + P_5) + \overline{P}_1 \overline{P}_6 \\
&= (x_1 + x_2 + x_5)(x_3 P_2 + x_4 P_3) + \overline{x}_1 \overline{x}_2 \overline{x}_5 \overline{P}_4 \overline{P}_5 \\
&= (x_1 + x_2 + x_5)(x_3 \overline{x}_4 + x_4 \overline{x}_3) + \overline{x}_1 \overline{x}_2 \overline{x}_5 (\overline{x}_3 + \overline{P}_2)(\overline{x}_4 + \overline{P}_3) \\
&= (x_1 + x_2 + x_5)(x_3 \overline{x}_4 + \overline{x}_3 x_4) + \overline{x}_1 \overline{x}_2 \overline{x}_5 (\overline{x}_3 + x_4)(\overline{x}_4 + x_3) \\
&= x_1 x_3 \overline{x}_4 + x_1 \overline{x}_3 x_4 + x_2 x_3 \overline{x}_4 + x_2 \overline{x}_3 x_4 + x_5 x_3 \overline{x}_4 + x_5 \overline{x}_3 x_4 + \\
&\quad \overline{x}_1 \overline{x}_2 \overline{x}_5 \overline{x}_3 \overline{x}_4 + \overline{x}_1 \overline{x}_2 \overline{x}_5 x_4 x_3
\end{aligned}
$$

Q5: (20 marks)

Figure 3 presents the structure of a hierarchical carry-lookahead adder. Show the complete circuit for a four-bit version of this adder, built using 2 two-bit blocks.

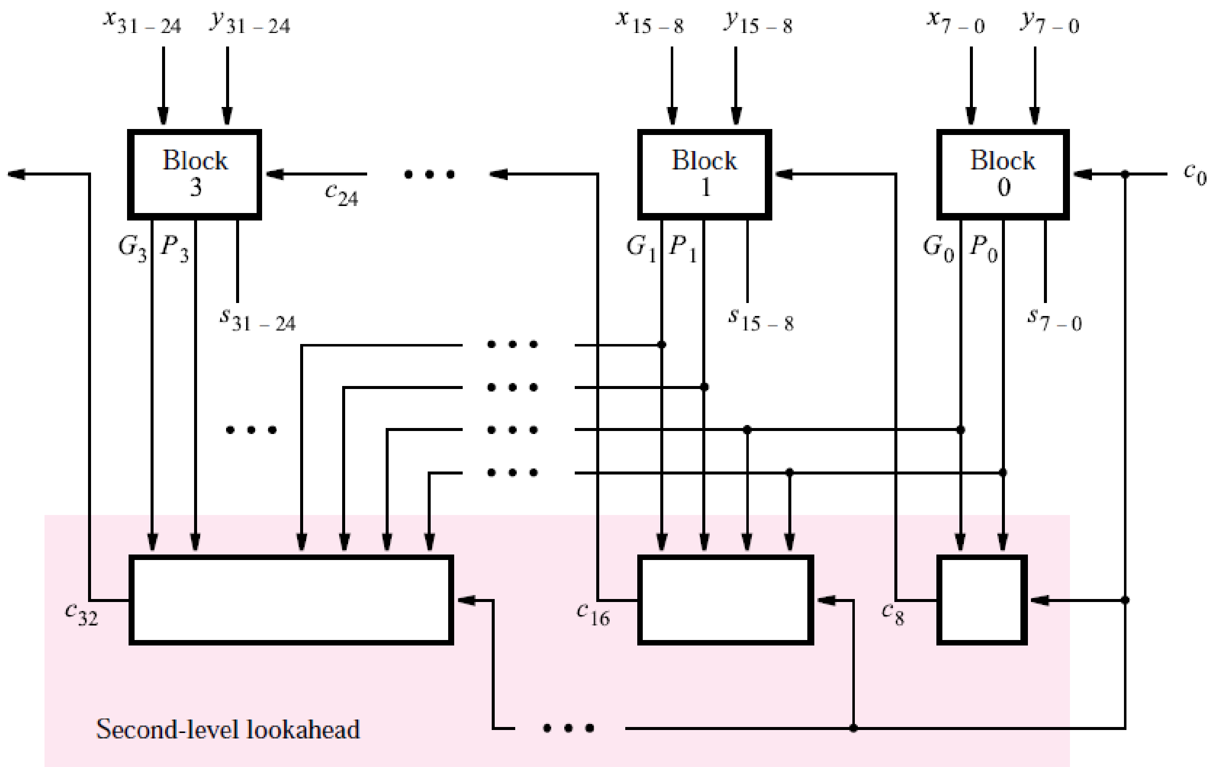
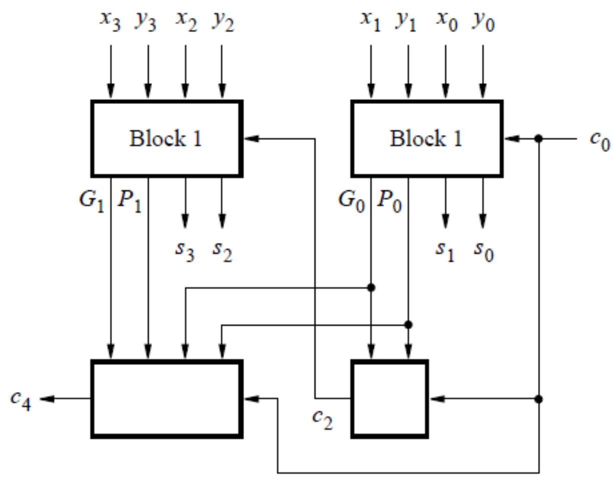


Fig.3

Solution:

5.14. The circuit for a 4-bit version of the adder based on the hierarchical structure in Figure 5.18 is constructed as follow :



Blocks 0 and 1 have the structure similar to the circuit in Figure 5.16. The overall circuit is given by the expressions

$$
\begin{aligned}
p_i &= x_i + y_i \\
g_i &= x_i y_i \\
P_0 &= p_1 p_0 \\
G_0 &= g_1 + p_1 g_0
\end{aligned}
$$

$$
\begin{aligned}
P_1 &= p_3 p_2 \\
G_1 &= g_3 + p_3 g_2 \\
c_2 &= G_0 + P_0 c_0 \\
c_4 &= G_1 + P_1 G_0 + P_1 P_0 c_0
\end{aligned}
$$