Université d'Ottawa
Faculté de génie

École d'ingénierie et de
technologie de l'information

uOttawa

L'Université canadienne
Canada's university

University of Ottawa
Faculty of Engineering

School of Information
Technology and Engineering

# CEG2136: Computer Architecture I
# CEG2536: Architecture des Ordinateurs I

## MIDTERM EXAMINATION

**Profs. V. Groza and W. Gueaieb**

**Length of Examination: 1 hour and 20 minutes** **October 19 2009, 10:00**

Name: _____ Signature: _____

SID: _____

**Hand in the exam sheet at the end of the exam.**
**Use the back of the paper when necessary.**

**Notes**

- All students should be aware of the University of Ottawa's policy on academic fraud.
- Closed book exam. Calculators are not allowed.
- Show all your work in detail. Explain all your assumptions and well define the symbols used.
- Untidy answers will not be marked.
- If you finish 10 minutes or less before the due time, remain seated until the end of the exam.

**Exam Record**

Problem 1 _____/ 24 points

Problem 2 _____/ 42 points

Problem 3 _____/ 34 points

Total: _____/ 100 points

CEG2136: Computer Architecture I
October 19 2009

Midterm

Name: _____
Profs. V. Groza and W. Gueaieb

**Problem 1.** (24 points) $A$ and $B$ are 9-bit registers that contain the binary values: $A = 100011101$ and $B = 111110000$.

(12pts) **1.**

| |
|---|
| 12 pts |

(a) (4 pts) A third 9-bit register $R$ is used to store the result of the micro-operation $R \leftarrow A+B$. What will be the binary value in $R$ as well as the two most significant output carries, $c_8$ and $c_9$, of the addition?

(b) (4 pts) If the numbers in $A$ and $B$ are considered unsigned numbers, does $R$ contain the correct result of $A + B$? Justify your answer.

(c) (4 pts) If the numbers in $A$, $B$ and $B$ are considered signed numbers, represented in their 2's complement format, then does $R$ contain the correct result of $A + B$? Justify your answer.

| |
|---|
| 12 pts |

(12^pts) **2.**

(a) (6 pts) If now the micro-operation $R \leftarrow A - B$ is executed, what will be the result stored in $R$ as well as the last two output carries, $c_8$ and $c_9$, of the subtraction?

12 pts

(b) (6 pts) If the numbers in $A$ and $B$ are considered signed numbers, represented in their 2's complement format, does $R$ contain the correct result of the subtraction? Justify your answer.

12 pts

12 pts

**Problem 2.** (42 points) In this problem, you will desgin a 3-bit ALU to perform the micro-operations described in Table 1. The ALU takes its operands from two 3-bit registers $A = A_2A_1A_0$ and $B = B_2B_1B_0$, and returns an output $F = F_2F_1F_0$. In the case of arithmetic operations, assume that the contents of $A$ and $B$ are signed numbers in 2's compelement representation.

Table 1: Function table of a 3-bit ALU.

| Selection $S_2$ | $S_1$ | $S_0$ | Operation | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | $F = A - 1$ | Decrement by 1 (Décrémentation par 1) |
| 0 | 0 | 1 | $F = A - B$ | Subtruction (Soustraction) |
| 0 | 1 | 0 | $F = A - 2$ | Decrement by 2 (Décrémentation par 2) |
| 0 | 1 | 1 | $F = A - B - 1$ | Subtraction with borrow (Soustraction avec emprunt) |
| 1 | 0 | 0 | $F = \overline{A} \vee B$ | Logic implication (Implication logique) |
| 1 | 0 | 1 | $F = A \oplus B$ | Comparison (Comparaison) |
| 1 | 1 | 0 | $F = cir\ A$ | Circular shift right (Décalage circulaire à droite) |
| 1 | 1 | 1 | $F = ashl\ A$ | Arithmetic shift left (Décalage arithmétique à gauche) |

(13 pts) **1. Design of arithmetic unit**

(a) (10 pts) Draw a detailed logic circuit of the ALU's arithmetic unit.

13 pts

(b) (3 pts) A Boolean variable $W$ is set to 1 when an overflow occurs and is reset to 0 otherwise. Find a simplified Boolean expression of $W$.

13 pts

(8pts) **2. Design of logic unit**

Draw a detailed logic circuit of the ALU's logic unit.

| |
|---|
| 8 pts |

(11pts) **3. Design of shift unit**

(a) (8 pts) Draw a detailed logic circuit of the ALU's shift unit.

| |
|---|
| 11 pts |

(b) (3 pts) A Boolean variable $V$ is set to 1 when an overflow occurs during the arithmetic shift and is

| |
|---|
| 19 pts |

reset to 0 otherwise. Find a simplified Boolean expression of $V$.

($10^{\text{pts}}$) **4. Finalizing the ALU design**

10 pts

(a) (4 pts) A Boolean variable $T$ is used to determine if one the micro-operations stated in Table 1 caused an overflow. $T$ is set to 1 when an overflow occurs and is reset to 0 otherwise. Find a simplified Boolean expression of $T$. (*Hint:* express $T$ in terms of $W$ and $V$, and possibly other Boolean variables).

(b) (6 pts) Use bloc diagrams of the arithmetic, logic and shifting units in order to draw the bloc diagram of the complete ALU, including the overflow detection bit $T$.

10 pts

**Probleme 3.** (34 points) Figure 1 shows the state diagram of a logic circuit which has a unique one-bit external input $x$.

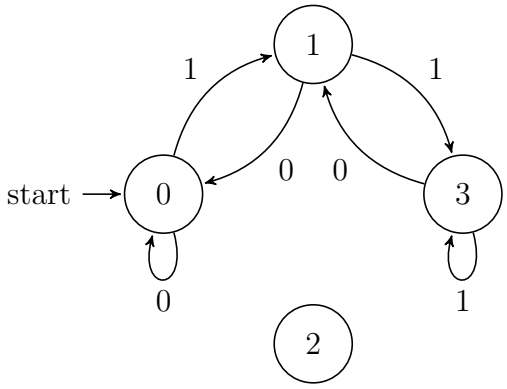


Figure 1: State diagram

(12pts) **1.** Start by deriving the state table of the circuit. Then, assuming that JK flip-flops are to be used in the implementation, extend the state table with the excitation table of the circuit.

12 pts

12 pts

(12pts) **2.** Find simplified expressions for each flip-flop inputs.

| |
|---|
| 12 pts |

(10pts) **3.** Draw the logic circuit using JK flip-flops and the minimum number of simple logic gates (AND/OR/NOT)

| |
|---|
| 10 pts |

| |
|---|
| 22 pts |

| |
|---|
| 0 pts |