



Quiz 2 / Fall 2016

Even

Q1. The two's complement representation of signed numbers is employed in three 10-bit registers A, B and C. Registers A and B carry the following signed numbers: A = 0100010011 and B = 0101100010.

1. Compute $C = B - A$. Show your work in detail. The result is a 10-bit signed number and is stored in the 10-bit register C. What is the content of C after the operation?

$$C = B - A = B + (-A) = 01\ 0110\ 0010 + 2\text{'s compl}(01\ 0001\ 0011) =$$

Carry:	1	1	1	1	1	0	0	0	0	0	
B	0	1	0	1	1	0	0	0	1	0	
-A	1	0	1	1	1	0	1	1	0	1	
C	0	0	0	1	0	0	1	1	1	1	

Verification in decimal:
 =256+64+32+2 = **354**
 =-(01 0001 0011) =-(256+16+2+1) = **-275**
 79

2. Given that 2's complement representation is employed, convert the content of the register C to its equivalent decimal number. Show your work in detail.

In 2's complement representation:

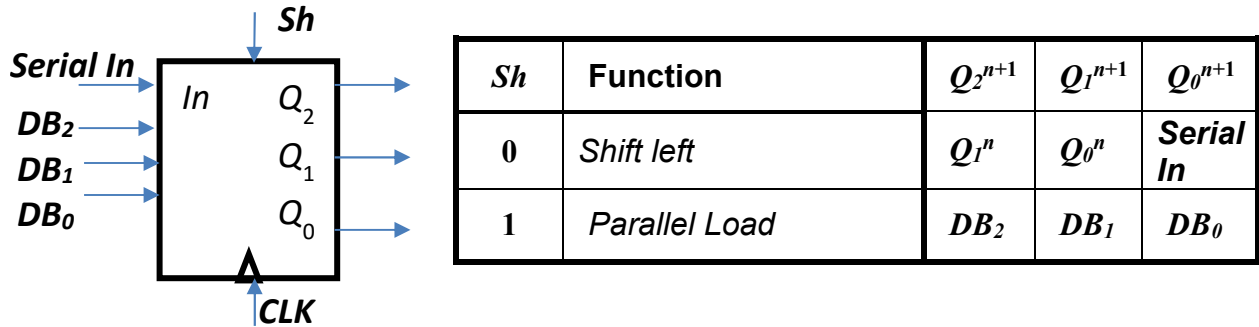
C = 00 0100 1111 represents a positive number (say c) since the msb, the sign bit = 0.

The magnitude of C = 64+8+4+2+1 = 79₁₀

=> C = 79, which is confirmed by performing B-A in decimal

Q2. Design a 3-bit shift left register with parallel load using D flip-flops, as described in the following functional table.

1. Provide the *next state functions* of the D flip-flops



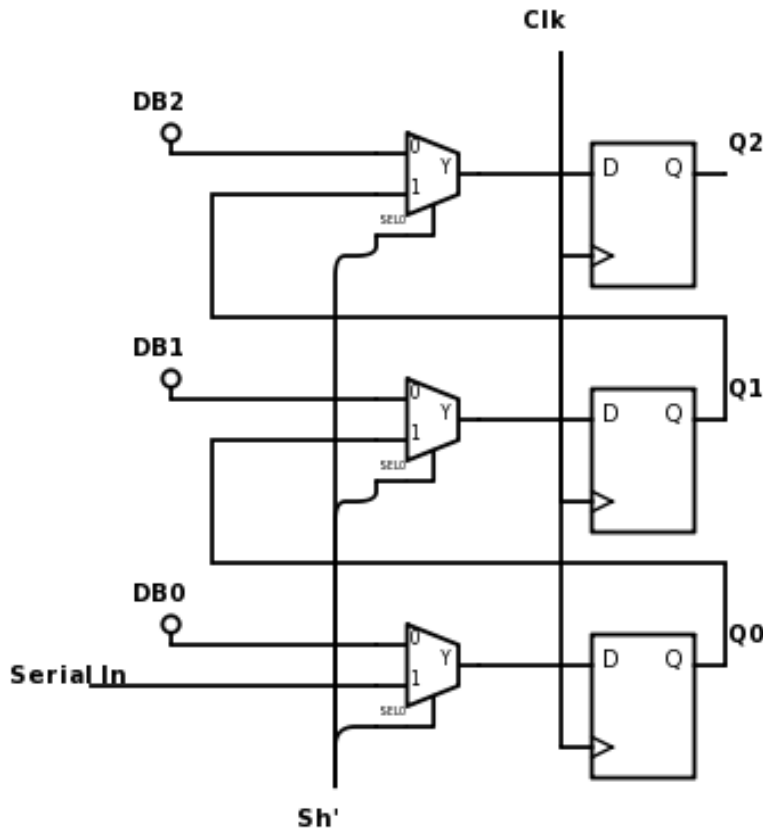
OR with equations:

$$Q_2^{n+1} = Sh DB_2 + Sh' \cdot Q_1^n$$

$$Q_1^{n+1} = Sh DB_1 + Sh' \cdot Q_0^n$$

$$Q_0^{n+1} = Sh DB_0 + Sh' \cdot \text{Serial In}$$

2. Draw the logic diagram of the circuit that you designed; explain your work



... or implementation with gates!