

DGD 6



Course Code : ITI 1100C

TA: Venkatraman

Professor : Dr. Ahmed Karmouch

Topics hope to cover

- Registers (Serial and Parallel)
- Counters
- Problems relating to designing counters and registers

Registers

- Multiple flip flops can be combined to form a data register
- Shift registers-allow data to be transported one bit at a time
- Two types of registers
 - (i) Serial Registers
 - (ii) Parallel Registers

Parallel Registers

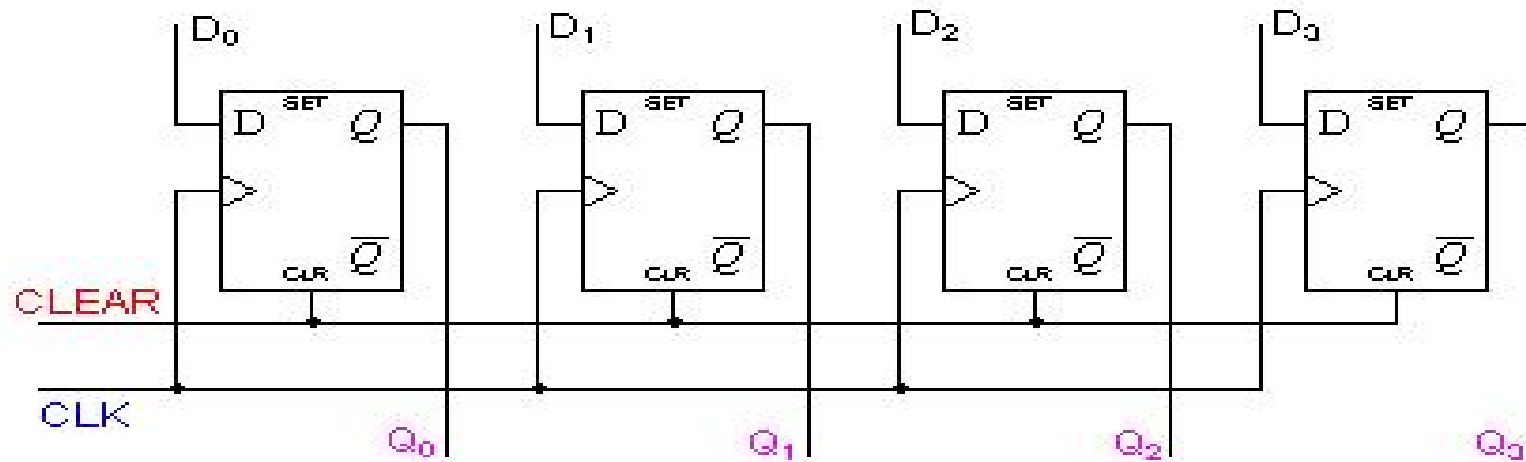
- Parallel Communications- Transfers a binary number through multiple data lines at the same time

There are two types-

- (i) Parallel in Parallel out
- (ii) Parallel in Serial out

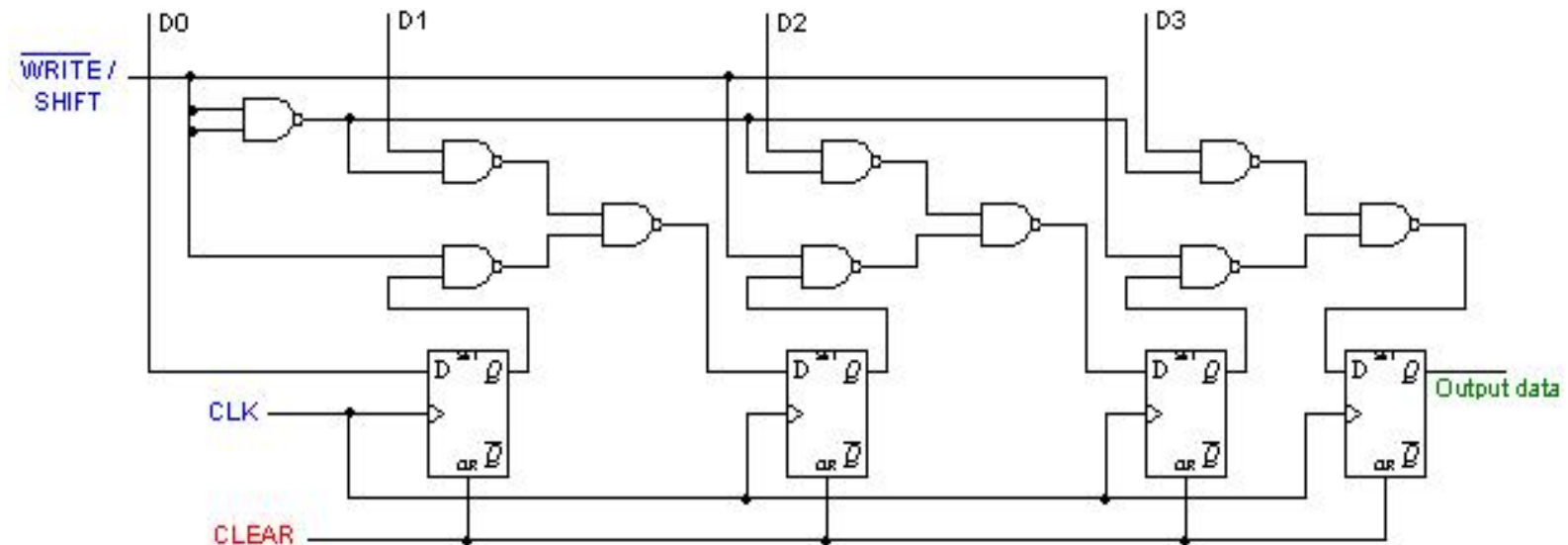
PiPo

- For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.



PiSo

D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the application of a clock pulse.



Serial Registers

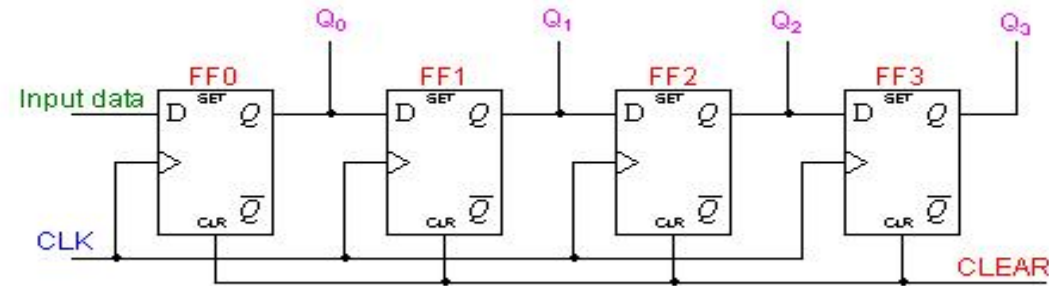
- Serial communications, transfers a binary number as a sequence of binary digits, one after another, through one data line

There are two types-

- (i) Serial In Serial out
- (ii) Serial in Parallel out

SiPo

For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below.



CLEAR 1001

Q0	Q1	Q2	Q3
0	0	0	0

100

Q0	Q1	Q2	Q3
1	0	0	0

10

Q0	Q1	Q2	Q3
0	1	0	0

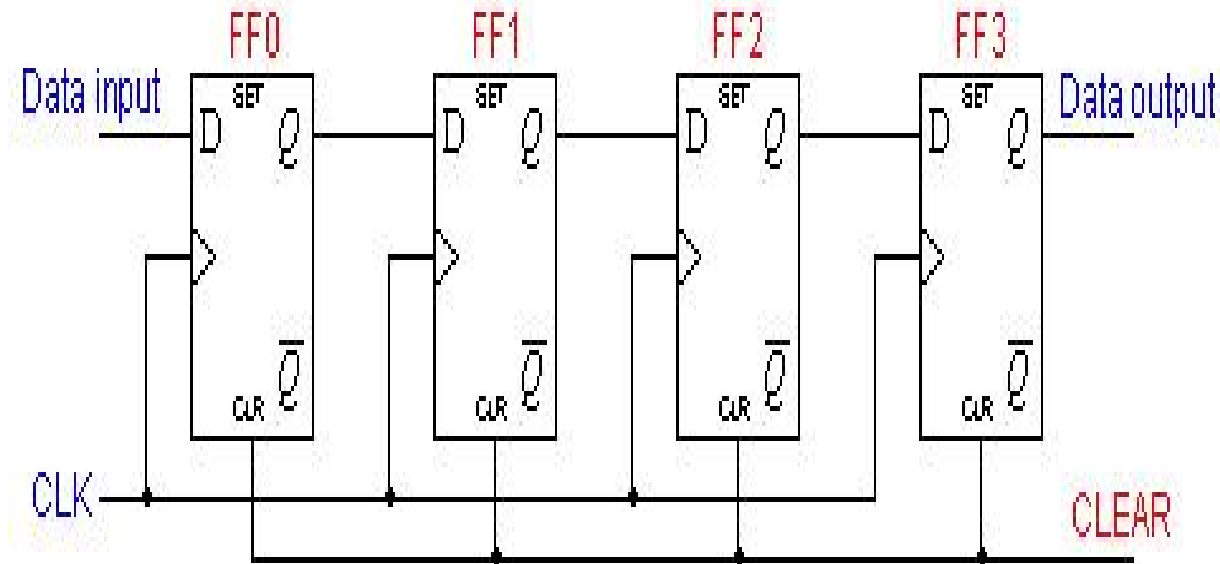
1

Q0	Q1	Q2	Q3
0	0	1	0

Movement of a four-bit binary number 1001. Each shift refers to the shifts in Q outputs of the register.

Design a SiSo (Serial in Serial out register) * Assume a data word to be 1001

Solution



The operation of the circuit is as follows. The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0). During each clock pulse, one bit is transmitted from left to right. The least significant bit of the data has to be shifted through the register from FF0 to FF3.

Solution - Tables

CLEAR	FF0	FF1	FF2	FF3
	0	0	0	0
1001	FF0	FF1	FF2	FF3
	0	0	0	0

1	FF0	FF1	FF2	FF3	000
	0	0	1	0	

100	FF0	FF1	FF2	FF3	0
	1	0	0	0	
10	FF0	FF1	FF2	FF3	00
	0	1	0	0	

0000	FF0	FF1	FF2	FF3	0000
	1	0	0	1	

■ What are Counters

A register that goes through a prescribed series of states

■ Different types of Counters

Asynchronous

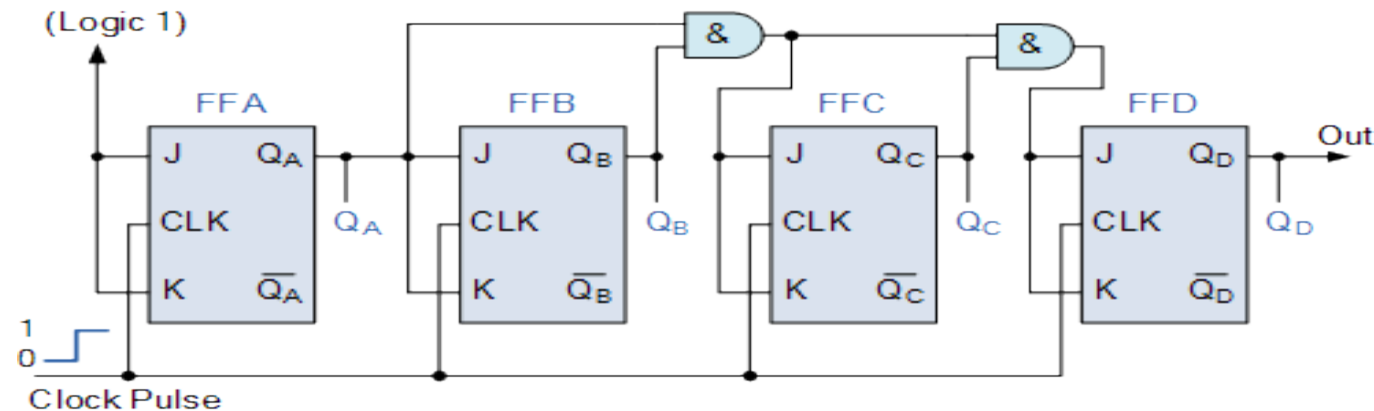
Flip flop output serves as a clock for triggering connected flip flops

Synchronous

All flip flops are triggered by a clock signal at the same time

Synchronous Counters

- All flip-flops get a clock.
- Bits come out at the same time.
- Practically speaking, stores the number of times a clock signal changes



Types of synchronous counters

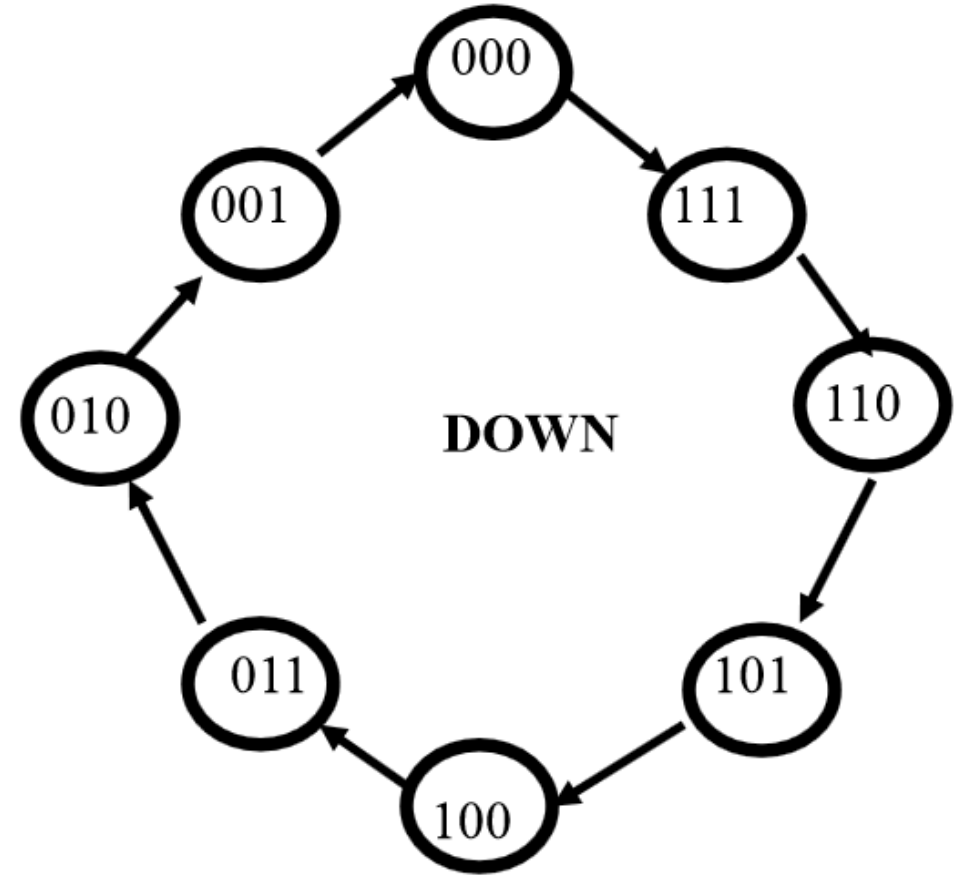
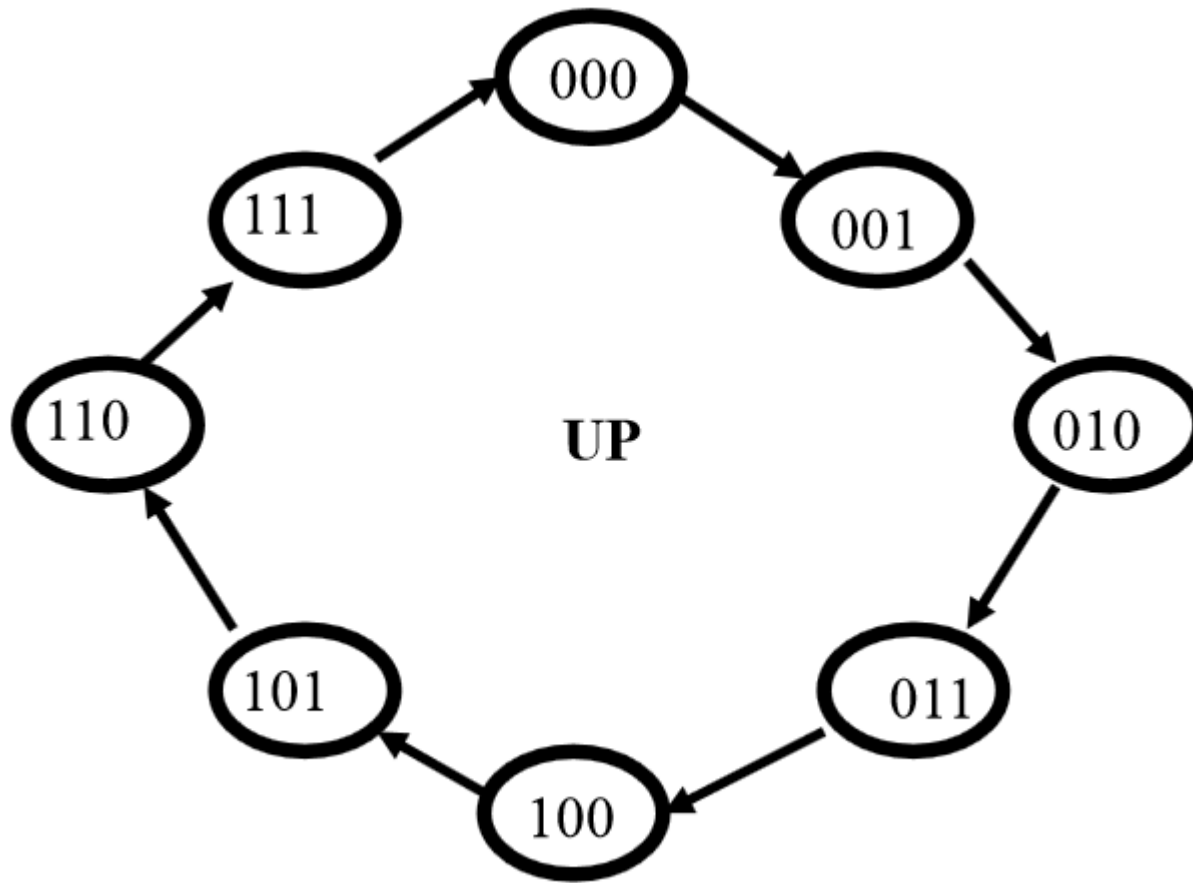


Different Synchronous

- Binary up counter
- Binary down counter
- BCD counter

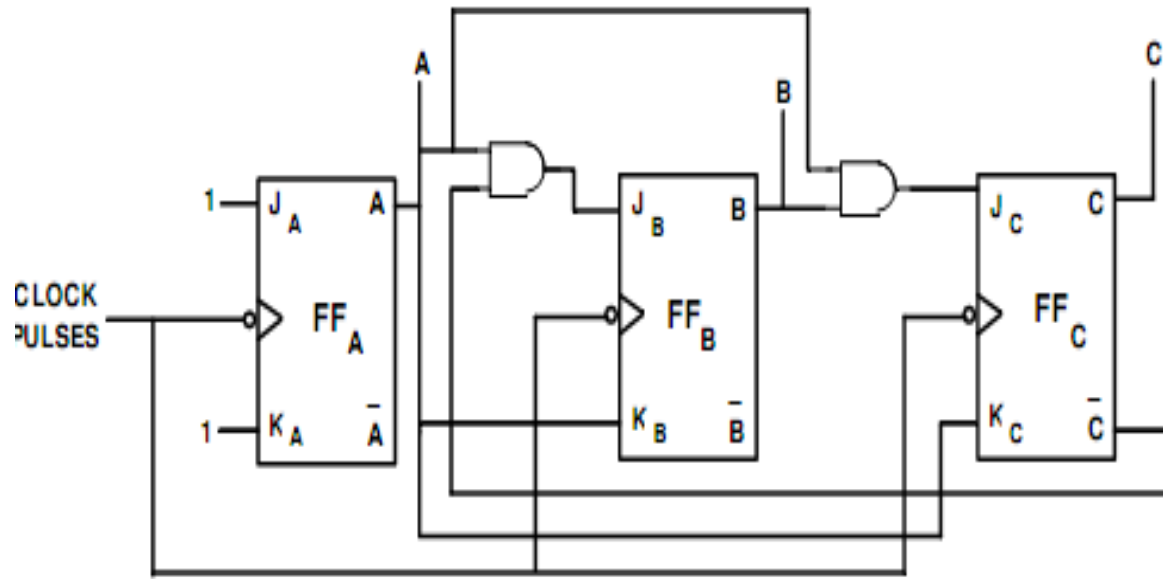
- Draw counter state diagram for Binary up/down counter

Up/down counters state diagrams



Problem 1.

- Design synchronous mod-6 up counter using J-K flip-flops, and do the following
- Convert the JK to T in the same scenario
- Get characteristic equations using K-maps
- Draw counter state diagrams



	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	1	1	X	1
A	X	X	X	X

Map for J_A
 $J_A = 1$
 Fig.(i)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	X	X	X	X
A	1	1	X	1

Map for K_A
 $K_A = 1$
 Fig.(ii)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	0	0	X	X
A	1	0	X	X

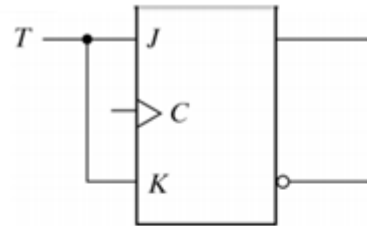
Map for J_B
 $J_B = A\bar{C}$
 Fig.(iii)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	X	X	X	0
A	X	X	X	1

Map for K_B
 $K_B = A$
 Fig.(iv)

- Short J-K to produce the T flip-flop

T Flip Flop



(a) From *JK* flip-flop

°Can be Created from JK or D flip flop

T	C	Q	Q'
0		Q_n	Q_n'
1		<i>Complement (toggle)</i>	

ITI1200A -A. Karmouch