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Exercises: 4.1, 4.5, 4.9, 4.21, 4.23, 4.27, 4.28, 4.33

Assignment 2

4.1 Consider the combinational circuit shown in Fig. P4.1.

a) Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs F_1 and F_2 as a function of the four inputs.

T_1	$\overline{B}C$
T_2	$\overline{A}B$
T_3	$(\overline{B}C) + A$
T_4	$D \oplus \overline{A}B$
F_1	$\left((\overline{B}C) + A\right) + (D \oplus \overline{A}B)$
F_2	$\overline{D} + (\overline{A}B)$

b) List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.

A	B	C	D	T1	T2	T3	T4	F1	F2
0	0	0	0	0	0	0	0	**0**	**1**
0	0	0	1	0	0	0	1	**1**	**0**
0	0	1	0	1	0	1	0	**1**	**1**
0	0	1	1	1	0	1	1	**1**	**0**
0	1	0	0	0	1	0	1	**1**	**1**
0	1	0	1	0	1	0	0	**0**	**1**
0	1	1	0	0	1	0	1	**1**	**1**
0	1	1	1	0	1	0	0	**0**	**1**
1	0	0	0	0	0	1	0	**1**	**1**
1	0	0	1	0	0	1	1	**1**	**0**
1	0	1	0	1	0	1	0	**1**	**1**
1	0	1	1	1	0	1	1	**1**	**0**
1	1	0	0	0	0	1	0	**1**	**1**
1	1	0	1	0	0	1	1	**1**	**0**
1	1	1	0	0	0	1	0	**1**	**1**
1	1	1	1	0	0	1	1	**1**	**0**

c) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expression are equivalent to the ones obtained in part (a).

F1	CD			
AB	00	01	11	10
00		1	1	1
01	1			1
11	1	1	1	1
10	1	1	1	1

$F_1 = A + C\overline{D} + \overline{B}D + B\overline{D}$

F2	CD			
AB	00	01	11	10
00	1			1
01	1	1	1	1
11	1			1
10	1			1

$F_2 = \overline{A}B + \overline{D}$

A	B	C	D	F1	F2	A + CD' + B'D + BD'	A'B + D'
0	0	0	0	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	1	1	1	1
0	0	1	1	1	0	1	0
0	1	0	0	1	1	1	1
0	1	0	1	0	1	0	1
0	1	1	0	1	1	1	1
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	1	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	0	1	0

Verification

4.5 Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

$A = \sum(3,6,7) = yz + xy\bar{z}$

A	yz			
x	00	01	11	10
0			1	
1			1	1

$B = \sum(1,2,4,5) = \bar{y}z + x\bar{y}\bar{z} + \bar{x}y\bar{z}$

B	yz			
x	00	01	11	10
0		1		1
1	1	1		

$C = \sum(0,2,5,7) = xz + \bar{x} \cdot \bar{z}$

C	yz			
x	00	01	11	10
0	1			1
1		1	1	

4.9 Using a truth table and K-Maps, design the BCD – to – seven – segment decoder using a minimum number of gates.

Truth Table:

A	B	C	D	*a*	*b*	*c*	*d*	*e*	*f*	*g*
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

K-Maps:

$a = A'C + A'BD + B'C'D' + AB'C'$

a	CD			
AB	00	01	11	10
00	1		1	1
01		1	1	1
11				
10	1	1		

$b = A'B' + A'C'D' + A'CD + AB'C'$

b	CD			
AB	00	01	11	10
00	1	1	1	1
01	1		1	
11				
10	1	1		

$c = A'B + A'D + B'C'D' + AB'C'$

c	CD			
AB	00	01	11	10
00	1	1	1	
01	1	1	1	1
11				
10	1	1		

$d = A'CD' + A'B'C + B'C'D' + AB'C' + A'BC'D$

d	CD			
AB	00	01	11	10
00	1		1	1
01		1		1
11				
10	1	1		

$e = A'CD' + B'C'D'$

e	CD			
AB	00	01	11	10
00	1			1
01				1
11				
10	1			

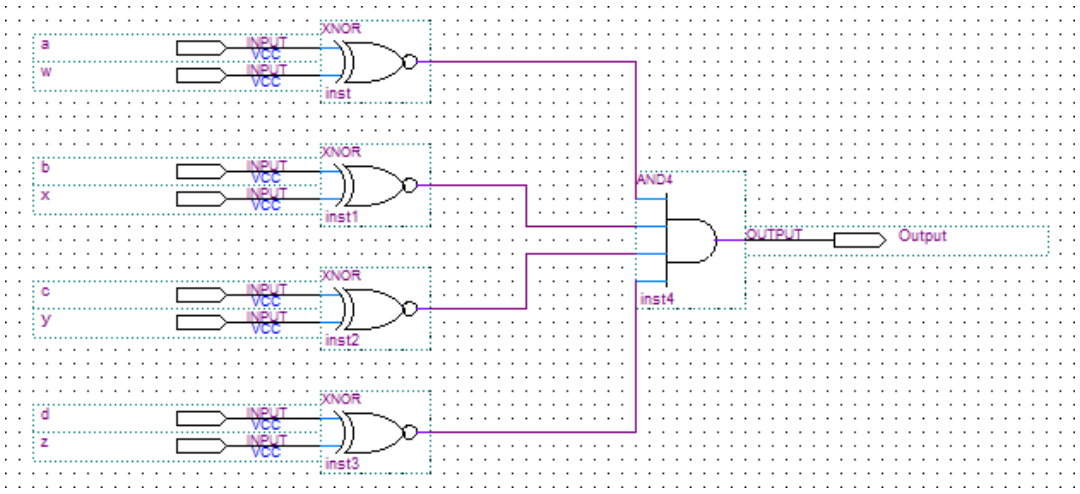
$f = A'BC' + A'C'D' + A'BD + AB'C'$

f	CD			
AB	00	01	11	10
00	1			
01	1	1		1
11				
10	1	1		

$g = A'CD' + A'B'C + A'BC' + AB'C'$

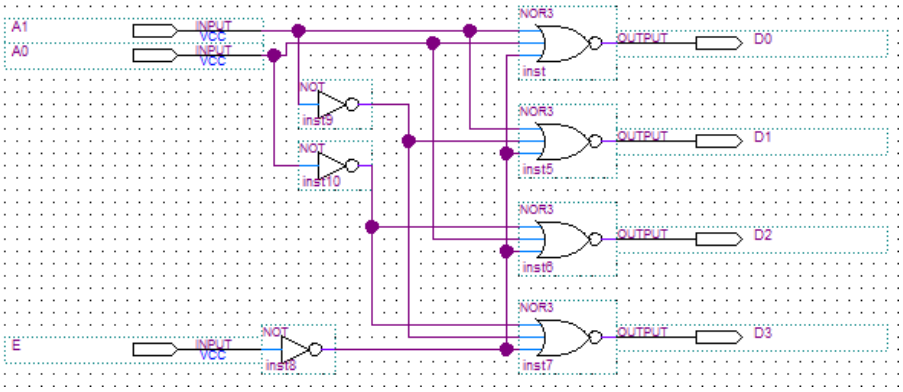
g	CD			
AB	00	01	11	10
00			1	1
01	1	1		1
11				
10	1	1		

4.21 Design a combinational circuit that compares two 4bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

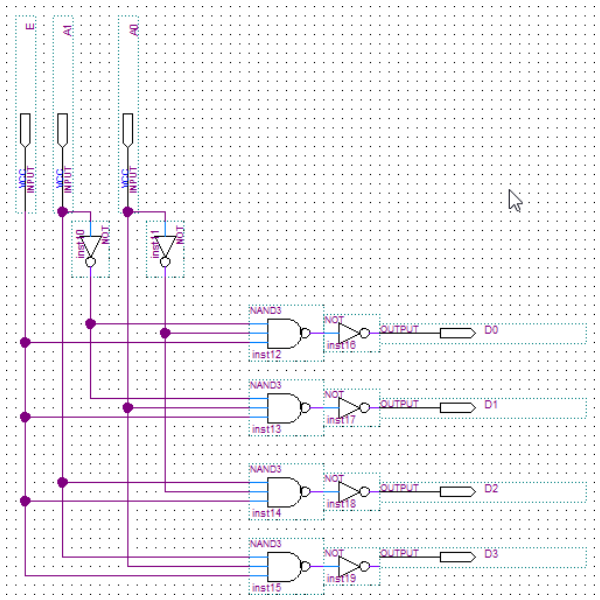


4.23 Design the logic diagram of a 2-to-4 line decoder using (a) NOR gates only and (b) NAND gates only. Include an enable input

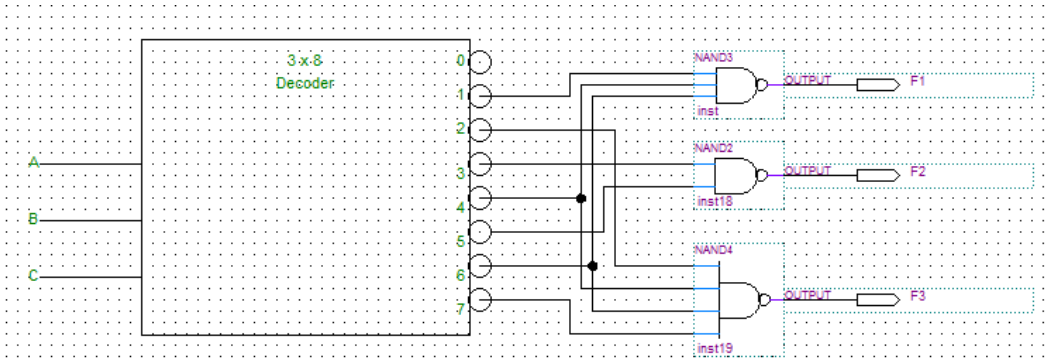
a)



b)



4.27 Implement the circuit with a decoder constructed with NAND gates.



4.33 Implement a full adder with two 4 x 1 multiplexers.