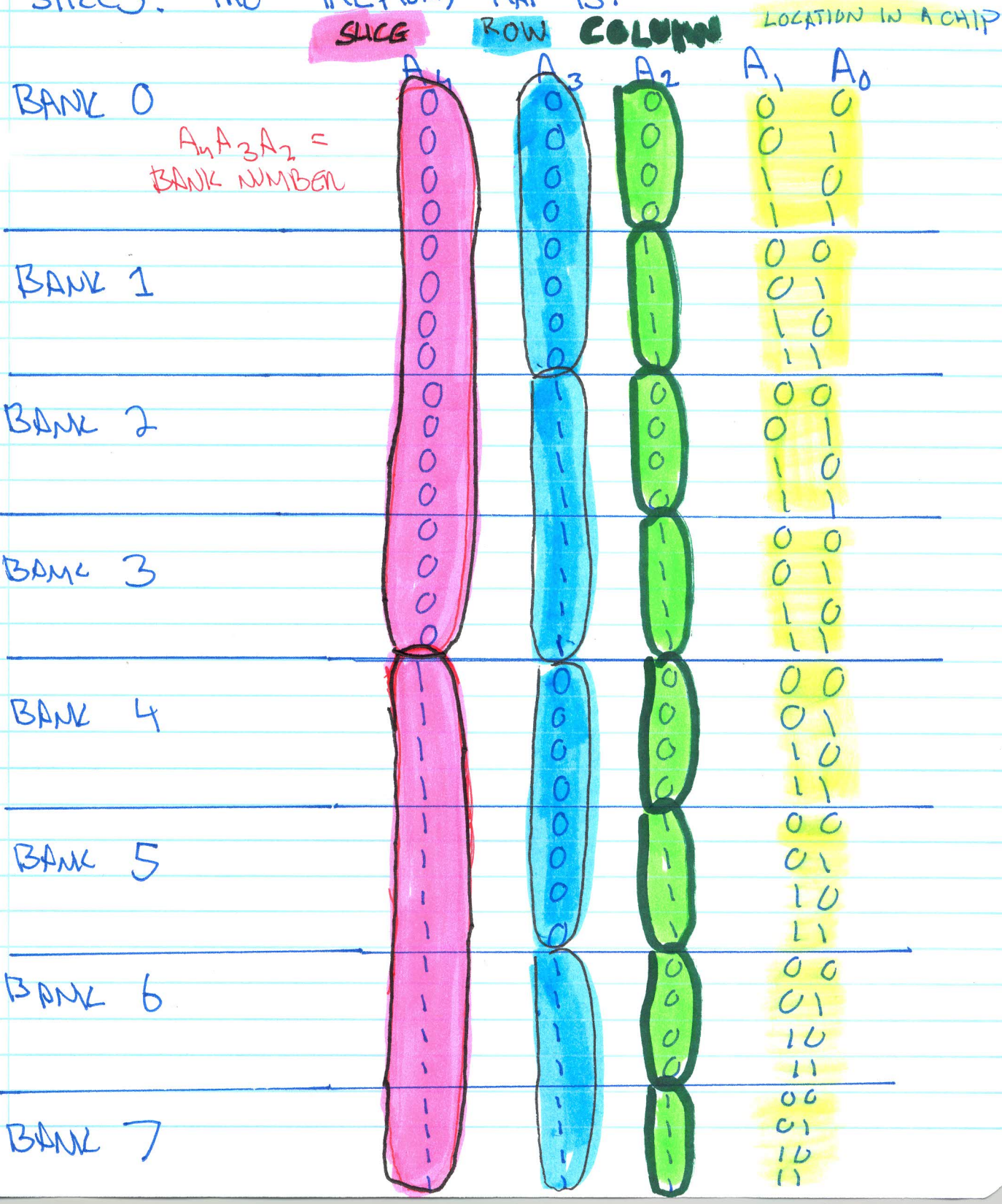
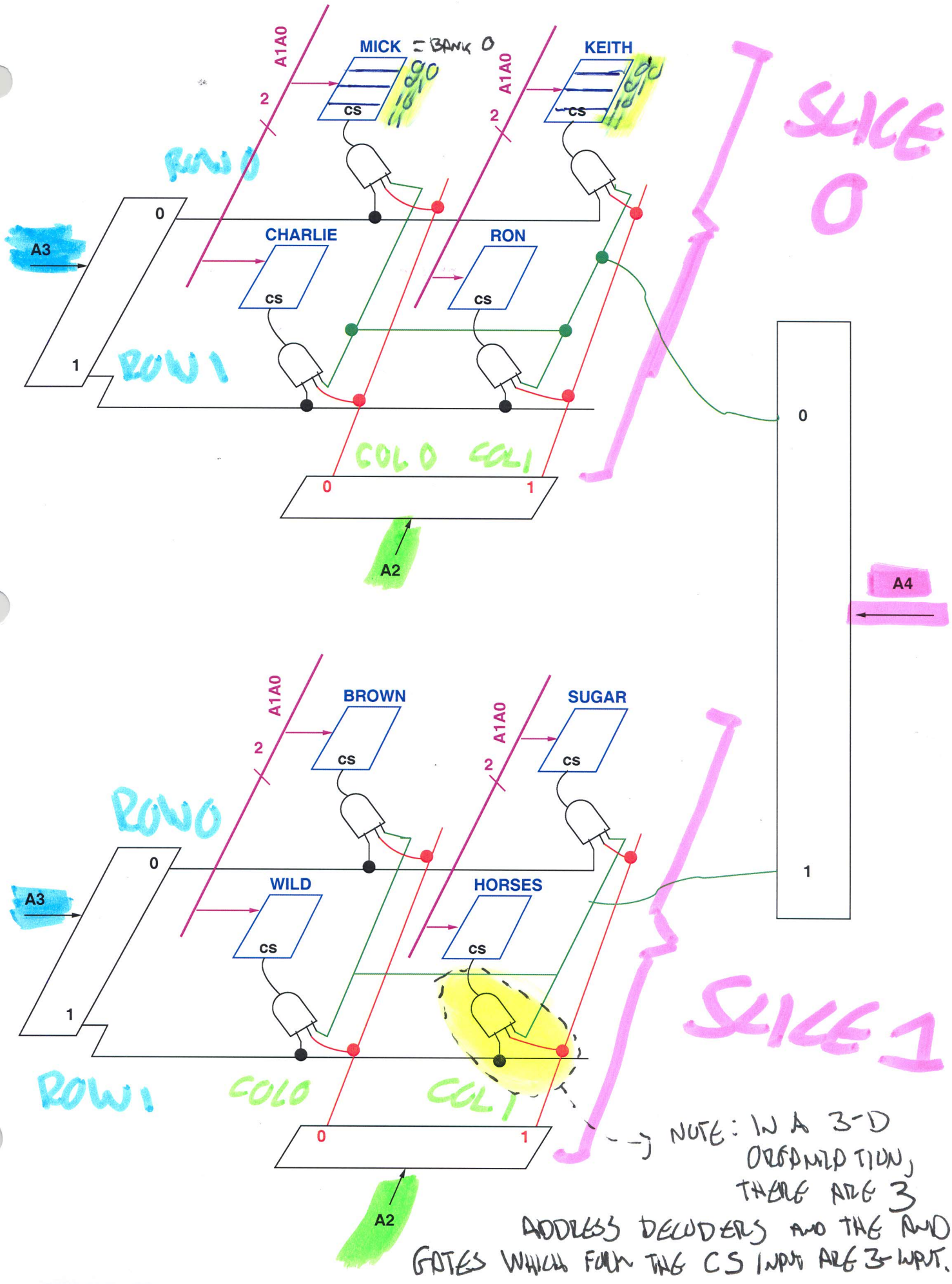
(USING CHIPS OF SIZE 4 LOCATIONS X 1 BIT)

3-D ORGANIZATION OF A 32 x 1 bit RAM

A 3-D organization employs three address decoders and consists of two "slices" of a 2-D memory system. The high-order address bit (A_4 in this example) decodes between the two slices. The MEMORY MAP is:




MICK = BANK 0
KEITH
CHARLIE
RON
BROWN
SUGAR
WILD
HORSES
A1A0
2
CS
A3
A2
A4
0
1
ROW 0
ROW 1
COL 0
COL 1
SLICE 0
SLICE 1
NOTE: IN A 3-D ORGANIZATION, THERE ARE 3 ADDRESS DECODERS AND THE AND GATES WHICH FORM THE CS INPUT ARE 3-INPUT.