Name:_____ Student #:_____ Section:_____

Question	Max Marks	Score
1	10	
2	20	
3	25	
4	25	
5	20	
Total	100	

CARLETON UNIVERSITY

FINAL
EXAMINATION
April 29, 2005

Duration: 3 hours

Department name and course number: Electronics ELEC-2507 (A,B,C)

Course Instructor(s): R. Mason, A. Steele Number of students: 220

AUTHORIZED MEMORANDA:

NON-PROGRAMMABLE CALCULATOR

Students MUST count the number of pages in this examination paper before beginning to write, and report any discrepancies immediately to a proctor. **This question paper has 17 pages**.

This examination question paper MAY NOT be taken from the examination room.

This exam consists of 5 questions, which should be answered on this exam paper in the space provided. Attempt all questions. Marks allocated to each question are indicated (total marks = 100).

Note: The solution must be clearly indicated. Multiple solutions or solutions that are not clearly identified, will be marked incorrect. Using approximate relations (unless they are given below or specified in a question) is not accepted. Clearly state all assumptions made. **Clearly mark the units for all final answers**. **Clearly indicate axis/units for any graphs**. **SHOW YOUR WORK!**

Diode:

Forward current: $I_D \approx I_S\left(e^{V_D / nV_T}\right)$

Small signal resistance: $r_d = \frac{nV_T}{I_D}$

$V_T = \frac{kT}{q} = 25mV$ at room temperature

Bipolar Transistor:

Active mode operation: V_{BE}= 0.7V
Saturation mode operation: V_{CEsat}= 0.2V

$$i_C = \beta i_B \quad i_C = \alpha i_E \quad i_E = i_B + i_C$$

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta}{g_m} \qquad r_o = \frac{V_A}{I_C}$$

$$r_e = \frac{\alpha}{g_m} = \frac{r_\pi}{\beta + 1} \qquad \alpha = \frac{\beta}{\beta + 1}$$

Operational Amplifier:

$V_o = A(V_+ - V_-)$; $R_i = \infty$; $R_o = 0$

MOSFET:

$$I_{DS} = k' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right];$$

$$I_{DS,sat} = k' \frac{W}{L} \frac{(V_{GS} - V_t)^2}{2}(1 + \lambda V_{DS});$$

$$k' = \mu C_{ox}; \quad K = k' \frac{W}{L}$$

$$V_{DS,sat} = V_{GS} - V_t \qquad g_{mb} = \chi g_m$$

$$g_m = k' \frac{W}{L}(V_{GS} - V_t) = \sqrt{2k' \frac{W}{L} I_{DS}}$$

$$r_{DS,triode} = \left[k' \frac{W}{L}(V_{GS} - V_t)\right]^{-1}; \; r_o = \frac{V_A}{I_D}$$

Q1: Answer the following by filling in the corresponding circles with your selection *a, b, c or d*

(10 marks).

i) Assuming all diodes have a forward bias turn on voltage of 0.7V which statement best describes how the circuit in Fig. 1.1 operates?

a) LED1 is illuminated when V_i is -5V
b) LED2 is illuminated when V_i is -5V
c) Both LED1 and LED2 are illuminated when V_i is 5V
d) LED2 is illuminated when V_i is 5V

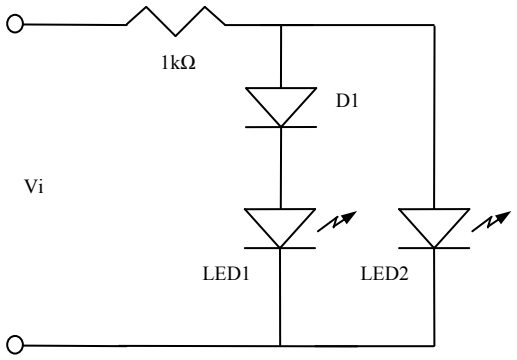


Fig 1.1

ii) Which one of the following statements best describes a forward biased silicon diode?

a) The current through the diode is exponentially related to the diode voltage
b) The voltage across the diode is 0 volts
c) The current through the diode is of the form kV_D^2 where k is a constant and V_D is the diode voltage
d) The current through the diode is 0 amps

iii) A npn BJT has I_B=1uA and β=100. Which of the following statements is true?

a) I_C=100uA, V_{CE}=0.01V, the devices is operating in active mode
b) I_C=10uA, V_{CE}=1V, the devices is operating in saturation mode
c) I_C=1000uA, V_{CE}=0.01V, the devices is operating in saturation mode
d) I_C=100uA, V_{CE}=1V, the devices is operating in active mode

iv) Which of the following best describes how we can increase the small signal voltage gain of a standard BJT common emitter amplifier?

a) increase the power supply voltage
b) decrease the transistor output resistance
c) increase the collector resistance
d) decrease the transistor β

v) What is the value of V_C for the circuit in Fig. 1.2

a) 8.7V
b) 10V
c) 0V
d) 1.7V

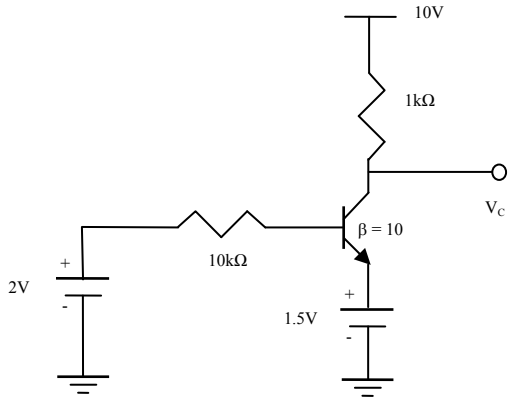


Fig. 1.2

vi) Which of the following is NOT a characteristic of an ideal operational amplifier?

a) infinite input impedance
b) zero common-mode rejection
c) zero output resistance
d) infinite open-loop gain

vii) Which is the best description of the circuit in figure 1.3?

a) unity gain amplifier
b) a buffer
c) an integrator
d) a differentiator

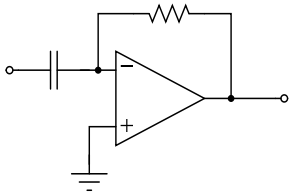


Fig 1.3

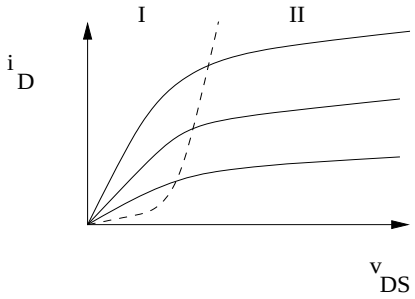


Fig. 1.4

viii) Figure 1.4 shows a sketch of the $i_D - v_{DS}$ characteristic curves for a MOSFET. What are regions I and II known as?

a) I-triode II-active
b) I-cut-off II-saturation
c) I-triode II-saturation
d) I-cut-off II-triode

ix) Examine the circuit in Fig. 1.5. Which statement below is correct?

a) $V_{DS} = V_{DD} + R_D I_D$
b) $V_{DS} = V_{GS}$
c) $V_{DS} = V_{GS} + R_G I_D$
d) $V_{DS} = V_{DD}$

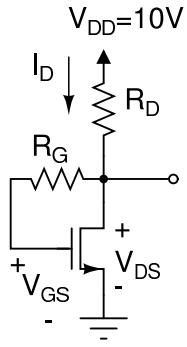


Fig. 1.5

x) A transistor amplifier has the following measure characteristics for two different load resistances.

Load resistance	Input voltage / mV	Output voltage /mV
Without R_L	8	80
With R_L = 5 kΩ	7	60

Calculate the open circuit voltage gain, A_{VO}, the voltage gain with the 5 kΩ load resistor, A_V and the output resistance, R_o. Which of the following best matches the calculated parameters?

a) A_{VO} = 10, A_V = 11.7 and R_o = 5 kΩ
b) A_{VO} = 8.6, A_V = 10 and R_o = 1.3 kΩ
c) A_{VO} = 10, A_V = 7.5 and R_o = 1.7 kΩ
d) A_{VO} = 10, A_V = 8.6 and R_o = 0.8 kΩ

Q2: Diodes

a) The circuit has been designed in Fig. 2.1, with diodes having forward voltages of 0.7V.

(i) If V_A = -3V V_B = 0.7V, V_C = 5V and V_D = 3V, what will be the output at Vx and the current I? If voltage V_A, V_B, V_C and V_D could only be 0V or 5V this circuit could be used as a logic gate. What type of gate would it be? **(4 Marks)**

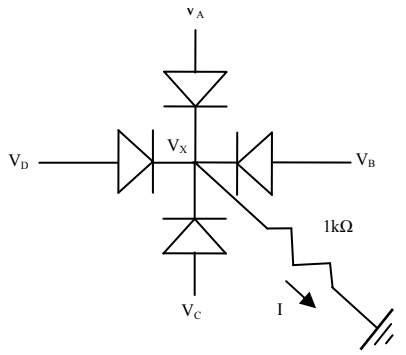


Fig. 2.1

V_x = _____

I = _____

Logic Gate Type = _____

b) A zener diode circuit has been designed using two identical zener diodes as shown in Fig. 2.2.

The zener data for each diode is V_z = 4 V at I_z = 2 mA,
r_Z = 20Ω and I_{zk} = 0.5 mA.

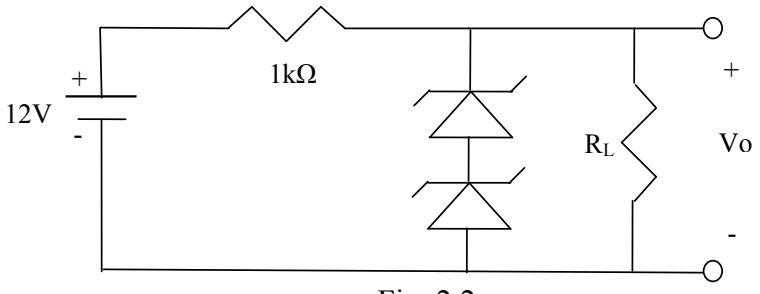


Fig. 2.2

Answer the following questions:

i) Find the DC value of V_O **with no load resistor** (R_L). **(4 Marks)**

$V_O =$ _____

ii) Find the change in V_O if the 12V power supply were to vary by ±1V. **(2 Marks)**

$\Delta V_O =$ _____

iii) For the nominal 12V supply, what is V_O if a 10kΩ load resistor, R_L, is added?

(3 Marks)

$V_O =$ _____

iv) For the nominal 12V supply, compute the minimum value of R_L so that the output is maintained at a relatively constant output.

(3 Marks)

$R_{Lmin} =$ _____

c) A square wave input as shown below is applied to V_i of the ideal diode circuit in Fig. 2.3.

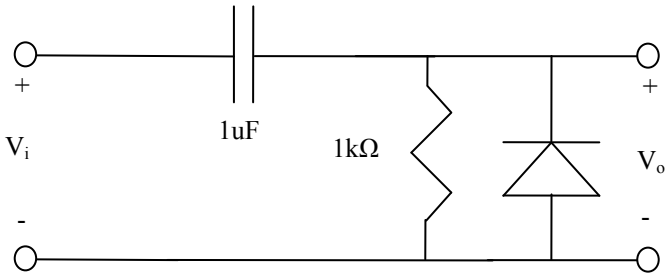
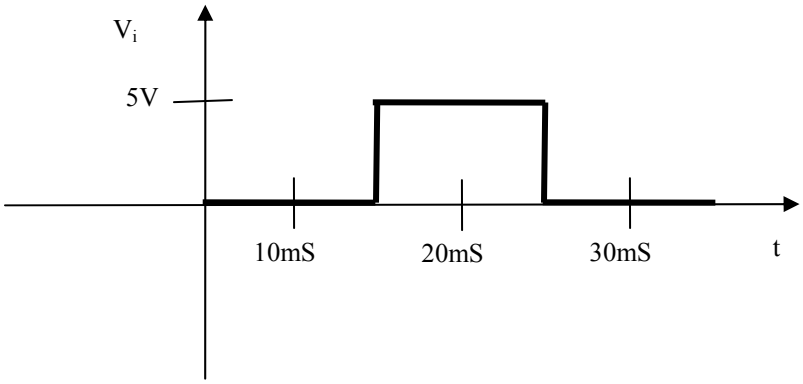
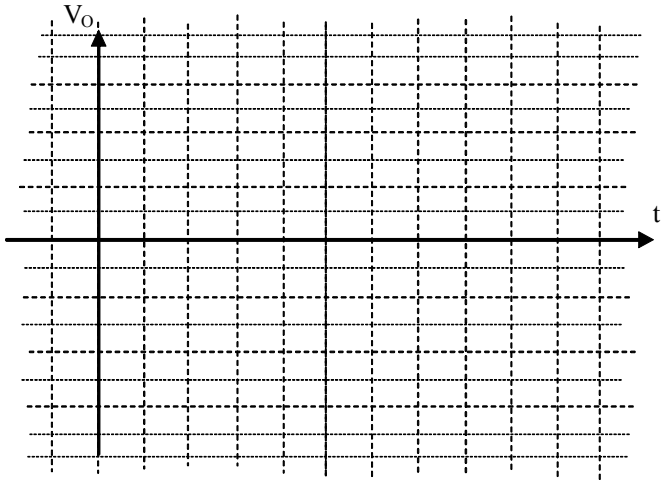


Fig. 2.3



Sketch the resulting waveform at Vo assuming the initial value of Vo is 0V. Make sure to include scales on the voltage and time axis **(4 Marks)**



Q3: MOSFET

The MOSFET circuit shown in Fig, 3.1 is biased by a constant current source.

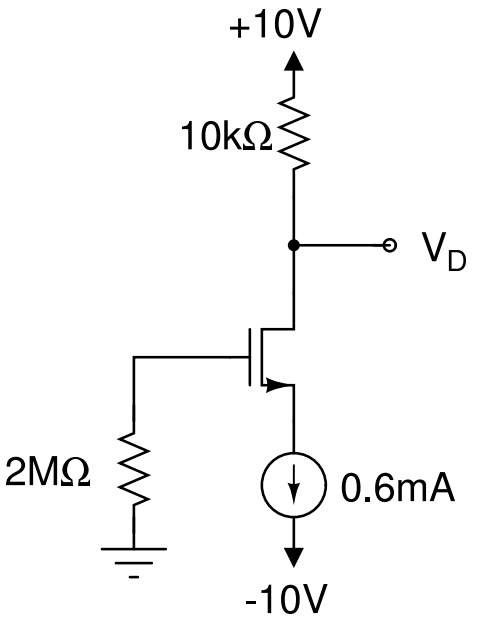


Fig. 3.1

a) Given V_t = 1.5 V, k'_n = 120 μA/V^2 and W/L = 10
   i. Find the following voltages, V_{GS}, V_G, V_S and V_D.

(5 Marks)

V_{GS} _____ V_G _____ V_S _____ V_D _____

ii. Calculate g_m & r_0 given V_A = 80V.

(2 Marks)

g_m _____ r_0 _____

iii. A MOSFET circuit that could be used as the constant source in Fig 3.1 is called the current mirror. Sketch the basic MOSFET current mirror circuit.

(3 Marks)

b) The circuit is modified so that it can be used as a small-signal amplifier. The new circuit, with the signal source, is shown in Fig. 3.2

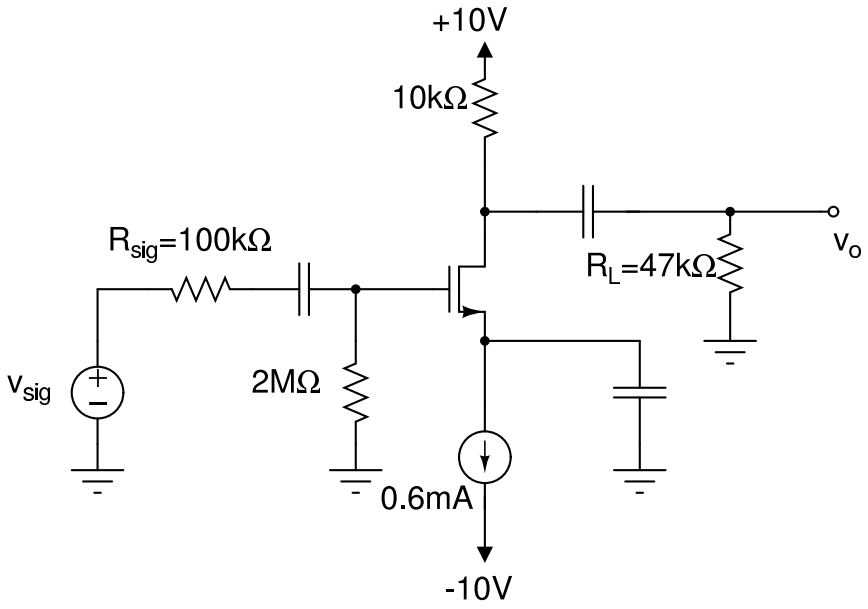


Fig. 3.2 (Assume all capacitors have an infinite value).

i. Sketch the equivalent hybrid-π small signal circuit model for this circuit.

(4 Marks)

ii. Determine the input resistance, R_{in}, output resistance, R_{out} and voltage gain, A_v for the amplifier (take into account r_0 & R_L).

(3 Marks)

R_{in} _____ R_{out} _____ A_v _____

iii. If v_{sig} is a 0.2 V peak-to-peak sinusoid and assuming small-signal operation, what output signal v_o results if R_{sig} and R_L are 100kΩ and 47kΩ, respectively?

(2 Marks)

v_o _____

c) A resistor is now place into the source branch of the circuit (after the MOSFET source terminal and prior to the capacitor and current source).

i. Sketch the equivalent T-model equivalent circuit for this circuit with a source resistor

(4 Marks)

ii. State what will happen to the output $v_{o,}$ now that the source resistor is inserted. (Note, you do not need to perform analysis, just state what will happen).

(2 Marks)

Q4: BJT

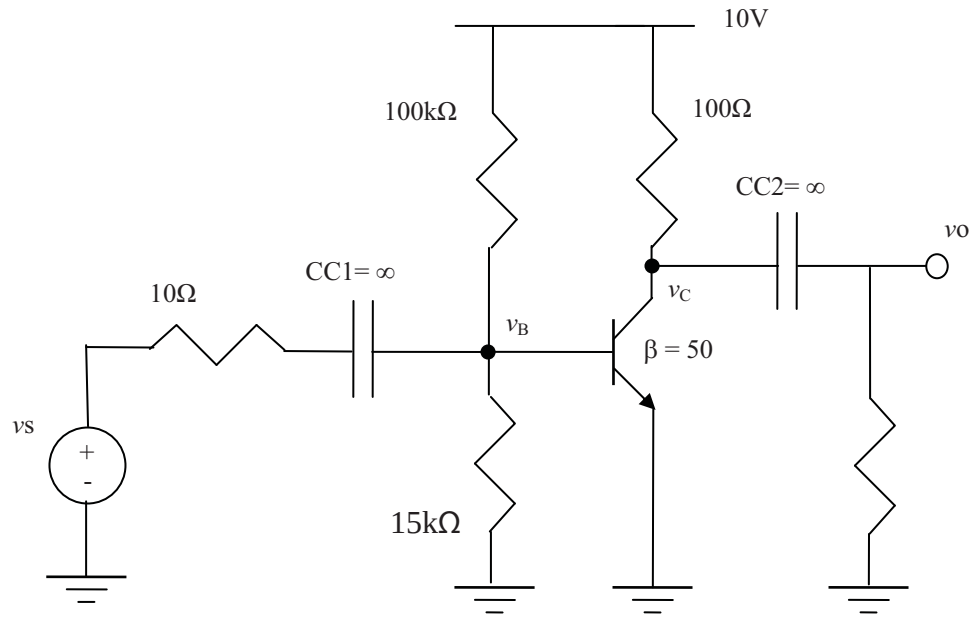


Fig. 4.1

a) For the BJT amplifier circuit shown in Fig. 4.1:

i) Draw the DC equivalent circuit that can be used for calculating DC voltages and currents

(3 Marks)

ii) Assuming room temperature, determine values for V_B, V_C, I_B, and I_C (where V_B etc. have their usual meaning):

(7 Marks)

V_C=_____

V_B=_____

I_B=_____

I_C=_____

4. b)

i) The BJT in figure 4.1 had an early voltage of 500V. Compute parameters $\mathbf{r_\pi}$, $\mathbf{g_m}$, **and** $\mathbf{r_o}$,

(3 Marks)

g_m=_____

r_o =_____

r_π =_____

ii) Draw the small signal A. C. equivalent circuit based on parameters calculated above in 4 b) **(use the hybrid π model).**

(5 Marks)

iii) Find the input resistance R_i

(**2 Marks)**

R_i=_____

iv) Find the intermediate voltage gain, $A_{v1} = v_i/v_s$.

(1 Mark)

A_{v1}=_____

(v) Find the intermediate voltage gain $A_{v2} = v_o/v_i$.

(3 Marks)

A_{v2}=_____

(vi) Find the overall voltage gain, $A_v=v_o/v_s$. **(1 Mark)**

A_v=_____

5. Operational Amplifier

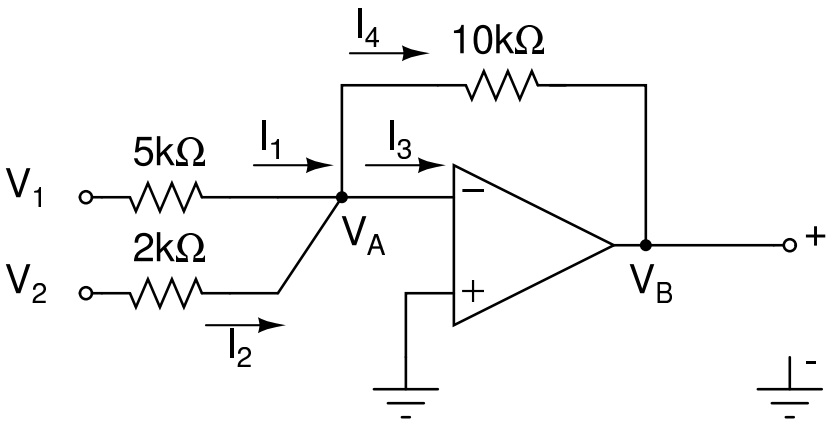


Fig. 5.1

a) Assuming ideal operational amplifiers (op-amps.), analyze the circuit in Fig. 5.1 and find expressions for the various branch currents and nodal voltages (as marked on the figure). Note: V_1 and V_2 are the inputs to the circuit.

(6 Marks)

I_1 =_____ I_2 =_____ I_3 =_____ I_4 =_____ V_A =_____ V_B =_____

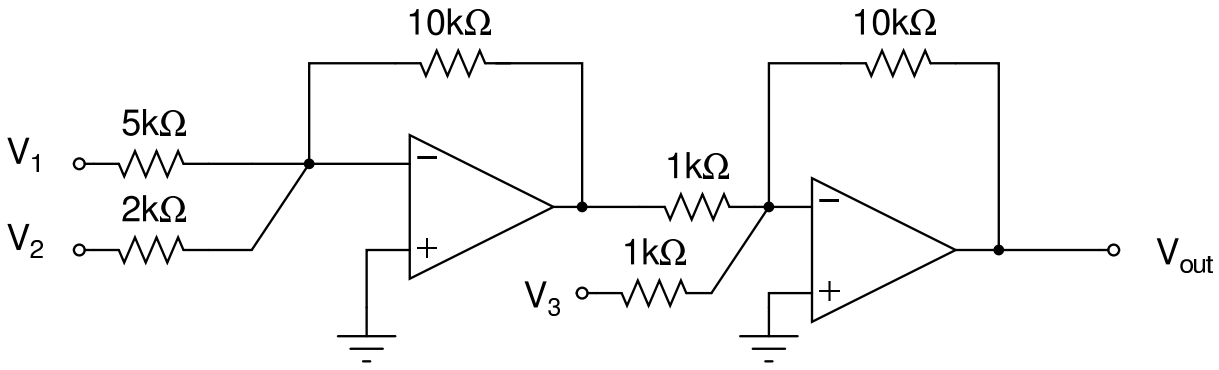


Fig. 5.2

b) The circuit in a) is now used to make a larger circuit, see Fig. 5.2. The intention is for this circuit to have the output response:

$$V_{out} = 2V_1 + 5V_2 + 10V_3 \qquad (5.1)$$

Measurements show that this circuit does not give the desired response, stated in (5.1)

i. Analyze the circuit and state the correct response of the proposed circuit.

(3 Marks)

ii. Provide a circuit design that will give the response of (5.1) using only the components shown in Fig. 5.2, plus an extra 10 kΩ resistor. Note: you do not need to use all the components.

(4 Marks)

c) An op-amp. based inverting Miller integrator is measured at 1 kHz and found to have a voltage of -50V/V.

i. Sketch the basic circuit for an op-amp. inverting Miller integrator.

(2 Marks)

ii. At what frequency is the gain reduced to -1V/V?

(3 Marks)

iii. Sketch the response of the magnitude of the gain (in dB) with respect to angular frequency (radians per second).

(2 Marks)

END