Course	Number	Section	
Electronics I	ELEC 311	BB	
Examination	**Date**	**Time**	**# of pages**
Final	August 12, 2005	Three hours	3
Instructor			
Dr. R. Raut			

Materials allowed: [X] No [ ] Yes (Please specify)

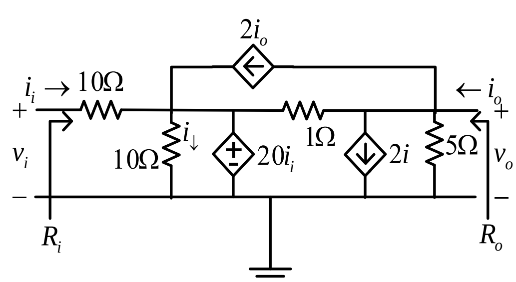
Calculators allowed: [ ] No [X] Yes

Students are allowed to use silent, non-programmable electronic calculators without text display.

Special Instructions:

Attempt all questions.
Show all steps clearly in neat and legible handwriting.
Students are required to return question paper together with exam booklet(s).

Q.1: For the equivalent circuit below, find the corresponding basic voltage amplifier model, i.e., find (a) $A_{VO} = v_o/v_i$, (ii) R_i , and (iii) R_o. Now find the corresponding transconductance model equivalent for the same circuit.

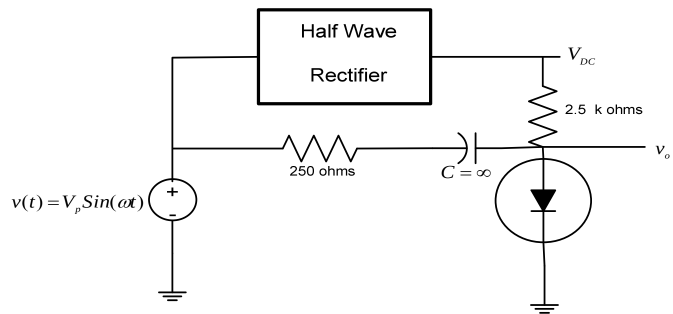


Q.2: A zener diode exhibits a constant voltage of 5.6 V for currents greater than five times than the knee current I_{ZK}=0.5 mA. The zener is used to build a shunt regulator fed from a raw DC supply with nominal value of 15 V. The load current varies from 0 mA to 15 mA. Find a suitable value for the resistance R which is connected in series with the raw DC supply. The zener has an internal resistance of 5 ohms. What will be the load regulation of this regulator system?

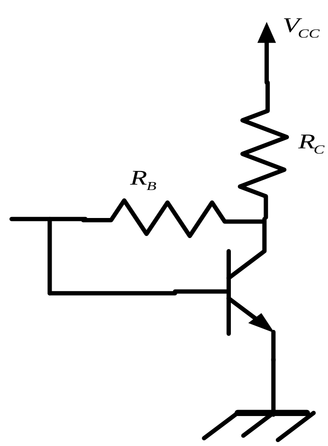
Q.3: A semiconductor junction diode is used in an automatic gain control system as shown below. The ac resistance of the diode is dependent on the amplitude V_p of the input signal. Higher V_p is, lower is the diode ac resistance and more it tends to attenuate the input ac signal. That is how the gain control mechanism works.

The input signal is half-wave rectified to generate a DC voltage which drives the DC current through the diode. This DC voltage is given by V_p / π. The diode is a 1 mA diode. The voltage drop across the diode changes by 100 milli volts for a decade (10 times) change in current through it. You may use the relation: $V_2 = V_1 + 2.303 n V_T \log(I_2 / I_1)$. The DC resistance of the diode can be neglected.

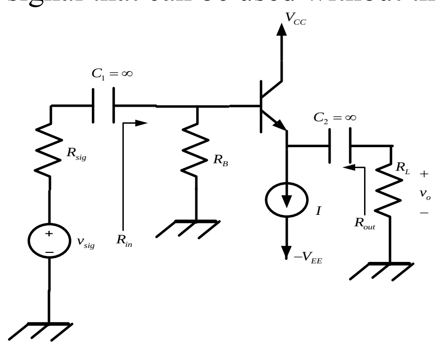
(a) If the input ac signal has an amplitude of 15 volts, what will be the output signal magnitude v_o?
(b) If the input ac signal amplitude shoots up to 30 volts, how much (approximately) will v_o become?



Q.4: Design the following BJT circuit to obtain a dc current of 1 mA and to ensure a ±2 V signal swing at the collector; that is design for V_{CE} =2.3 V. Given that V_{CC}=10 V, and β = 100.

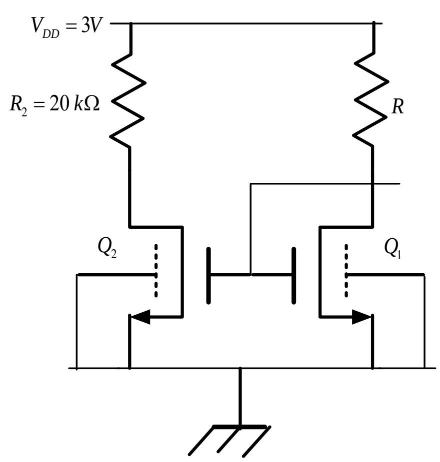


Q.5: Consider the emitter-follower BJT amplifier circuit below. Find R_{in}, R_{out} and the voltage gain v_o/v_{sig}. Given R_{sig} = 10 kΩ, R_B = 40 kΩ, R_L = 1 kΩ, β=49**,** and V_A = 100 V. The bias current I = 5 mA. What is the largest peak amplitude of an output sine-wave signal that can be used without the transistor cutting off?



Q.6: (a) Consider the MOS circuit below. The transistor Q_1 is biased for I_D = 80 μA. Both Q_1 and Q_2 have V_t=0.6 V. Design R and then find the drain current and drain voltage for Q_2. The channel modulation effect may be ignored and you may use the I-V equation: $I = K_{ni}(V_{GS} - V_t)^2$, i=1,2 for your work. Given $K_{n1} = 500\ \mu A/V^2$, $K_{n2} = 750\ \mu A/V^2$ for transistors Q_1 and Q_2 respectively.

(b) Assume now that the early voltage V_A = 40 V for both Q_1 and Q_2. Draw the ac equivalent model for the circuit below.



Course	Number	Section
Electronics I	ELEC 311	BB

Final Examination	Date	Time	# of pages
	August 22, 2006	Three hours	4

Instructor

Dr. R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use silent, non-programmable electronic calculators without text display.

Special Instructions:

Attempt all questions.
Show all steps clearly in neat and legible handwriting.
Students are required to return question paper together with exam booklet(s).

Q.1: For the circuit shown below, find I_D and V_D for the case V_{DD} =5 V, and R= 10 kΩ. Assume that the diode has a voltage drop of 0.7 V at 1-mA current and that the voltage changes by 0.1 V/decade of current change. Use (a) iteration method, and (b) the piecewise-linear model for the diode with V_{DO}=0.65 V and r_D =20 Ω.

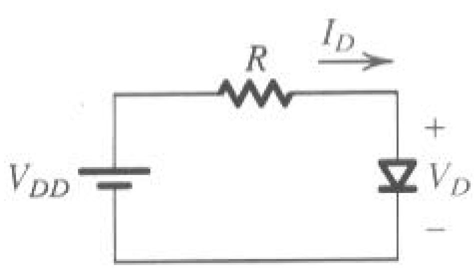


Figure 1

Q.2: A bridge-rectifier circuit with a filter capacitor has R= 100 ohms. The secondary transformer delivers a sinusoid of 12 V (rms) and has a frequency of 60 Hz. The diodes have V_D = 0.8 V each.
(a) What will be the value of the filter capacitor so that the ripple voltage is limited to below 0.5 V peak-to-peak?

(b) What is the DC voltage at the output of the system?
(c) What is the conduction angle for the diode?

Q.3: For the transistor amplifier shown below, assume $\alpha \cong 1$ and V_{BE} =0.5 V at the edge of conduction.

(a) What are the values of V_E and V_C for V_B =0 V?
(b) For what value of V_B does the transistor cut off?, Saturate?
(c) In each case, what values of V_E and V_C result?

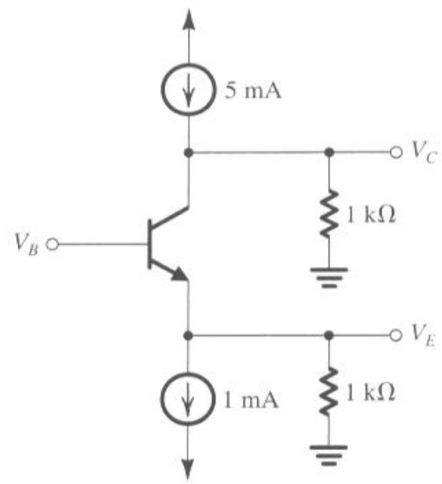


Figure 3

Q.4: For the BJT circuit below, the signal source generates ac signal with zero DC. The transistor has β =100, and r_o =200 kΩ.
(a) Find R_E to establish a DC current of 0.5 mA. Assume V_{BE}=0.7 V for conduction.
(b) Find R_C to obtain V_C = 5 V.
(c) With R_L = 10 kΩ, draw the ac equivalent circuit for the amplifier system, and
(d) Determine the system voltage gain.

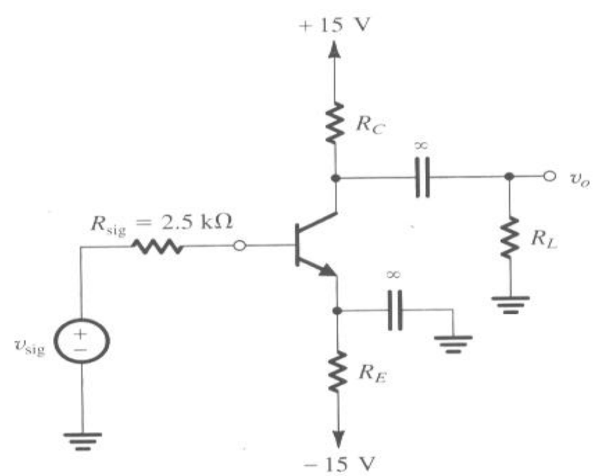


Figure 4

Q.5: For the circuit shown below, find
(a) the input resistance R_{in} , and
(b) the voltage gain v_o/v_{sig} . Assume that the source provides a small signal v_{sig} and that β=100.
(c)What will be the maximum v_{sig} value for which the small signal approximation will remain valid?

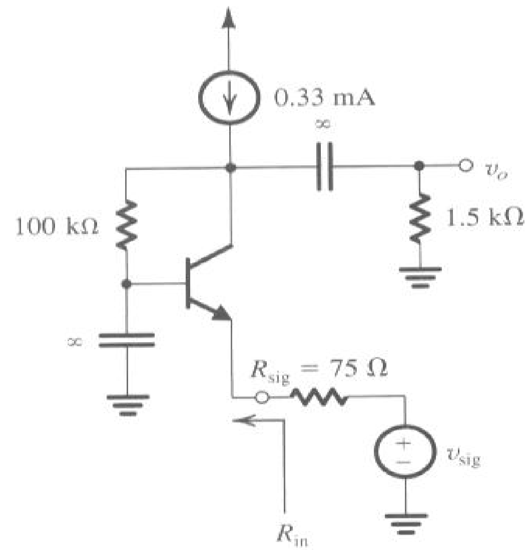


Figure 5

Q.6: Consider the MOSFET amplifier in the figure below. Given that V_G= 4V, R_S=1 kΩ. The transistor has V_t= 1V, and $k_n'(W/L) = 2$ mA/V^2 .
(a) Find the bias current I_D?
(b) What will be the voltage gain $\mathbf{v_o}/v_{sig}$, if R_D =20 kΩ, R_{G1} = 2 MΩ, R_{G2} =1 MΩ, R_{sig} =10 kΩ, and V_{DD} =12 V?

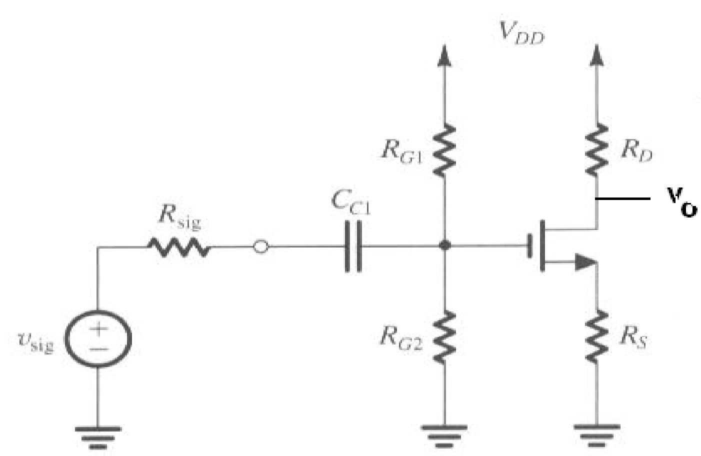


Figure 6

Some important Formulas (BJT & MOSFET)

Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right) \qquad r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships Between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta+1 = \frac{1}{1-\alpha}$$

Overdrive voltage:

$$v_{OV} = v_{GS} - V_t$$
$$v_{GS} = V_t + v_{OV}$$

Operation in the *triode* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \geq V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{OV}$

- i-v Characteristics:

$$i_D = \mu_n C_{ox}\frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

- For $v_{DS} \ll 2(v_{GS} - V_t) \quad \Leftrightarrow \quad v_{DS} \ll 2v_{OV}$

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = 1\Big/\left[\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)\right]$$

Operation in the *saturation* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \leq V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{OV}$

- i-v Characteristics:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

$$r_o = \left[\lambda\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2\right]^{-1} = \frac{V_A}{I_D}$$

where

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

- Transconductance:

$$g_m = \mu_n C_{ox}\frac{W}{L}V_{OV} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{OV}}$$

- Output resistance:

$$r_o = V_A/I_D = 1/\lambda I_D$$

Course	Number	Section
Electronics I	ELEC 311	BB

Final Examination	Date	Time	# of pages
	August 15, 2007	Three hours	4

Instructor

Dr. R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use silent, non-programmable electronic calculators without text display.

Special Instructions:

Attempt all questions.
Show all steps clearly in neat and legible handwriting.
Students are required to return question paper together with exam booklet(s).

Q.1: For the equivalent circuit below, find the corresponding basic voltage amplifier model, i.e., find (a) $A_{VO} = v_o/v_i$, (ii) R_i , and (iii) R_o.

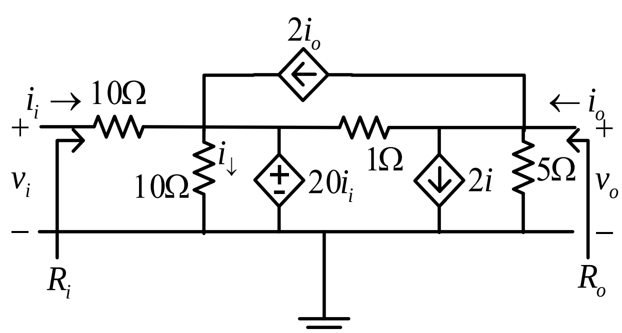


Figure 1

Q.2: A semiconductor junction diode is used in an automatic gain control system as shown below. The ac resistance of the diode is dependent on the amplitude V_p of the input signal. Higher V_p is, lower is the diode ac resistance and more it tends to attenuate the input ac signal. That is how the gain control mechanism works.

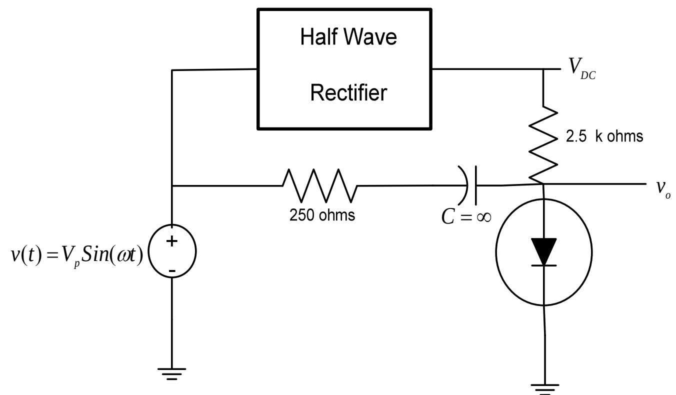


Figure 2

The input signal is half-wave rectified to generate a DC voltage which drives the DC current through the diode. This DC voltage V_{DC} is given by V_p / π, where V_p is the amplitude of the *ac* signal.

The diode is a 1 mA diode. The voltage drop across the diode changes by 100 milli volts for a decade (10 times) change in current through it. You may use the relation $V_2 = V_1 + 2.303 n V_T \log(I_2 / I_1)$. The DC resistance of the diode can be neglected.

(a) If the input ac signal has an amplitude of 15 volts, what will be the amplitude of the output signal v_o?
(b) If the input ac signal amplitude shoots up to 30 volts, how much will v_o become?

Q.3: For the transistor amplifier shown below, assume $\alpha \cong 1$ and V_{BE} =0.5 V at the edge of conduction.

(a) What are the values of V_E and V_C for V_B =0 V?
(b) For what value of V_B does the transistor cut off?, Saturate?
(c) In each case, what values of V_E and V_C result?

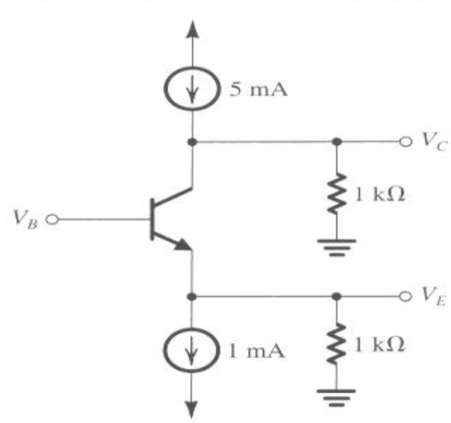


Figure 3

Q.4: For the circuit shown below, find

(a) the input resistance R_{in} , and

(b) the voltage gain v_o/v_{sig} . Assume that the source provides a small signal v_{sig} and that β=100.

(c)What will be the maximum v_{sig} value for which the small signal approximation will remain valid?

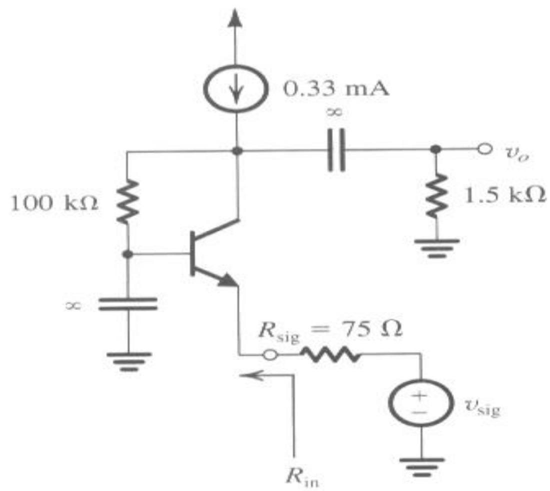


Figure 4

Q.5: Consider the MOSFET amplifier in the figure below. Given that V_G= 4V, R_S-=1 kΩ. The transistor has V_t= 1V, and $k_n'(W/L) = 2$ mA/V^2 .

(a) Find the bias current I_D?

(b) What will be the voltage gain $\mathbf{v_o}/v_{sig}$, if R_D =20 kΩ, R_{G1} = 2 MΩ, R_{G2} =1 MΩ, R_{sig} =10 kΩ, and V_{DD} =12 V?

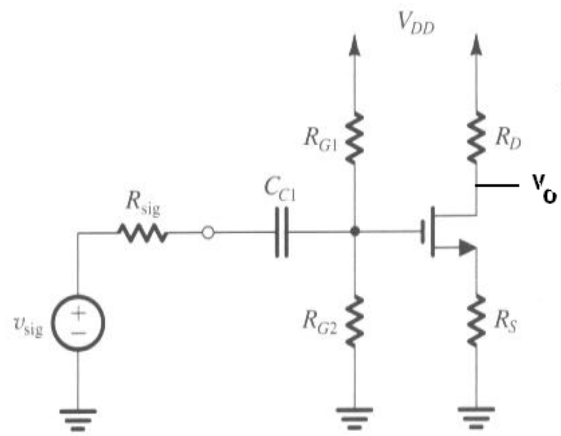


Figure 5

Q.6: (a) Consider the MOS circuit below. The transistor Q_1 is biased for $I_D = 80\ \mu A$. Both Q_1 and Q_2 have V_t=0.6 V. Design R and then find the drain current and drain voltage for Q_2. The channel modulation effect may be ignored and you may use the I-V equation: $I_i = K_{ni}(V_{GS} - V_t)^2$, i=1,2 for your work. Given $K_{n1} = 500\ \mu A/V^2$, $K_{n2} = 750\ \mu A/V^2$ for transistors Q_1 and Q_2 respectively.

(a) Assume now that the early voltage V_A = 40 V for both Q_1 and Q_2. Draw the ac equivalent model for the circuit below.

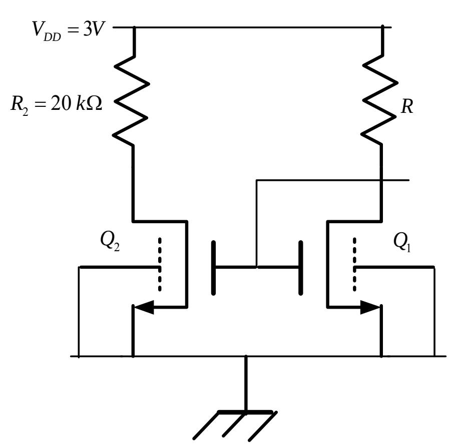


Figure 6

Course	Number	Section
Electronics I	ELEC 311	BB

Examination	Date	Time	# of pages
Final	August 20, 2008	3 hours	4

Instructor(s)

R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use ENCS approved calculators only.

Special Instructions:

Attempt ALL questions.
Show all steps clearly in neat and legible handwriting.
Students are required to return question paper together with exam booklet(s).

Q.1: A full wave bridge rectifier circuit with 1-kΩ load R_L operates from a 120-V (rms) 60-Hz supply through a 10:1 step-down transformer as shown in figure 1 below. Each of the diode is modeled as a battery with 0.7-V drop.

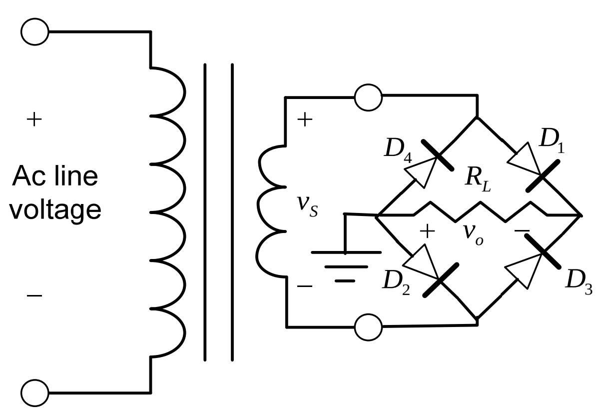


Figure 1

(a) What is the peak value of the rectified voltage across the load?
(b) For what fraction of a cycle does each diode conduct?
(c) What is the average current through the load?

Q.2: For the circuit shown in figure 2, the voltage V_E was measured to be -0.7 V. If □=50, find I_E, I_B, I_C, and V_C.

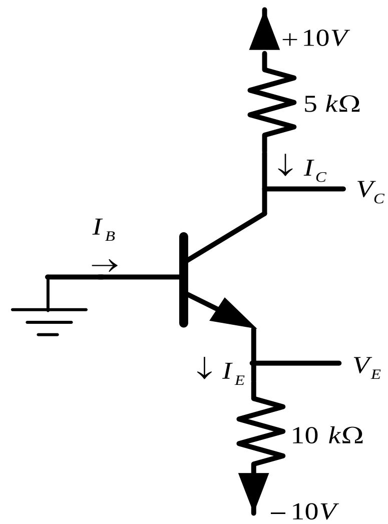


Figure 2

Q.3: In the circuit shown below (Fig.3), the transistor has □=199. Find

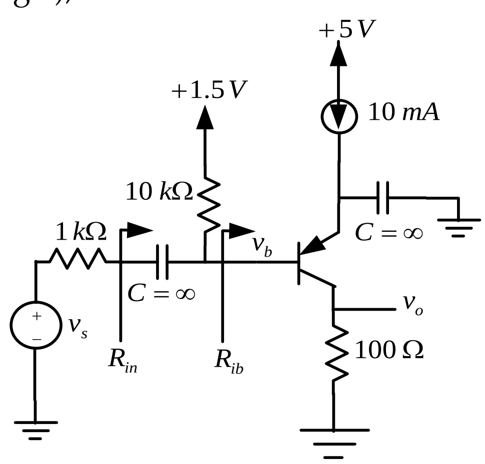


Figure 3

(a) the DC voltage at the collector.
(b) the DC voltage at the base
(c) the input resistance R_{in} (*use the small-signal ac equivalent circuit model for the BJT*)

Q.4: In the BJT amplifier circuit of figure 4, the DC bias current I_C is 2.3 mA. The transistor has a β=100 and Early voltage V_A =100 Volts.

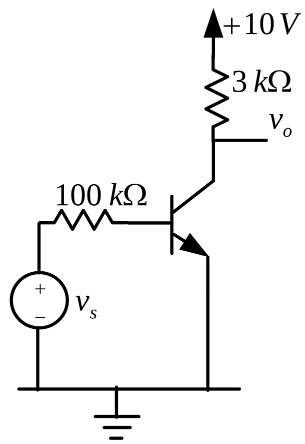


Figure 4

(a) Draw the small-signal ac equivalent model for the amplifier and show the values of the ac parameters g_m, r_π, r_o.
(b) Find the voltage gain v_o/v_s.
(c) Up to what value of v_s the amplifier will operate properly (i.e., the BJT shall remain in the active mode)?

Q.5: Consider the MOFET amplifier shown in figure 5. Design the resistances so that you can achieve V_D=3.4 V, V_S =1.6 V, and I_D=0.3 mA. The voltage divider resistances R_{G1}, R_{G2} has a current of 1-μA. The MOSFET has V_t=1 V, $k_n(w/L) = 1$ mA/V^2.

Given VDD=10V

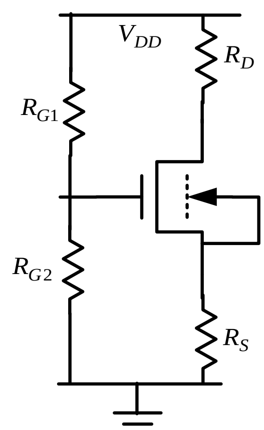


Figure 5

Q.6: For the NMOS amplifier shown in figure 6, replace the transistor with its T-equivalent model.

Derive
(a) the expression for the voltage gain v_s/v_i.
(b) the expression for the voltage gain v_d/v_i.

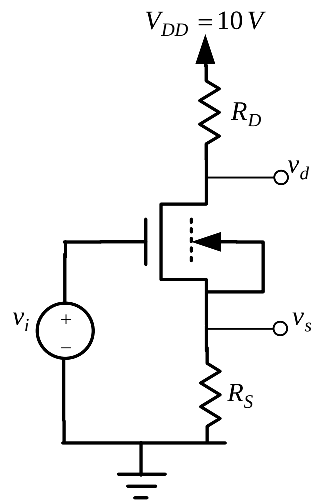
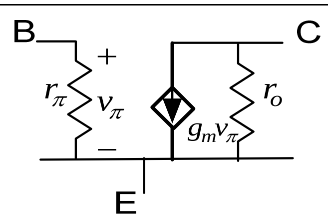
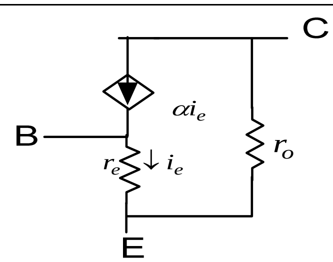
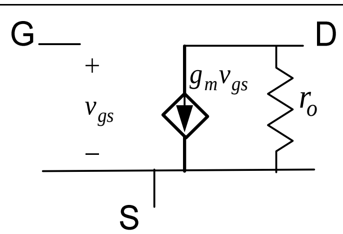
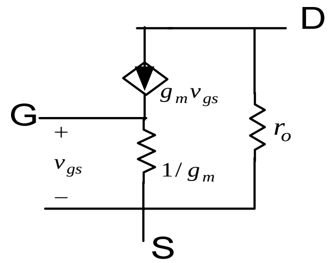


Figure 6

(Some formulae and equivalent circuits)

$I_C = \beta I_B$, $I_E = (\beta+1) I_B$	$g_m = \dfrac{I_C}{V_T}$, $r_\pi = \dfrac{\beta}{g_m}$, $\alpha = \dfrac{\beta}{\beta+1}$	$r_o = \dfrac{V_A}{I_C}$, $r_e = \dfrac{r_\pi}{\beta+1}$, $I_C = I_S \exp(V_{BE}/V_T)$
$I_D = k\left(\dfrac{W}{L}\right)\left((V_{GS}-V_t)V_{DS} - \dfrac{V_{DS}{}^2}{2}\right)$ (linear region)	$I_D = k\left(\dfrac{W}{2L}\right)(V_{GS}-V_t)^2(1+\lambda V_{DS})$ (saturation region)	$g_m = k\left(\dfrac{W}{L}\right)(V_{Gs}-V_t) = \sqrt{\dfrac{2kI_D W}{L}}$ $r_o = \dfrac{V_A}{I_D}$
 BJT hybrid pi	 BJT T	
 MOS hybrid pi	 MOS T	

Course		Number	Section
Electronics I		ELEC 311/1	BB
Examination	**Date**	**Time**	**# of pages**
Final	August 14, 2009	3 hours	6

Instructor(s)

Dr.R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use ENCS faculty approved calculators

Special Instructions:

You MUST attempt **Q.1** (*soft skill* component) .

For **Q.2-Q.7**, answer any **FOUR** questions.

Before submitting your answer book, **fill in the Table below** indicating the answers you want to be graded.

If you **do not** *fill in the Table*, the instructor will mark your answers *as they appear one after another in the answer book*

Show all steps clearly in neat and legible handwriting.

Students are required *to return the question paper* together with exam booklet(s).

Table

Answers to be graded	**Q.1 (compulsory)**				
Marks					

(**Soft skill component-** *The student MUST answer this question*)

Q.1: Consider the MOS circuit below. Both Q_1 and Q_2 have V_t=0.7 V. Ignore the channel modulation effect. You may use the I-V equation: $I = K_{ni}(V_{GS} - V_t)^2$, i=1,2 for your work.

Given $K_{n1} = 500\ \mu A/V^2$, $K_{n2} = 750\ \mu A/V^2$ for transistors Q_1 and Q_2 respectively.

(a) Design R to establish I_D = 100 μA in the transistor Q_1

(b) Find the drain current and drain voltage for Q_2.

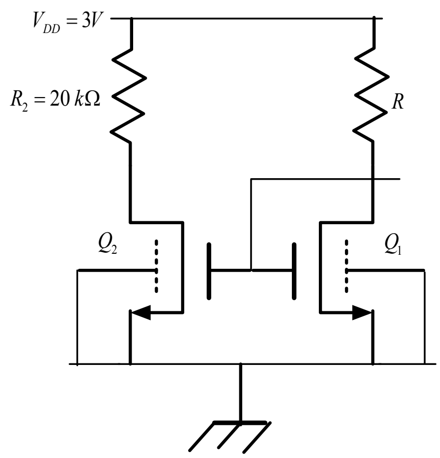


Figure 1:

(Answer any **FOUR** from the questions below)

Q.2: A zener diode exhibits a voltage of 6.5 V for I_Z= 5 mA. The zener has I_{ZK}=0.5 mA, and a minimum of *five times* I_{ZK} must flow through the zener for reliable operation. The diode has an internal resistance of 15 ohms. The device is used to build a shunt regulator circuit as shown below.

The raw DC supply has a nominal value of 15 V, and can range between 12 V to 18 V. The load current varies from 0 mA to 15 mA.

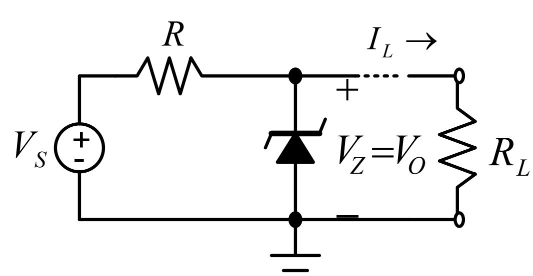


Figure 2:

(a) Design a suitable value for the resistance R for reliable operation.
(b) What will be the output voltage if R_L= 450 Ω is connected across the output of the system and the raw DC is at its lowest value (12 V)?

Q.3: A bridge-rectifier circuit with a filter capacitor has R_L = 100 ohms. The secondary transformer delivers a sinusoid of 15 V (rms) and has a frequency of 60 Hz. The diodes have V_{DO} = 0.7 V each.

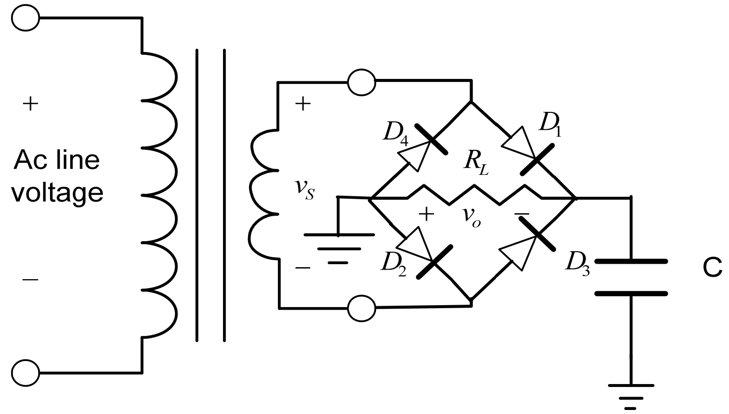


Figure 3

(a) What will be the value of the filter capacitor *C* so that the ripple voltage is limited to below 500 mV peak-to-peak?

(b) What is the DC voltage at the output of the system?

(c) What is the conduction angle for each diode in the system? Explain with appropriate sketches.

Q.4: For the BJT circuit (Figure 4), the signal source generates ac signal with zero DC. The transistor has β=100, and r_o =20 kΩ.

(a) Find R_E to establish a DC current of I_E= 0.5 mA. Assume V_{BE}=0.7 V for conduction.

(b) Find R_C to obtain V_C = 5 V.

(c) Determine the system voltage gain with R_L = 10 kΩ,

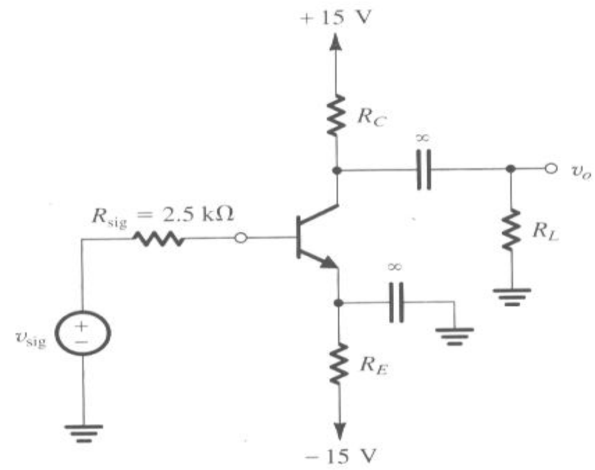


Figure 4:

Q.5: Consider the emitter-degenerated CE BJT amplifier circuit shown below. The signal source has a resistance R_s = 1 kΩ and the load R_L is 5 kΩ.

Given V_A = infinity, β =100, I_E = 2 mA.

(a) What value of R_E will make R_{in} =10 kΩ?
(b) With the above value of R_E, what will be the overall voltage gain v_o/v_i of the system?
(c) If R_E is by-passed by a large capacitance (negligible reactance), what voltage gain can be obtained?

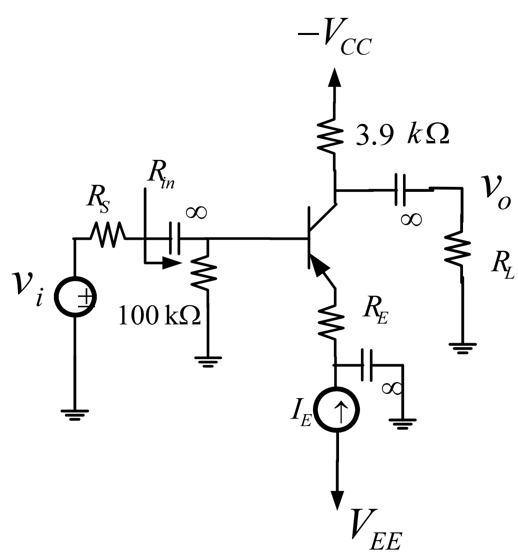


Figure 5:

Q.6: For the circuit shown (Figure 6)

(a) Draw the ac equivalent circuit for the amplifier.

(b) Find the voltage gain v_o/v_{sig} . Assume that the source provides a small signal v_{sig} with zero DC., and that β=100.

(c)What will be the maximum v_{sig} value for which the small signal approximation will remain valid?

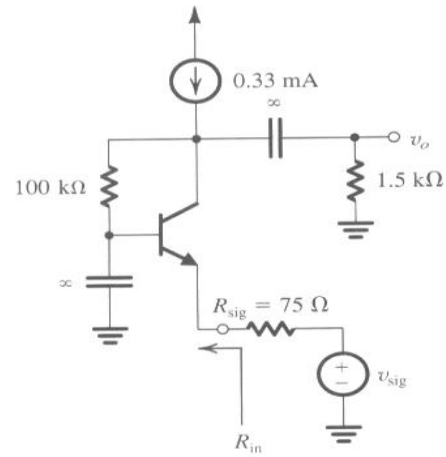


Figure 6:

Q.7: Consider the MOSFET amplifier in the figure below. Given that V_G= 4V V_{DD} =10 V, R_S=1 kΩ. The transistor has V_t= 1V, and $k_n'(W/L)$= 5 mA/V^2 .

(a) Find the bias current I_D through the MOS device.

(b) What will be the voltage gain $\mathbf{v_o}/v_{sig}$, if R_D =15 kΩ, R_{G1} = 2 MΩ, R_{G2} =1 MΩ,R_{sig} =10 kΩ?

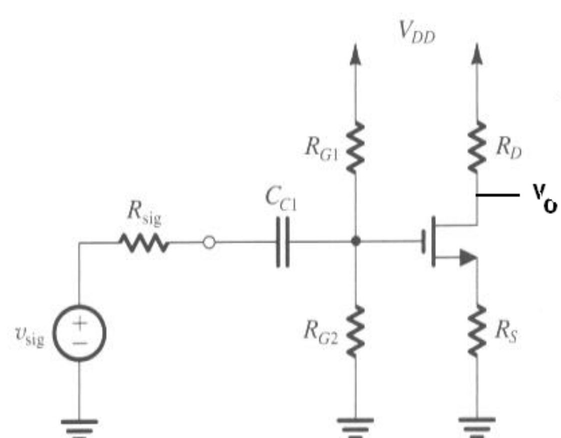


Figure 7:

Some important Formulas (BJT & MOSFET)

Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right) \qquad r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships Between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta+1 = \frac{1}{1-\alpha}$$

Overdrive voltage:

$$v_{OV} = v_{GS} - V_t$$
$$v_{GS} = V_t + v_{OV}$$

Operation in the *triode* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \geq V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{OV}$

- i-v Characteristics:

$$i_D = \mu_n C_{ox}\frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

- For $v_{DS} \ll 2(v_{GS} - V_t) \quad \Leftrightarrow \quad v_{DS} \ll 2v_{OV}$

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = 1\Big/\left[\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)\right]$$

Operation in the *saturation* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \leq V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{OV}$

- i-v Characteristics:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

- Transconductance:

$$g_m = \mu_n C_{ox}\frac{W}{L}V_{OV} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{OV}}$$

- Output resistance:

$$r_o = V_A/I_D = 1/\lambda I_D$$

Course		Number	Section
Electronics I		ELEC 311/1	BB
Examination	Date	Time	# of pages
Final	August 17, 2012	3 hours	6

Instructor(s)
Dr.R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use ENCS faculty approved calculators

Special Instructions:

You MUST attempt **Q.1** (*soft skill* component) .
For **Q.2-Q.8**, answer any **FIVE** questions.

Before submitting your answer book, **fill in the Table below** indicating the answers you want to be graded.
If you **do not** *fill in the Table*, the instructor will mark your answers *as they appear one after another in the answer book*

Show all steps clearly in neat and legible handwriting.
Students are required *to return the question paper* together with exam booklet(s).

Table (*Do not* forget to fill in!)

Answers to be graded	**Q.1 (compulsory)**					
Marks						

(Soft skill component- *The student MUST answer this question***)**

Q.1: Figure 1 depicts two NMOS transistors each with V_{THN} =0.5 V, K_n =0.5 mA/V^2, and W/L ratio of 4. The *early* voltage for M2 can be assumed to be *infinity.*

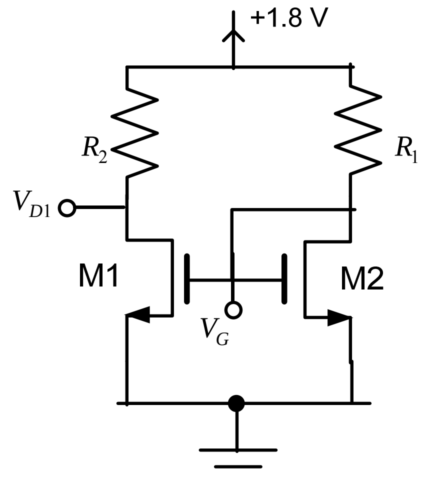


Figure 1

(a) Design R_1 so that V_G =0.7 V.
(b) Find R_2 so that M1 will be just at the edge of saturation region.
(c) What will be the current in M1 if it has an *early* voltage of 50 V?

(Answer **any FIVE** questions)

Q.2: A semiconductor junction diode **D** is used in an automatic gain control system as shown in **figure 2**. The ac resistance of the diode is dependent on the amplitude V_p of the input signal. The capacitance acts as a *short circuit* and the inductor acts as an *open circuit* for the *ac* signal.

The input signal is full-wave rectified to generate a DC voltage which drives the DC current through the diode. This DC voltage is given by $2V_p / \pi$. The diode is a 1 mA diode. The voltage drop across the diode changes by 100 milli volts for a decade (10 times) change in current through it. For the diode you may use the relation: $V_2 = V_1 + 2.303nV_T \log_{10}(I_2 / I_1)$, where V_T is the thermal voltage (=25 mV). The DC resistance of the diode can be neglected.

If the input ac signal has a peak amplitude of 10 volts, what will be the output signal magnitude v_o?

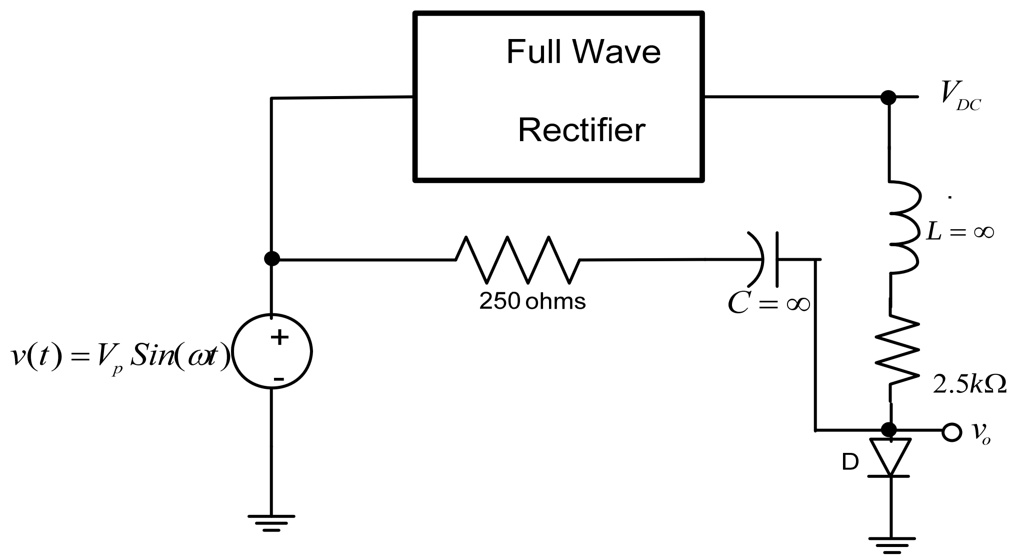


Figure 2

Q.3: The bridge-rectifier circuit in **figure 3** with a filter capacitor has R_L= 200 ohms. The secondary transformer delivers a sinusoid of 15 V (rms) and has a frequency of 60 Hz. The diodes have V_D = 0.8 V each.

(a) What will be the value of the filter capacitor so that the ripple voltage is limited to below 0.5 volts peak-to-peak?

(b) What is the DC voltage at the output of the system?

(c) What should be the PIV rating for the diodes?

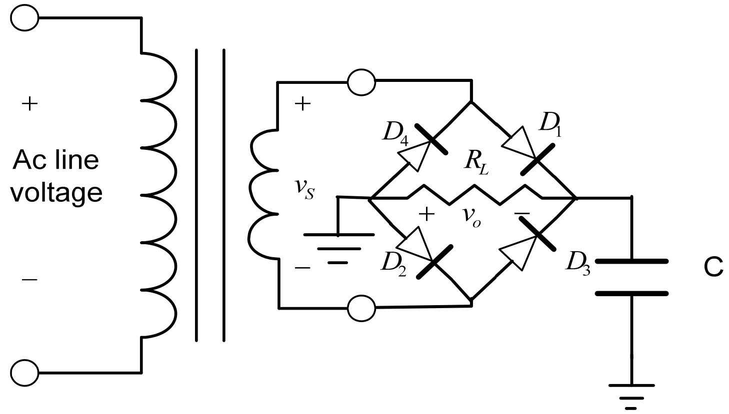


Figure 3

Q.4: Calculate the small signal gain v_o/v_s for the BJT amplifier circuit in **figure 4**. Assume transistor parameters of $\beta = 80$, V_{BE} (on) = 0.7 V, $V_A = 50V$.

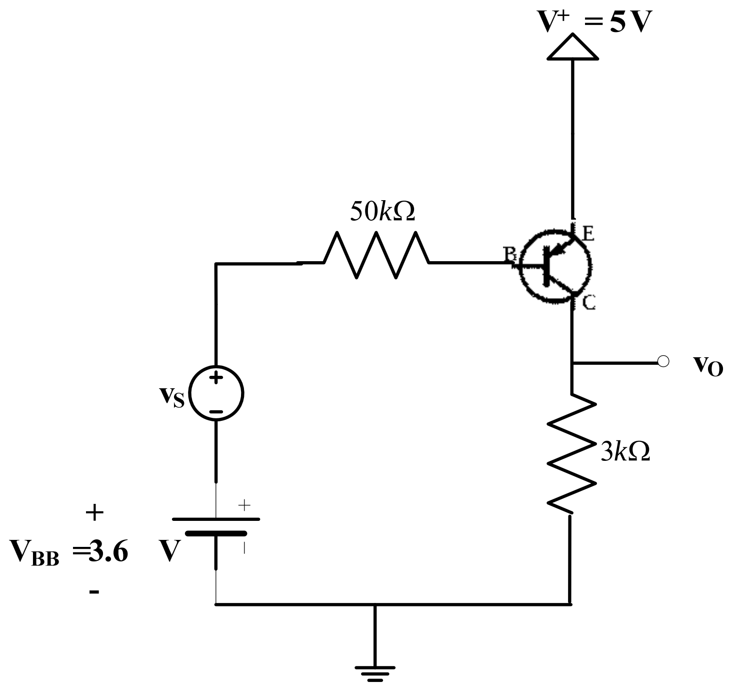


Figure 4

Q.5: Design (i.e., design the resistor values) a bias-stable PNP-BJT amplifier stage of **figure 5** to meet the following specifications.

The transistor Q-point values are to be: $V_{ECQ} = 6$ V, $I_{CQ} \approx 0.5$ mA and $V_{RE} \approx 2$ V. Assume transistor parameters of $\beta = 99$ and V_{BE} (ON) = 0.7 V.

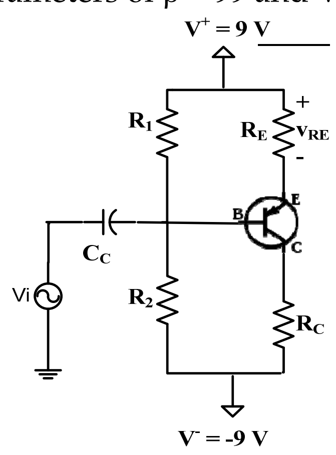


Figure 5

Find R_1, R_2, R_E, and R_C.

Q.6: For the circuit shown in **figure 6** find
(a) the input resistance R_{in} , and
(b) the voltage gain v_o/v_s . Assume that the source provides a small signal v_{sig} and that β =100.
(c) What will be the maximum v_s value for which the small signal approximation will remain valid?

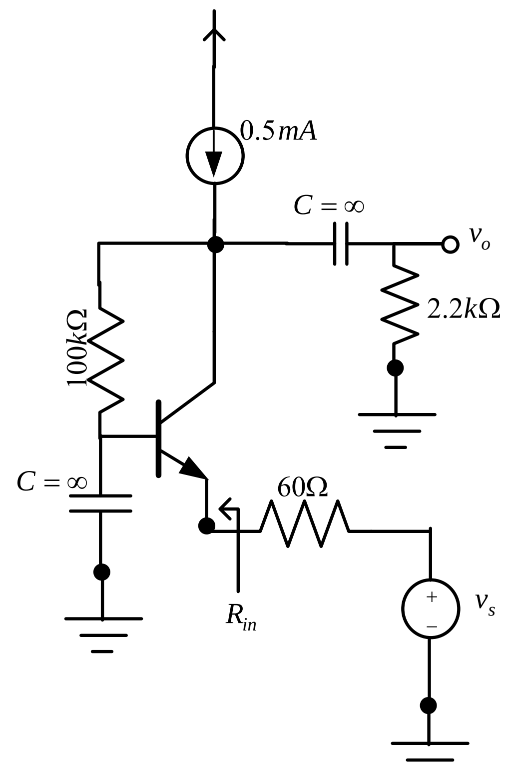


Figure 6

Q.7: A Common Source (CS) MOSFET amplifier is biased at I_D =0.25 mA with a current source connected at the Source terminal of the MOSFET. The transistor has V_{OV} =0.3 V, and a drain resistance of R_D =15 kΩ connected to the DC supply of 15 V. The device has V_A =50 V. The amplifier is capacitively fed from a source with internal resistance R_{sig} =100 kΩ, and a 20 kΩ load is capacitively coupled to the drain of the amplifier.

(a) Draw the schematic for the amplifier system.
(b) Calculate the voltage gain of the system.

Q.8: Consider **figure 8.** Calculate the labeled node voltages V_1 and V_2, given that the MOSFETs have V_{THN} =1 V, and $K_n \frac{W}{L} = 3$ mA/V^2.

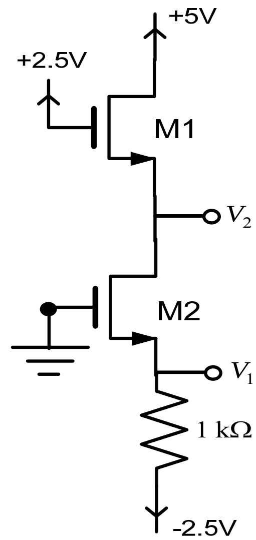
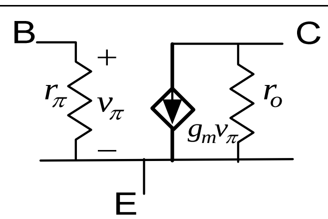
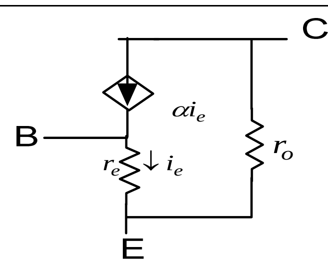
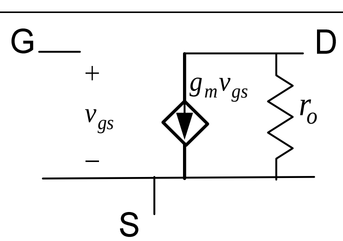
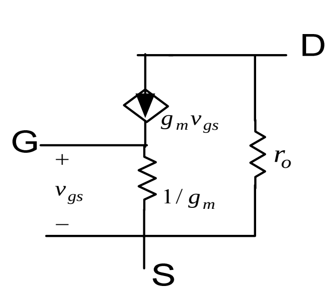


Figure 8

(Some formulae and equivalent circuits)

$I_C = \beta I_B$, $I_E = (\beta+1)I_B$	$g_m = \dfrac{I_C}{V_T}$, $r_\pi = \dfrac{\beta}{g_m}$, $\alpha = \dfrac{\beta}{\beta+1}$	$r_o = \dfrac{V_A}{I_C}$, $r_e = \dfrac{r_\pi}{\beta+1}$, $I_C = I_S \exp(V_{BE}/V_T)$
$I_D = k\left(\dfrac{W}{L}\right)\left((V_{GS}-V_t)V_{DS} - \dfrac{V_{DS}^{\;2}}{2}\right)$ (linear region)	$I_D = k\left(\dfrac{W}{2L}\right)(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$ (saturation region)	$g_m = k\left(\dfrac{W}{L}\right)(V_{Gs}-V_{TH}) = \sqrt{\dfrac{2kI_DW}{L}}$ $r_o = \dfrac{V_A}{I_D}$
 BJT hybrid pi	 BJT T	
 MOS hybrid pi	 MOS T	

Course	Number	Section
Electronics I	ELEC 311/2	F,U

Examination	Date	Time	# of pages
Final	December 13, 2012	3 hours	8

Instructor(s)

Dr.R. Raut, Dr. V. Ramachandran

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use ENCS faculty approved calculators

Special Instructions:

You are required to *answer* **SIX** questions

You MUST attempt **Q.1** (*soft skill* component) : **6 marks**

From **Q.2-Q.6**, answer any **THREE** questions.: **8 marks** (each)

From **Q.7**-**Q.10** answer any **TWO** questions: **10 marks** (each)

Before submitting your answer book, **fill in the Table below** indicating the answers you want to be graded.

(If you **do not** *fill in the Table*, the instructor will mark your answers *as they appear one after another in the answer book)*

Show all steps clearly in neat and legible handwriting.

Students are required *to return the question paper* together with exam booklet(s).

(STUDENT) NAME: **ID #**

Table

Answers to be graded	**Q.1 (compulsory)**					
Marks						

(**Some important formulae**)

$I_C = \beta I_B$, $I_E = (\beta+1)I_B$	$g_m = \frac{I_C}{V_T}$, $r_\pi = \frac{\beta}{g_m}$, $\alpha = \frac{\beta}{\beta+1}$	$r_o = \frac{V_A}{I_C}$, $r_e = \frac{r_\pi}{\beta+1}$, $I_C = I_S \exp(V_{BE}/V_T)$
$I_D = K\left(\frac{W}{L}\right)\left((V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right)$ (linear region)	$I_D = K\left(\frac{W}{2L}\right)(V_{GS}-V_{TH})^2$ (saturation region, excluding Early effect)	$g_m = K\left(\frac{W}{L}\right)(V_{GS}-V_{TH}) = \sqrt{\frac{2KI_D W}{L}}$ $r_o = \frac{V_A}{I_D}$

Section I (Compulsory): Soft skill component- *The student **MUST answer** this question*

Q. 1: The NMOS transistor in the circuit of Figure 1 have $V_{THN} = 1$ V, $K = 120$ μA/V^2 , $\lambda = 0$, and $L_1 = L_2 = L_3 = 1.5$μm. Find the required values of gate width for each of M_1, M_2, and M_3 to obtain the voltage and current values indicated. (**6 marks**).

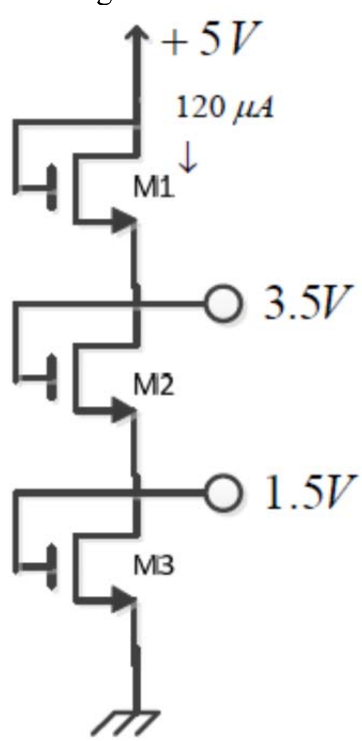


Figure 1:

Section II (From **Q.2-6,** answer <u>ONLY **three**</u> questions**)**

Q.2: The current-voltage relationship of a diode is given by

$$i_D = I_s\, e^{\frac{v_D}{V_T}}$$

where I_s is the scale current of the diode,

V_T is the thermal voltage = 25 mV at room temperature,

v_D is the voltage across the diode.

(a) What is the mA rating of the diode, given I_S= 10^{-15} amperes?
(b) Assuming that V_i = 0.7 V and v_s =0.05 Sin (360t) are applied to the diode (see Fig.2), draw the corresponding (i) DC model and (ii) the *ac* model of the diode.
(c) Using the above equivalent circuits, obtain the output voltage across the diode configured as in Fig.2.

(8 marks)

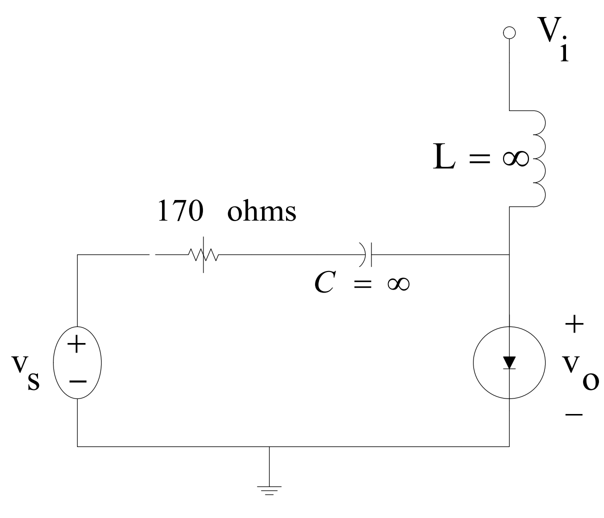


Figure 2:

Q.3: . Figure 3 shows an electronic amplifier employing a power *npn* BJT device.

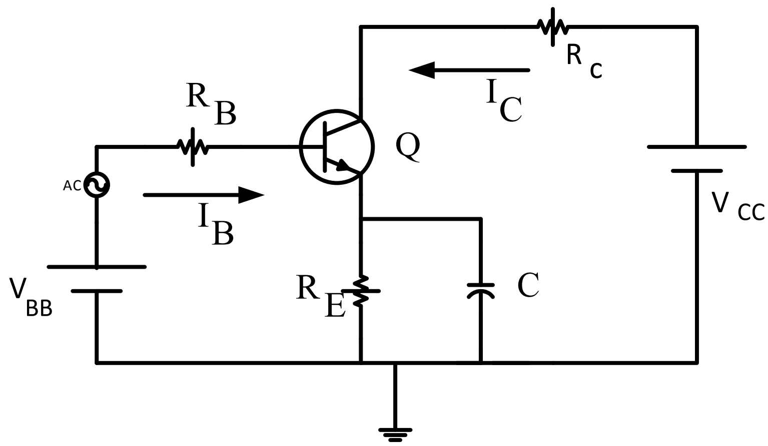


Figure 3:

It is given that V_{BB} = 6 V, V_{BE} = 0.7 V, V_{CC} = 80 V, R_B = 10,000 ohms, R_C = 5000 ohms, R_E=10,000 ohms, C→ ∞ and β of the transistor is 29.

(a) Verify that the transistor is in the active region.
(b) Draw the *ac* equivalent circuit, given V_A = 200 V. Label the calculated *ac* parameters.

(**8 marks**)

Q.4(a) Figure 4(a) shows a half-wave rectifier circuit. The diode D can be considered ideal.

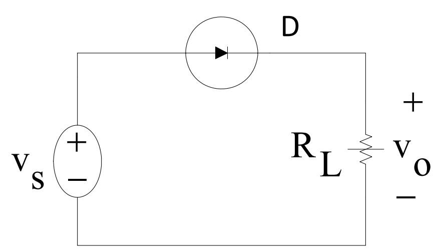


Figure 4(a):

The system data are: v_s (t)= 60 Cos[(120πt)] Volts and R_L = 100 kilo ohms.

(i) Obtain the DC component of v_o(t)
(ii) What is the peak inverse voltage across the diode?

(b) In the system shown in **Fig.4(a),** a capacitor of value 10 μF is connected across R_L, as shown in **Fig.4(b).**

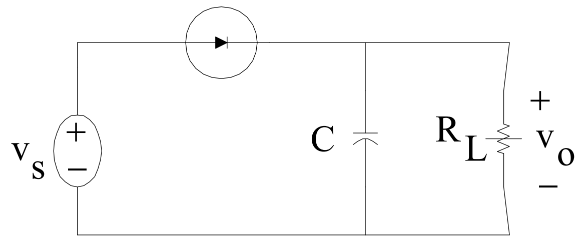


Figure 4(b):

(i) Sketch the waveform of v_o (t) and label the various values. Find the *ripple* voltage.
(ii) Determine the DC component of v_o(t).
(iii) What is the peak inverse voltage across the diode?
(iv) What should be the new value of C, if the *ripple* found in (i) is to be reduced to half the value?

(**8 marks**)

Q.5: Figure 5 shows a MOSFET circuit.

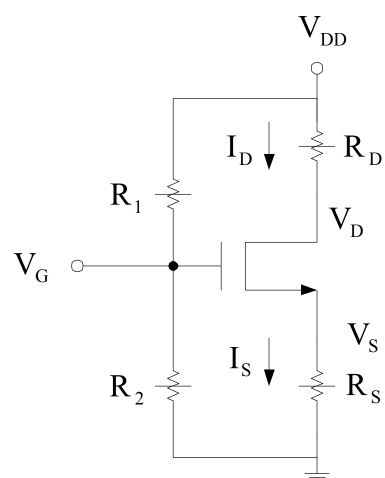


Figure 5:

The various component values are given by: R_1 = 200 kilo ohms, R_2 = 150 kilo ohms, R_D = 6 kilo ohms, R_S = 4.5 kilo ohms, V_{DD} = 10 volts. For the transistor, K = 200 $\mu A/V^2$, (W/L) = 5, V_{GS} = 1.1 V, V_{THN} = 0.7 V.

(a) Verify that the MOSFET is in the saturation region.
(b) Draw the complete *ac* equivalent circuit of Fig.5.

(8 marks)

Q.6: For the circuit shown in figure 6 assume that the source v_s provides a small signal v_{sig} and that the BJT has β=100.

Find:

(a) the input resistance R_{in} .

(b) What will be the maximum v_s value for which the small signal approximation will remain valid?

(8 marks)

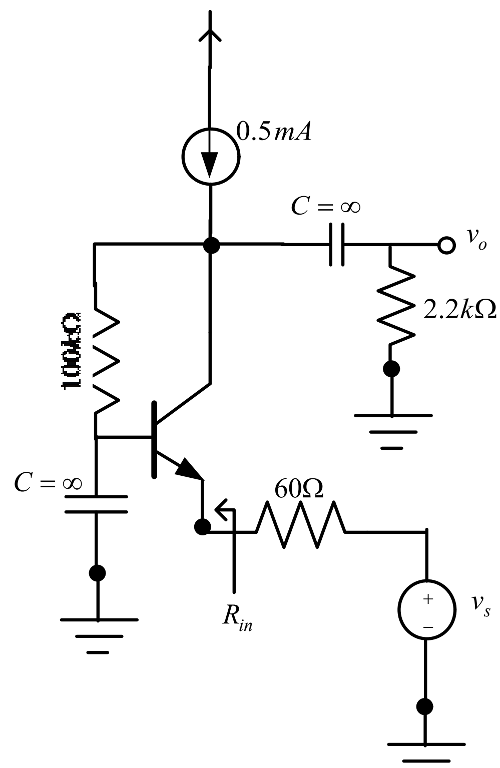


Figure 6:

Section III (From **Q.7-10,** answer <u>ONLY **two**</u> questions**)**

Q.7: Design (i.e., design the resistor values) a bias-stable PNP-BJT amplifier stage of figure 7 to meet the following specifications.

The transistor Q-point values are to be: $V_{ECQ} = 6$ V, $I_{CQ} \approx 0.5$ mA and $V_{RE} \approx 2$ V. Assume transistor parameters of $\beta = 99$ and V_{EB} (ON) = 0.7 V.

(10 marks)

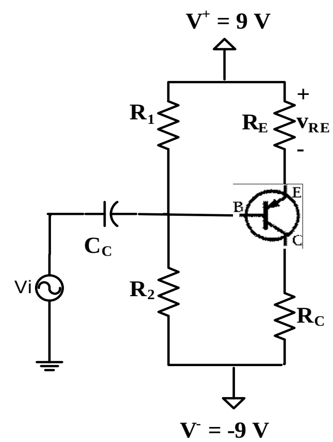


Figure 7:

Q.8: Consider the emitter-degenerated CE BJT amplifier circuit shown in figure 8. The signal source has a resistance R_s = 1 kΩ and the load R_L is 5 kΩ.

Given V_A = infinity, β =100, I_E = 2 mA.

(a) What value of R_E will make R_{in} =10 kΩ?
(b) With the above value of R_E, what will be the overall voltage gain v_o/v_i of the system?
(c) If R_E is by-passed by a large capacitance (negligible reactance), what voltage gain can be obtained?

(10 marks)

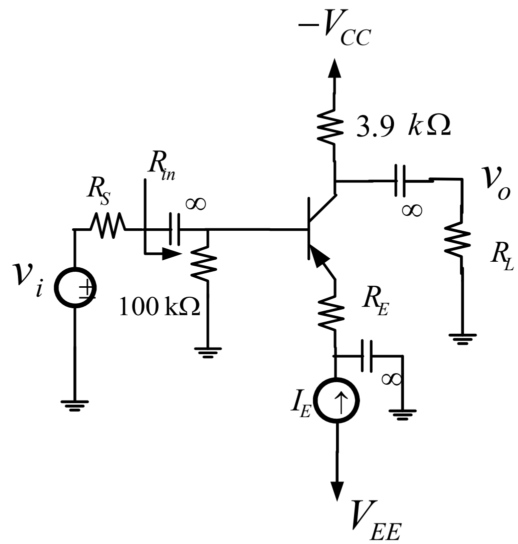


Figure 8:

Q.9: A Common Drain (CD) MOSFET amplifier is biased at I_D =0.25 mA with a current source connected at the Source terminal of the MOSFET. The transistor has V_{OV} =0.3 V, and a load resistance of 15 kΩ is connected to the source terminal via a coupling capacitance of *infinite* value. The device has V_A =50 V. The amplifier is fed from a source with internal resistance R_{sig} =100 kΩ via a coupling capacitor of *infinite* value.

(a) Draw the schematic diagram for the amplifier system.
(b) Calculate the voltage gain of the system.

(10 marks)

Q.10: Figure 10 presents a Common Gate MOS amplifier as an integrated circuit. The transistor M0 provides a bias current of 0.5 mA. The output resistance of M0 can be *assumed as infinity*. Assume that for M2, K_P=100 μA/V^2, and for M1, K_n = 300 μA/V^2. Further, for M2, V_{Ap}= -40 V, and for M1, V_{An}=30 V. Given that V_{THN} =|-V_{THP}|=1V, and W/L=2 for all the transistors. The body transconductance g_{mb} of M1 can be ignored.

M1 is the *driver* transistor, and M2 serves as the active load. V_{DD} =|-V_{SS}|= 10 V.

Draw the *ac* equivalent circuit, and then find the voltage gain v_o/v_{in} for the amplifier.

(10 marks)

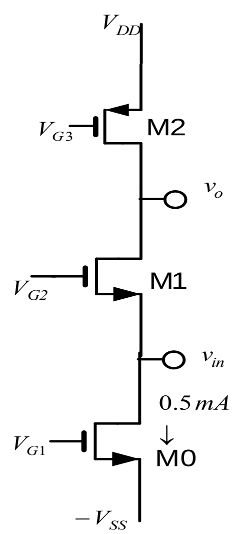


Figure 10:

Course	Number	Section
Electronics I	ELEC 311/1	BB

Examination	Date	Time	# of pages
Final	August 21, 2013	3 hours	7

Instructor(s)

Dr.R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use **ONLY** ENCS faculty approved calculators

Special Instructions:

You are required to *answer* **SIX** questions

You MUST attempt **Q.1** (*soft skill* component) : **5 marks**

From **Q.2-Q.8**, answer any **FIVE** questions.: **9 marks** (each)

Before submitting your answer book, **fill in the Table below** indicating the answers you want to be graded.

(If you **do not** *fill in the Table*, the instructor will mark your answers *as they appear one after another in the answer book)*

Show all steps clearly in neat and legible handwriting.

Students are required *to return the question paper* together with exam booklet(s).

(STUDENT) NAME: **ID #**

Table

Answers to be graded	**Q.1 (compulsory)**					
Marks						

(**Some important formulae**)

$I_C = \beta I_B$, $I_E = (\beta+1)I_B$	$g_m = \frac{I_C}{V_T}$, $r_\pi = \frac{\beta}{g_m}$, $\alpha = \frac{\beta}{\beta+1}$	$r_o = \frac{V_A}{I_C}$, $r_e = \frac{r_\pi}{\beta+1}$, $I_C = I_S \exp(V_{BE}/V_T)$
$I_D = K\left(\frac{W}{L}\right)\left((V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right)$ (linear region)	$I_D = K\left(\frac{W}{2L}\right)(V_{GS}-V_{TH})^2$ (saturation region, excluding Early effect)	$g_m = K\left(\frac{W}{L}\right)(V_{Gs}-V_{TH}) = \sqrt{\frac{2KI_D W}{L}}$ $r_o = \frac{V_A}{I_D}$

Section I (Compulsory): Soft skill component- *The student **MUST answer** this question*

Q. 1: For the MOS circuit shown in **Fig.1**, find V_1, and V_2. For the NMOS transistors V_{TH}=1V, K =1mA/V^2, W/L=8.

(**5 marks**).

Figure 1:

Section II (From **Q.2-8,** answer <u>ONLY **FIVE**</u> questions**)**

Q.2: A given shunt regulator system is driven by a raw DC voltage source of 10 V (nominal) with a variation of ±1 V. The diode is a 6.8 V Zener at an operationg current of 5 mA, with r_Z =20 Ω, and $I_{ZK(Min)}$ =0.2 mA. The line resistance used is 500 Ω. Calculate the following, with supporting circuit analysis. A circuit model for the diode is shown in **Fig.2.**

(a) Draw the equivalent circuit for the whole system.
(b) Calculate the line regulation and the amount of fluctuation of the output voltage when the input fluctuates by ±1 V.
(c) Find the output voltage if a 500 Ω resistance is connected as the load to the system.

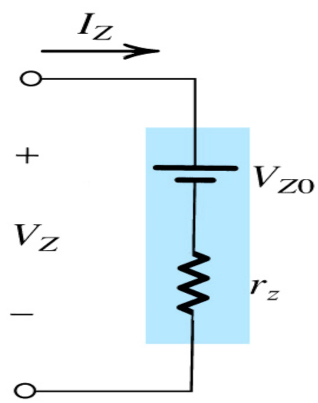


Figure 2:

(9 marks)

Q.3(a) : Figure 3(a) shows a half-wave rectifier circuit. The diode D can be considered ideal.

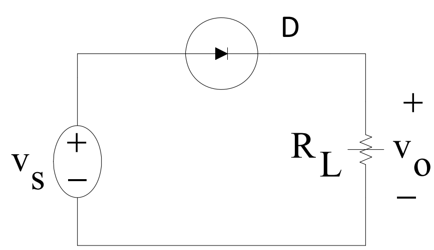


Figure 3(a):

Given: v_s (t)= 60 Cos[(120πt)] Volts and R_L = 100 kilo ohms.

(i) Obtain the DC component of v_o(t)
(ii) What is the peak inverse voltage across the diode?

Q.3(b): In the system shown in **Fig.3(a),** a capacitor of value 10 μF is connected across R_L, as shown in **Fig.3(b).**

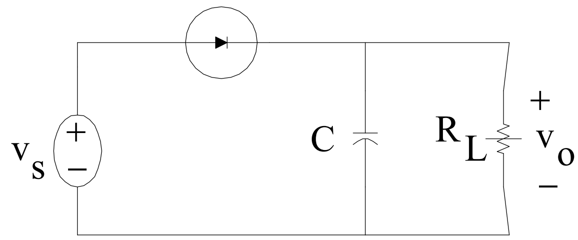


Figure 3(b):

(i) Sketch the waveform of $v_o(t)$ and label the various values. Find the *ripple* voltage.
(ii) Determine the DC component of $v_o(t)$.
(iii) What should be the new value of C, if the *ripple* found in (i) is to be reduced to half the value?

(**9 marks**)

Q.4: Calculate the small signal gain v_o/v_s for the BJT amplifier circuit in **Fig. 4**. Assume transistor parameters of $\beta = 99$, V_{BE} (on) = 0.7 V, V_A = 50V.

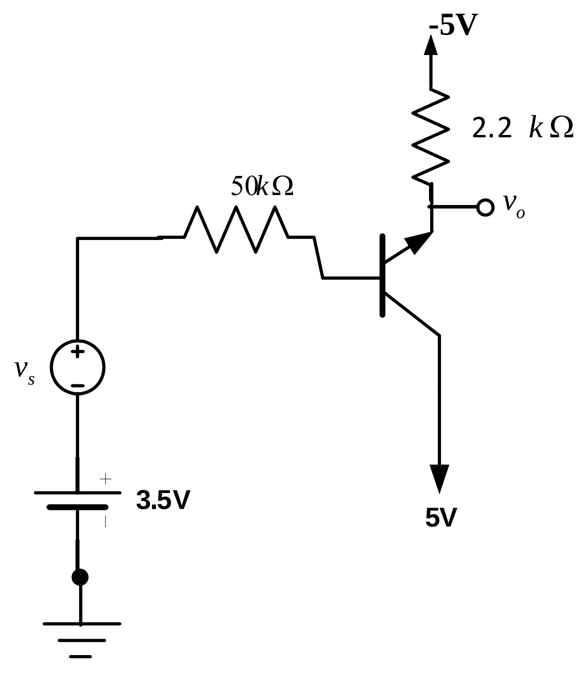


Figure 4

(9 marks)

Q.5: For the circuit shown in figure 5 assume that the source v_s provides a small signal v_{sig} and that the BJT has β=49. Find:

(a) the input resistance R_{in} .

(b) What will be the maximum v_s value for which the small signal approximation will remain valid for the operation of the BJT?

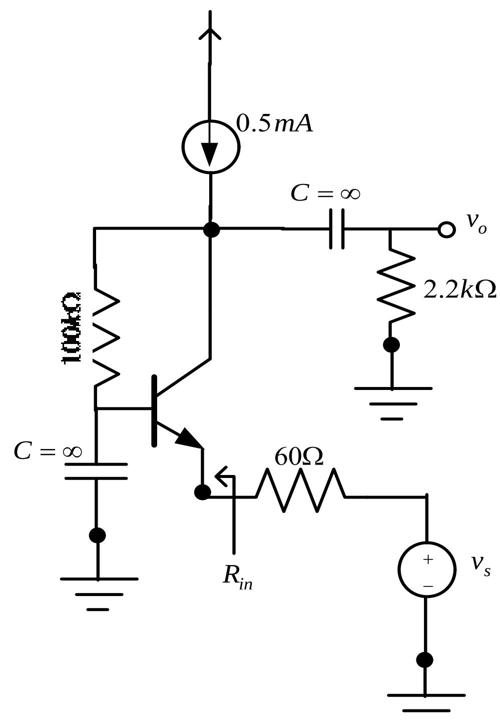


Figure 5:

(**9 marks**)

Q.6: A common emitter amplifier uses a BJT device with β=100, *Early* voltage =50 V, and is biased by a current source at *I* =5 mA. The amplifier operates between a voltage source with R_{sig} =10,000 ohms, and a resistance R_C of 1000 ohms at the collector. Figure 6 shows the schematic diagram.

(a) Draw the *ac* equivalent circuit and find the voltage gain of the system.

(b) What is the *small signal* current gain of the system?

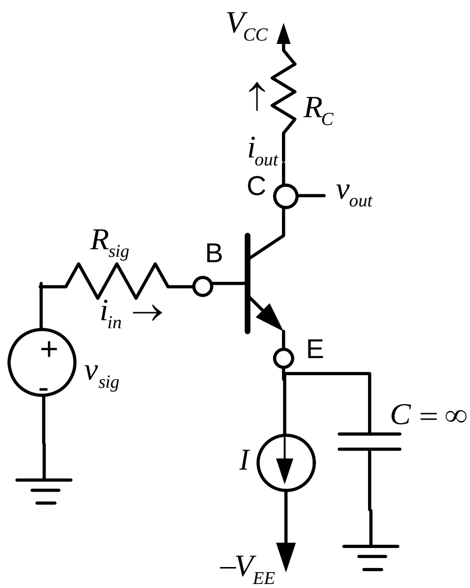


Figure 6

(9 marks)

Q.7: Consider figure 7 as the conceptual model of a MOSFET circuit operating as a common source amplifier. Given that V_{TH} =0.5V, K=5 mA/V^2, W/L =2, V_{GS} =0.7V, V_{DD} =2V, R_D =5000 ohms, and V_A (*Early* voltage) =50V;

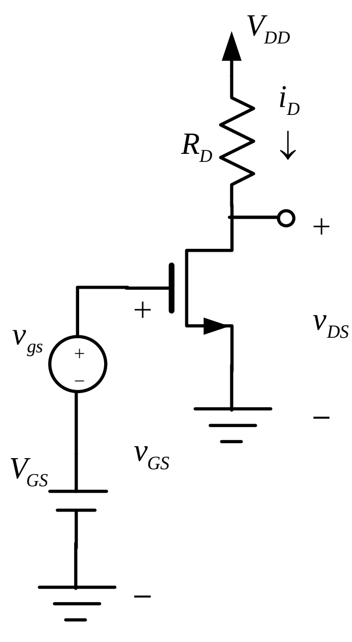


Figure 7

Calculate:

(a) The *ac* transconductance of the MOS device
(b) The small signal voltage gain of the system.

(9 marks)

Q.8: Figure 8 presents a common gate MOS amplifier as an integrated circuit. The transistor M0 provides a bias current of 0.5 mA. The body transconductance g_{mb} is approximately $0.2g_m$ of the transistor M1, which is the *driver* transistor. M2 serves as an active load. Find the voltage gain v_o/v_{in} for the amplifier in terms of the *ac* equivalent circuit parameters.

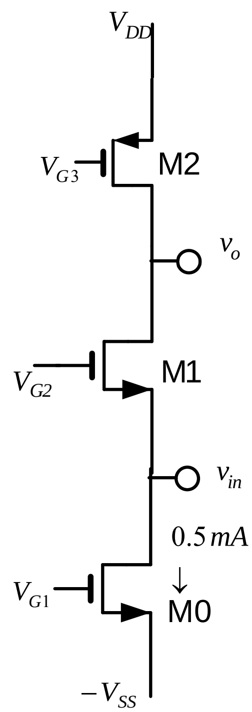


Figure 8

(9 marks)

Examination Cover Sheet

COURSE: ELEC	**NUMBER**: 311	**SECTION(S)**: **F**	
EXAMINATION: _X__ **FINAL** __ **ALTERNATE** ___ **DEFERRED** **VERSION**: __________	**DATE**: Dec.16, 2014	**TIME**: 14:00-17:00 **Exam Length: 3 hours**	**PAGES**: Including cover Seven
INSTRUCTOR(S: R. Raut		**DIVISION**:	
MATERIALS ALLOWED: __X__ Booklets ____ IBM (Scantron) ___ Blue ___ Green ____ Printed Translation Dictionary Other_________ __X__ Calculator _X__ENCS Approved ____ Other _______________________________________		**INSTRUCTIONS:** _X__ Return all ___ Answer on Exam ___ Open book ___ Crib sheet Details_______________	

Please print your name, I.D. number and section in the appropriate spaces below.

STUDENT NAME: ____

I.D. NO. _________________________ **SECTION**: __________________________________

SPECIAL INSTRUCTIONS:
(on next page)

Course

Electronics I

Examination: Final

Date: December 16, 2014

Instructor(s): Dr.R. Raut

Materials allowed: [X] No [ ] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed to use ENCS faculty approved calculator

Special Instructions:

You are required to <u>*answer* **SIX** questions</u>

You MUST attempt **Q.1** (*soft skill* component) : **5 marks**

From **Q.2-Q.8**, answer any **FIVE** questions.: **9 marks** (each)

Before submitting your answer book, **<u>fill in the Table below</u>** in

(If you **do not** *fill in the Table*, the instructor will mark your ansv

answer book)

Show all steps clearly in neat and legible handwriting.

Students are required *to return the question paper* together wit

(STUDENT) NAME: **ID #**

Table

Answers to be graded	**Q.1 (compulsory)**					
Marks						

Section I (Compulsory): <u>Soft skill component</u>**-** *The student* ***MUST answer*** *this question*

Q. 1:Consider **figure 1.** Calculate the labeled node voltages V_1 and V_2, given that the MOSFETs have $V_{THN}=1$ V, and $K\frac{W}{L}=5\,mA/V^2$. (**5 marks**)

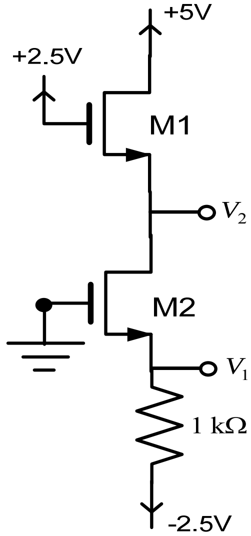


Figure 1

(**Some important formulae**)

BJT	$I_C=\beta I_B$, $I_E=(\beta+1)I_B$	$g_m=\frac{I_C}{V_T}$, $r_\pi=\frac{\beta}{g_m}$, $\alpha=\frac{\beta}{\beta+1}$	$r_o=\frac{V_A}{I_C}$, $r_e=\frac{r_\pi}{\beta+1}$, $I_C=I_S\exp(V_{BE}/V_T)$
MOS	$I_D=K\left(\frac{W}{L}\right)\left((V_{GS}-V_t)V_{DS}-\frac{V_{DS}^2}{2}\right)$ (linear region)	$I_D=K\left(\frac{W}{2L}\right)(V_{GS}-V_{TH})^2$ (saturation region, excluding Early effect)	$g_m=K\left(\frac{W}{L}\right)(V_{GS}-V_{TH})=\sqrt{\frac{2KI_DW}{L}}$ $r_o=\frac{V_A}{I_D}$

Section II (From **Q.2-8,** answer <u>ONLY **FIVE**</u> questions**)**

Q.2: Consider the BJT amplifier in Fig.2.
Find the DC operating points (i.e., I_C, I_E) for the amplifier stage. The transistor has β=75. Assume V_{BE} =0.7V. **(9 marks)**

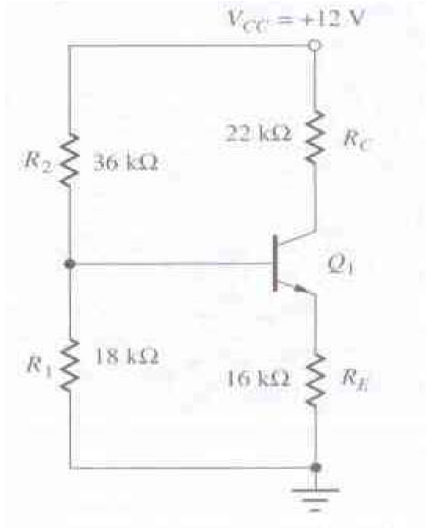
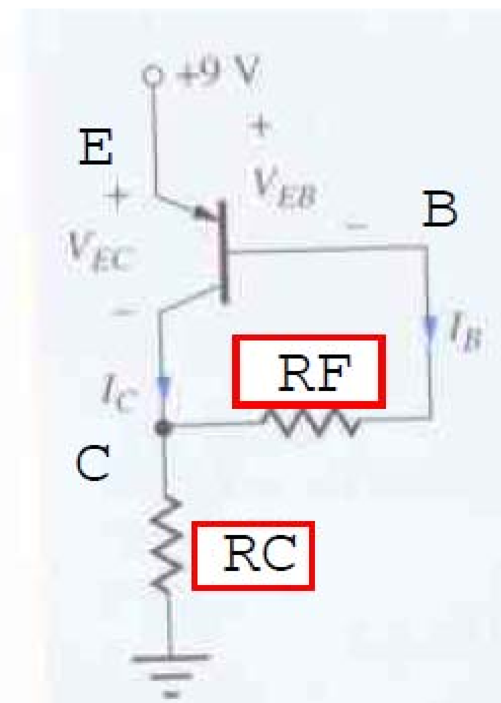
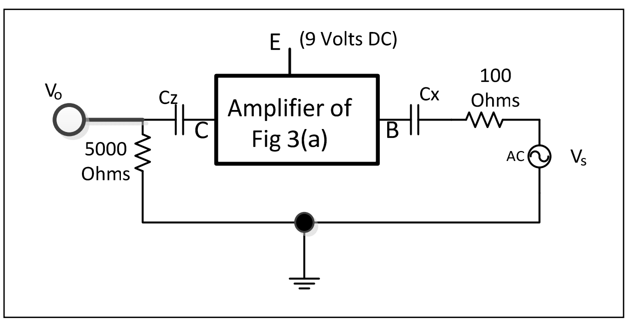


Figure 2:

Q.3: In Fig.3(a) the resistor RF and RC establish the DC operating point for the amplifier.
(a) Design RC and RF so that I_C =6 mA is achieved. Given V_{EB} =0.7V, and β=50.
(b) The amplifier of Fig 3(a) is connected between a signal voltage source V_S and a load resistance of 5000 ohms as in Fig.3(b). The terminals B,C,E in Fig. 3(b) correspond to the identical terminals in Fig. 3(a). Using the *small signal* ac equivalent circuit for the BJT find the *small* signal voltage gain V_O / V_S. The capacitors C_X, and C_Z can be assumed to be very large (i.e., *infinity*) in values. **(9 marks)**



(a)



(b)

Figure 3:

Q.4: Consider the emitter-follower BJT amplifier circuit of Fig.4. Find R_{in}, R_{out} and the voltage gain v_o/v_{sig}. Given R_{sig} = 10 kΩ, R_B = 40 kΩ, R_L = 1 kΩ, β=49, and V_A = 100 V. The bias current source is *ideal* with I = 5 mA. Further V_{CC} =|-V_{EE}| =10 volts (DC).

(**9 marks**)

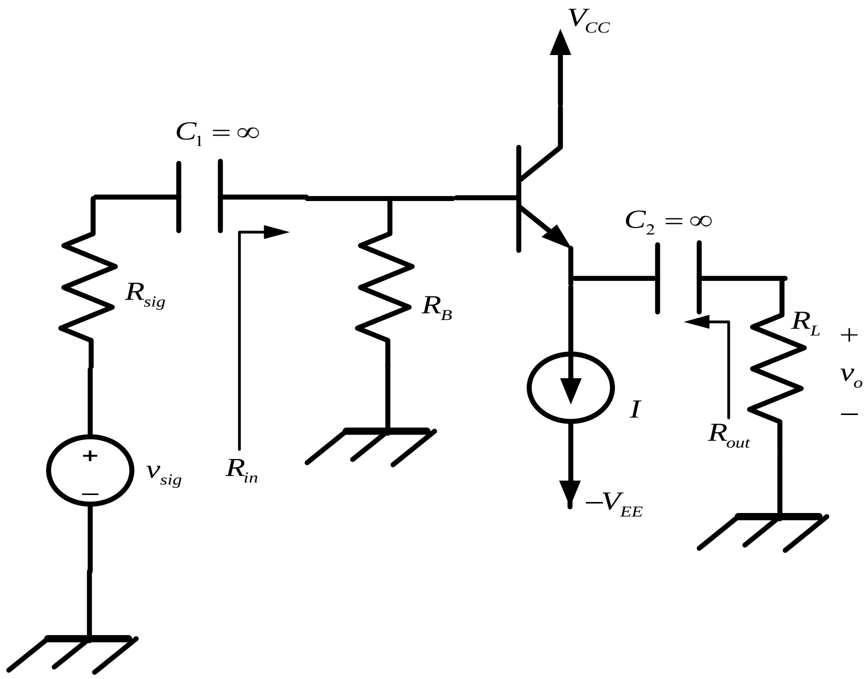


Figure 4:

(**Some important formulae**)

BJT	$I_C = \beta I_B$, $I_E = (\beta+1)I_B$	$g_m = \frac{I_C}{V_T}$, $r_\pi = \frac{\beta}{g_m}$, $\alpha = \frac{\beta}{\beta+1}$	$r_o = \frac{V_A}{I_C}$, $r_e = \frac{r_\pi}{\beta+1}$, $I_C = I_S \exp(V_{BE}/V_T)$

Q.5: Figure 5 shows a *common source* MOSFET amplifier circuit with the DC quantities shown alongside the schematic. (**9 marks**)

(**Some important formulae**)

MOS	$I_D = K\left(\frac{W}{L}\right)\left((V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right)$ (linear region)	$I_D = K\left(\frac{W}{2L}\right)(V_{GS} - V_{TH})^2$ (saturation region, excluding Early effect)	$g_m = K\left(\frac{W}{L}\right)(V_{GS} - V_{TH}) = \sqrt{\frac{2KI_DW}{L}}$ $r_o = \frac{V_A}{I_D}$

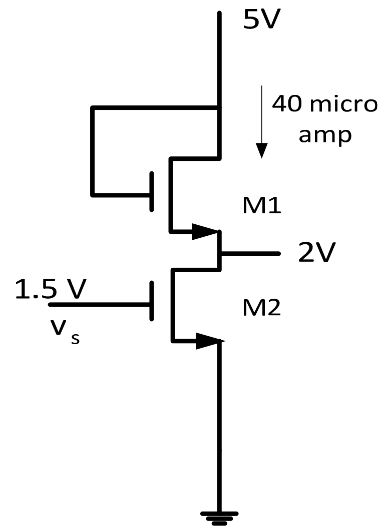


Figure 5:

For the NMOS transistors, $K = 40\ \mu A/V^2$, $V_{THN} = 1$ V.

(a) Verify that the MOSFET is in the saturation region.

(b) Find the width *W* values for M1 and M2, given that *L*=1 micro meters for each of the transistors.

(c) Draw the complete *ac* equivalent circuit associated with the schematic. Ignore the *body* transconductance.

Q.6: The bridge-rectifier (see Fig.6) circuit with a filter capacitor has $R_L = 100$ ohms. The secondary transformer delivers a sinusoid of 15 V (rms) and has a frequency of 60 Hz. The diodes have $V_{DO} = 0.7$ V each.

(a) What will be the value of the filter capacitor so that the ripple voltage is limited to below 500 mV peak-to-peak?

(b) What is the DC voltage at the output of the system?

(c) What is the conduction angle for each diode in the system? Explain with appropriate sketches.

(9 marks)

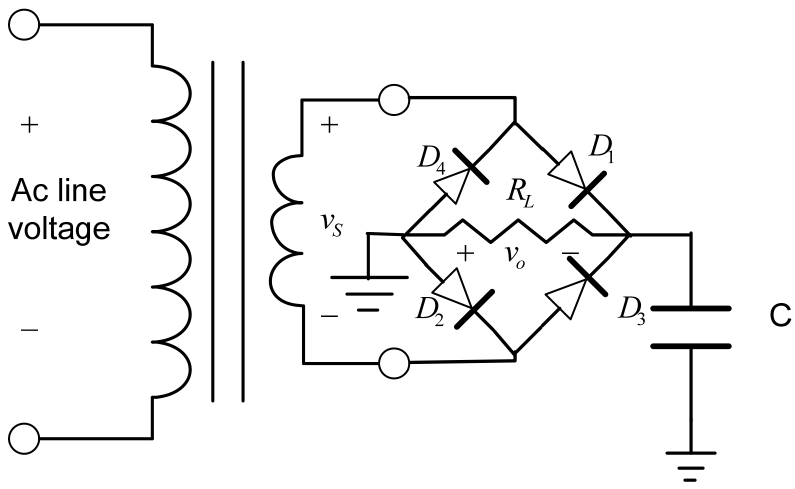


Figure 6:

Q.7: A Common Source (CS) MOSFET amplifier is biased at I_D =0.25 mA with a current source connected at the Source terminal of the MOSFET. The transistor has V_{OV} =0.3 V, and a drain resistance of R_D =15 kΩ connected to the DC supply of 15 V. The device has V_A =50 V. The amplifier is capacitively fed from a source with internal resistance R_{sig} =100 kΩ, and a 20 kΩ load is capacitively coupled to the drain of the amplifier.

(a)Draw the schematic for the amplifier system.
(b)Calculate the voltage gain of the system.

(9 marks)

(Some important formulae)

MOS	$I_D = K\left(\frac{W}{L}\right)\left((V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right)$ (linear region)	$I_D = K\left(\frac{W}{2L}\right)(V_{GS} - V_{TH})^2$ (saturation region, excluding Early effect)	$g_m = K\left(\frac{W}{L}\right)(V_{Gs} - V_{TH}) = \sqrt{\frac{2KI_D W}{L}}$ $r_o = \frac{V_A}{I_D}$

Q.8: A semiconductor junction diode **D** is used in an automatic gain control system as shown in **figure 8**. The ac resistance of the diode is dependent on the amplitude of the input *ac* signal. The capacitance acts as a *short circuit* and the inductor acts as an *open circuit* for the *ac* signal.
The input signal is full-wave rectified to generate a DC voltage which drives the DC current through the diode. This DC voltage is given by $2V_p / \pi$, where V_p is the peak value of the signal. The diode is a 1 mA diode. For the diode you may use the relation: $V_2 = V_1 + 2.303 V_T \log_{10}(I_2 / I_1)$, where V_T is the thermal voltage (=25 mV). The DC resistance of the diode can be neglected.
If the input *ac* signal has a peak amplitude of 15 volts, what will be the output *ac* signal amplitude v_o?

(9 marks)

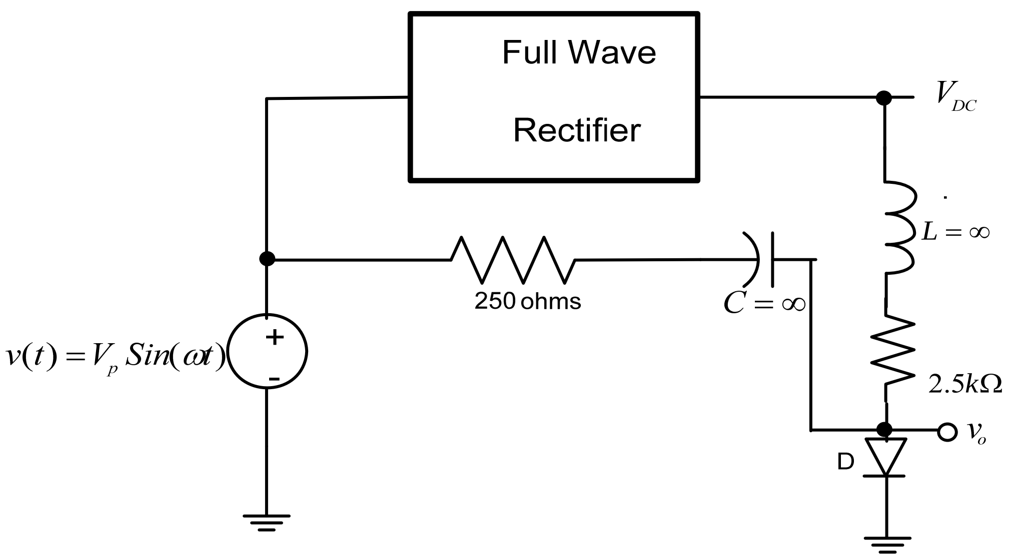


Figure 8: