

CEG2136: Computer Architecture I
CEG2536: Architecture des Ordinateurs I

**MIDTERM EXAMINATION
SOLUTIONS**

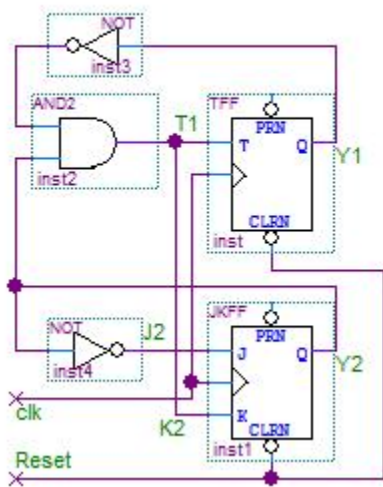
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Duration: 1 hour and 20 minutes

October 23, 2015@16:00

Question 1 (20 points)

A sequential circuit is presented below:



- a. Find the equations of the inputs J2, K2, and T1 of the two flip-flops
 $T1 = K2 = Y2 Y1'$
 $J2 = Y2'$

- b. If the system's initial state is $Y2 = Y1 = 0$, derive the transition table and then draw the state diagram.

Use the FF's Characteristic Tables to derive the transition table of the sequential circuit :

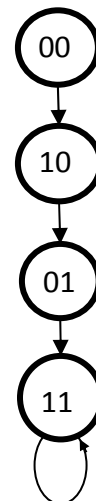
J	K	$Q(n+1)$
0	0	$Q(n)$
0	1	0
1	0	1
1	1	$Q(n)'$

T	$Q(n)$	$Q(n+1)$
0	0	0
0	1	1
1	0	1
1	1	0

transition table

$Y2(n)$	$Y1(n)$	J_2	K_2	T1	$Y2(n+1)$	$Y1(n+1)$
0	0	1	0	0	1	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	1	1

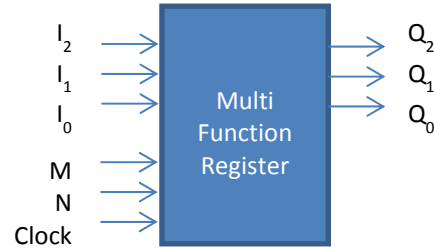
state diagram



Question 2 (20 points)

Design a 3-bit register whose function is described in the following table, where M and N are two control bits. Using the proper digital components (encoders, decoders, multiplexers, etc.), logic gates, and D flip-flops, draw a detailed diagram of the logic circuit of the register.

Clock	M	N	Operation
↑	0	0	No change
↑	0	1	Loading external inputs, say $I_2 I_1 I_0$
↑	1	0	Increment by 3
↑	1	1	Decrement by 1



Use the D Flip Flop Excitation equation ($D_i = Q_i(n+1)$ for $i=1,2,3$) or table:

$Q(n)$	$Q(n+1)$	D	M	N	Next State Equations:	D_i for $i=1,2,3$
0	0	0	0	0	$Q_i(n+1) = Q_i(n)$ for $i=1,2,3$	$D_i = Q_i$
0	1	1	0	1	$Q_i(n+1) = I_i$ for $i=1,2,3$	$D_i = I_i$
1	0	0	1	0	$Q_2(n+1)Q_1(n+1)Q_0(n+1) = [Q_2(n)Q_1(n)Q_0(n)] + 3$?
1	1	1	1	1	$Q_2(n+1)Q_1(n+1)Q_0(n+1) = [Q_2(n)Q_1(n)Q_0(n)] - 1$?

Control MN	Present State			Next State			Excitation Equations			
	$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	D_2	D_1	D_0	
00	0	0	0	0	0	0	0	0	0	$D_2 = Q_2$ $D_1 = Q_1$ $D_0 = Q_0$
	0	0	1	0	0	1	0	0	1	
	0	1	0	0	1	0	0	1	0	
	0	1	1	0	1	1	0	1	1	
	1	0	0	1	0	0	1	0	0	
	1	0	1	1	0	1	1	0	1	
	1	1	0	1	1	1	1	1	0	
	1	1	1	1	1	1	1	1	1	
01	0	0	0	I_2	I_1	I_0	I_2	I_1	I_0	$D_2 = I_2$ $D_1 = I_1$ $D_0 = I_0$
	0	0	1	I_2	I_1	I_0	I_2	I_1	I_0	
	0	1	0	I_2	I_1	I_0	I_2	I_1	I_0	
	0	1	1	I_2	I_1	I_0	I_2	I_1	I_0	
	1	0	0	I_2	I_1	I_0	I_2	I_1	I_0	
	1	0	1	I_2	I_1	I_0	I_2	I_1	I_0	
	1	1	0	I_2	I_1	I_0	I_2	I_1	I_0	
	1	1	1	I_2	I_1	I_0	I_2	I_1	I_0	
10	0	0	0	0	1	1	0	1	1	$D_2 = Q_2'(Q_0+Q_1) + Q_2Q_1'Q_0'$ $= Q_2 \oplus (Q_1+Q_0)$ $D_1 = Q_1'Q_0' + Q_1Q_0$ $D_0 = Q_0'$
	0	0	1	1	0	0	1	0	0	
	0	1	0	1	0	1	1	0	1	
	0	1	1	1	1	0	1	1	0	
	1	0	0	1	1	1	1	1	1	
	1	0	1	0	0	0	0	0	0	
	1	1	0	0	0	0	0	0	1	
	1	1	1	0	1	0	0	1	0	

MN	$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	D_2	D_1	D_0	
11	0	0	0	1	1	1	1	1	1	
	0	0	1	0	0	0	0	0	0	$D_2 = Q_2(Q_0+Q_1) + Q_2'Q_1'Q_0'$ $= Q_2 \odot (Q_1+Q_0)$
	0	1	0	0	0	1	0	0	1	
	0	1	1	0	1	0	0	1	0	$D_1 = Q_1'Q_0'+Q_1Q_0$
	1	0	0	0	1	1	0	1	1	
	1	0	1	1	0	0	1	0	0	$D_0 = Q_0'$
	1	1	0	1	0	1	1	0	1	
1	1	1	1	1	1	0	1	0		

MN = 10

D_2

Q_1	Q_0	00	01	11	10
Q_2					
0		0	1	1	1
1		1	0	0	0

$D_2 = Q_2'Q_1 + Q_2'Q_0 + Q_2Q_1'Q_0'$
 $D_2 = Q_2 \oplus (Q_0 + Q_1)$

D_1

Q_1	Q_0	00	01	11	10
Q_2					
0		1	0	1	0
1		1	0	1	0

$D_1 = Q_1'Q_0' + Q_1Q_0 = Q_1 \odot Q_0$
 $D_1 = (Q_1 \oplus Q_0)'$

D_0

Q_1	Q_0	00	01	11	10
Q_2					
0		1	0	0	1
1		1	0	0	1

$D_0 = Q_0'$

MN = 11

D_2

Q_1	Q_0	00	01	11	10
Q_2					
0		1	0	0	0
1		0	1	1	1

$D_2 = Q_2Q_1 + Q_2Q_0 + Q_2'Q_1'Q_0'$
 $D_2 = (Q_2 \oplus (Q_0 + Q_1))'$

D_1

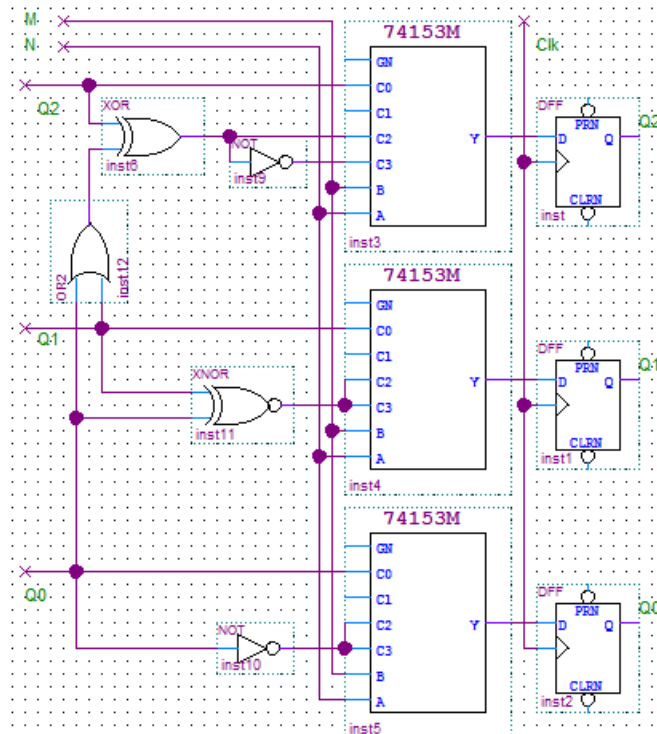
Q_1	Q_0	00	01	11	10
Q_2					
0		1	0	1	0
1		1	0	1	0

$D_1 = Q_1'Q_0' + Q_1Q_0 = Q_1 \odot Q_0$
 $D_1 = (Q_1 \oplus Q_0)'$

D_0

Q_1	Q_0	00	01	11	10
Q_2					
0		1	0	0	1
1		1	0	0	1

$D_0 = Q_0'$



Question 3 (30 points)

The 2's complement representation is used in an 8-bit register which contains the binary value 10011100.

- a. What is the register value after an arithmetic shift right? Give your result both in binary and decimal.

	Binary								Decimal
R	1	0	0	1	1	1	0	0	-100 ₁₀
R >>	1	1	0	0	1	1	1	0	-50 ₁₀

- b. Starting again from the initial number 10011100, determine the register value after an arithmetic shift left, both in binary and decimal.

	Binary								Decimal
	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0	
R	1	0	0	1	1	1	0	0	-100 ₁₀
<< R	0	0	1	1	1	0	0	0	+56 ₁₀

- c. What arithmetic operations are performed by these shifts?

a = division by 2

b = multiplication by 2

- d. Is there any overflow? Justify your answer.

R >> Shifting to the right is equivalent to dividing by 2, which may NOT create any overflow.

<< R Shifting to the left is equivalent to multiplication with 2, which may create overflow.

In our case:

$R = -100$

$\ll R = +56 \Rightarrow$ **overflow**

As signed numbers \Rightarrow if changes the sign \Rightarrow BAD! OFL

Or, remember:

An overflow occurs in an n -bit register R after an arithmetic shift-left if **initially**, before the shift operation, the sign bit R_{n-1} is different from its precedent bit R_{n-2}

$$OVL = R_7 \oplus R_6 = 1 \oplus 0 = 1$$

Question 4 (30 points)

A 3-bit arithmetic circuit takes three control bits, x , y and z , and two 3-bit data inputs, A and B . The operations supported by the arithmetic unit are described in the following table.

Draw a detailed logic diagram of the circuit using 1-bit full adders and the digital components of your choice (encoders, decoders, multiplexers, etc.) (Note: X' is the 1's complement of X)

$x y$	$z = 0$	$z = 1$
0 0	$F = A + B$ (add)	$F = A + B + 1$
0 1	$F = A + B'$	$F = A - B$ (subtract)
1 0	$F = A$ (transfer)	$F = A + 1$ (increment)
1 1	$F = A - 1$ (decrement)	$F = A' + 1$ (2's complement)

$x y$	$z = 0$			$z = 1$		
0 0	$A_2 A_1 A_0 +$	$B_2 B_1 B_0 +$	0	$A_2 A_1 A_0 +$	$B_2 B_1 B_0 +$	1
0 1	$A_2 A_1 A_0 +$	$B_2' B_1' B_0' +$	0	$A_2 A_1 A_0 +$	$B_2' B_1' B_0' +$	1
1 0	$A_2 A_1 A_0 +$	0 0 0 +	0	$A_2 A_1 A_0 +$	0 0 0 +	1
1 1	$A_2 A_1 A_0 +$	1 1 1 +	0	$A_2' A_1' A_0' +$	0 0 0 +	1

NOTE: the MUX inputs might be numbered in a weird order below!!!

