Lab #1: Logic Gates

ITI 100 A - Digital Systems

Fall 2015

School of Electrical Engineering and Computer Science
University of Ottawa

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Group #: 14

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Objectives:

- Construct simple combinational logic circuits from a schematic.
- Experimentally determine the functional operation of simple combinational logic circuits.
- Identify common logic functions produced by various circuit configurations by the resulting truth table.
- Connect various gates together to create simple logic functions.
- Analyze combinational logic circuits and predict their operation.
- Construct and test more complex combinational logic circuits.

Equipment and Components:

- QUARTUS II Student Edition Software
- Altera UP-1 circuit board
- AC adapter, minimum output: 9VDC, 250mA
- Anti-static wrist straps
- #22 solid-core wires
- Wire strippers

Circuit Diagrams:

Part I - Combinational Logic Circuits Construction

One Chip Logic Circuit

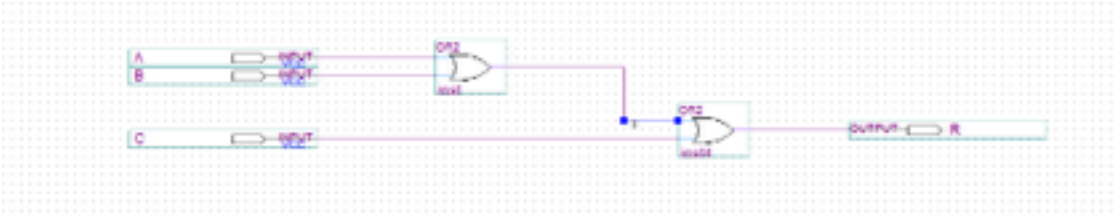

Figure 1: Screenshot of One-chip logic circuit diagram (Figure 6.1.1 of Lab Manual)

Part II - Combinational Logic Circuits Analysis

Exclusive OR circuit

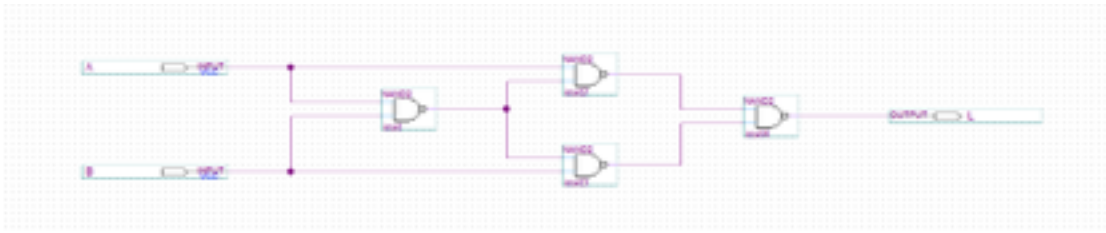

Figure 2: Screenshot of Exclusive OR logic circuit diagram (Figure 6.1.5 of Lab Manual)

Multiple Output Circuit

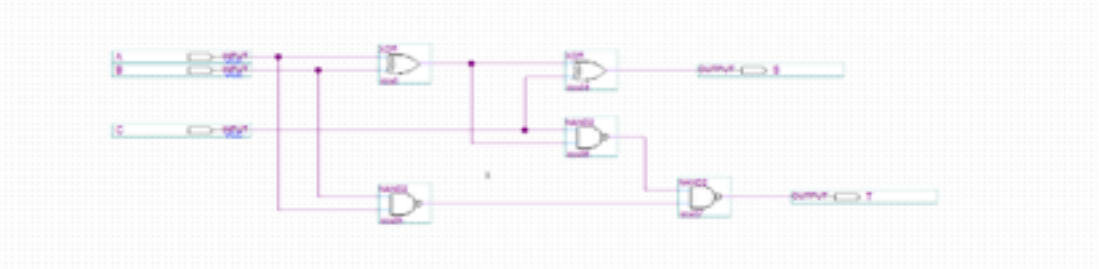

Figure 3: Screenshot of Multiple Output logic circuit diagram (Figure 6.1.8 of Lab Manual)

Experimental Data and Data Processing:

Part I - Combinational Logic Circuits Construction

One Chip Logic Circuit

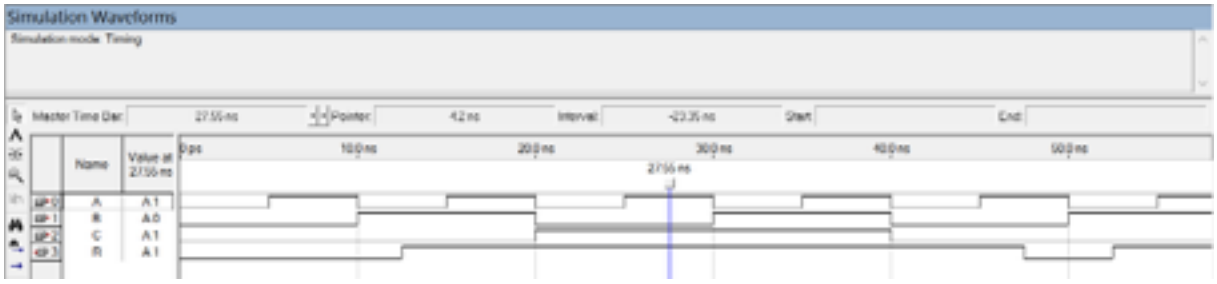

Figure 4: Simulation output waveform of one chip circuit

Table 1: Experimental data observed from MAX 7128 Circuit Board

Input Given From Dip Switches			Observed Output from LEDs
A	**B**	**C**	**OUTPUT R**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Part II - Combinational Logic Circuits Analysis

Exclusive OR circuit

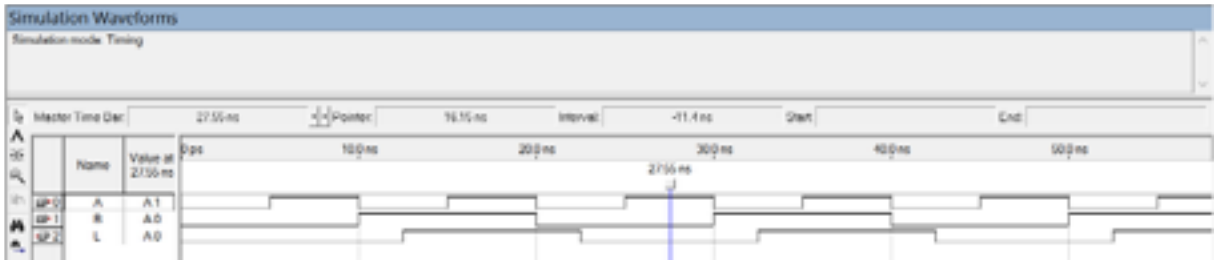

Figure 5: Simulation output waveform of exclusive OR circuit

Table 2: Experimental data observed from MAX 7128 Circuit Board

Input Given From Dip Switches		Observed Output from LEDs
A	**B**	**OUTPUT L**
0	0	0
0	1	1
1	0	1
1	1	0

Multiple Output Circuit

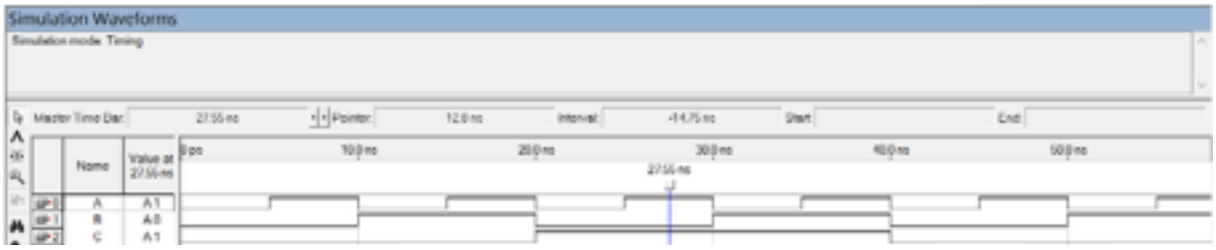

Figure 6: Simulation waveform of multiple output circuit

Table 3: Experimental data observed from MAX 7128 Circuit Board

Input Given From Dip Switches			Observed Output from LEDs	
A	B	C	OUTPUT S	OUTPUT T
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Comparison of Theoretical Data and Experimental Data:

Part I - Combinational Logic Circuits Construction

One Chip Logic Circuit

Table 4: Comparison of Theoretical and Experimental results for one chip logic circuit

Inputs			Expected Results	Actual Results
A	B	C	OUTPUT R	OUTPUT R
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

The results observed experimentally for the one chip circuit from MAX 7128 were identical to results obtained theoretically as expected.

Part II - Combinational Logic Circuits Analysis

Exclusive OR circuit

Table 5: Comparison of Theoretical and Experimental results for exclusive OR circuit

Inputs		Expected Results	Actual Results
A	B	OUTPUT L	OUTPUT L
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	1

The results observed experimentally for the exclusive OR circuit from MAX 7128 differed drastically from results obtained theoretically due to a circuit board malfunction.

Multiple Output Circuit

No results were observed for the multiple output circuit due to time constraints.

Discussion and Conclusions:

- Analysis of the circuit's output for all possible input combinations were made prior to the experiment to predict the theoretical operations of combinational logic circuits Figures 1-3 (6.1.1, 6.1.5, 6.1.8 from lab manual).
- Outputs observed from our circuit board were compared with our predicted theoretical operations (pre-lab truth tables).
- Experimental data for the one chip circuit aligned predictably with our expected data.
- Due to issues in the Quartus II program after running our first project on the circuit, we were asked to switch stations. Our new station was, unfortunately, equipped with a faulty circuit board, thus resulting in inaccurate output results for our exclusive OR circuit (Table 5).
- While we did not have enough time to re-upload our exclusive OR circuit on a different circuit board, we will come to future labs with pre-constructed simulations to avoid wasting time on device malfunctions and to minimize human error in the rushed construction of our simulations and schematic maps.