Question (1)

The range of signed integers N expressed in 2-s complement representation that can be stored in a 10-bit register is:

(a) $-1024 \leq N \leq +1023$ (b) $-1023 \leq N \leq +1024$
(c) $-512 \leq N \leq +511$ (d) $-511 \leq N \leq +512$
(e) None of the above

SOLUTION

1-bit for the Sign and 9 bits represents the number, so
$-2^9 \leq N \leq 2^9-1$

(c) $-512 \leq N \leq +511$

Question (2)

Identify the decimal number which is represented next in floating point with the IEEE 754 standard:

11000010100010101100000000000000

(a) (- 133.375)10 (b) (- 69.375)10
(c) (- 138.750)10 (d) (- 34.6875)10
(e) (- 8.671875)10

SOLUTION

1	10000101	00010101100000000000000
S	E	M

Question (2) (Cont.)

SOLUTION

1	10000101	00010101100000000000000
S	E	M

✓ Find "real" exponent, n

$n = E - 127$

$= 10000101_2 - 127 = 133 - 127 = 6$

✓ Put S, M, and n together to form binary result
(Don't forget the implied "1." on the left of the mantissa.)

$-1.000101011_2 \times 2^6 = (-1000101.011)_2$

-69

$2^{-2} = 0.25$

$2^{-3} = 0.125$

0.375

(b) $(-\ 69.375)_{10}$

Question (3)

Give the best binary approximation of $A = (26.6)_{10}$ and $B = -\ (23.4)_{10}$ employing signed 2's-complement representation with 2 bits for the fractional part.

SOLUTION

$A = (26.6)_{10} \approx +(11010.10)_2 = (011010.10)_2 = (26.5)_{10}$

$B = -\ (23.4)_{10} = -(010111.10)_2 = -b$ with $b = +23.5$ (closest to 23.4)

Let's assume that we don't know how to find the 2's-complement of a fractional negative number, so we'll consider

- $b = (010111.10)_2 = (010111.10)_2 \times 2^2/2^2 = (01011110)_2/2^2$
- First we'll find the 2's-complement of $(01011110)_2 = (10100010)_2$
- then we'll divide it by 2^2 to scale back, such that

=> 2's-complement of $(010111.10)_2 = (10100010)_2/2^2 = (101000.10)_2$

Question (4)

Two 6-bit register contain two numbers X = 01010 and Y = 10101 (expressed in 2's complement representation). Calculate the sum (S = X+Y) and the difference (D=X-Y) of these numbers using additions and 2's complementation only. Since both S and D have to be represented with 6 bits, indicate if overflow occurs, and explain how a circuit can detect these situations. <u>Convert in decimal and write each intermediate and final result</u>, to check the correctness of your assertions.

<u>SOLUTION</u>

Since both <u>X AND Y ARE ALREADY IN 2'S COMPLEMENT REPRESENTATION</u>, their value is

$X = (01010)_2 = +10_{10}$ and

$Y = (10101)_2 = -$ 2's complement of $(0101)_2 = -(1011)_2 = -11_{10}$

$=> -11_{10} = -(+11)_{10}$ represented with 6 bits is: $-(001011)_2$ = 2's complement$(001011)_2 = (110101)_2$

As $-Y$ is needed too: $-Y$ = 2's complement of$(110101)_2 = (001011)_2 =$ (just for verification) $= +11_{10}$

S = X+Y — 2's complement representation — Base 10 representation

CY:		0	0	0	0	0	0	
X +	0	0	1	0	1	0		+10
Y	1	1	0	1	0	1		-11
S	1	1	1	1	1	1		-1

D=X-Y — 2's complement representation — Base 10 representation

CY:		0	0	1	0	1	0	
X +	0	0	1	0	1	0		+10
-Y	0	0	1	0	1	1		+11
D	0	1	0	1	0	1		+21

No Overflow

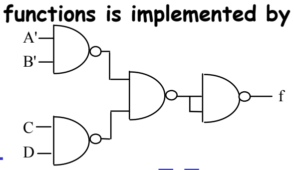
Overflow Detection Expressions

OFL = → if (SgnX=SgnY) ≠SgnC, i.e.,
$(SgnX.SgnY.\overline{SignC} + \overline{SgnX}.\overline{SgnY}.SgnC)$

or → if either of the last two carry bits is 1
$(C_7 . \overline{C_6} + \overline{C_7} . C_6) = C_7 \oplus C_6$

Question (5)

Which of the logic functions is implemented by the following circuit?



<u>SOLUTION</u>

$F = \overline{\overline{\overline{A}.\overline{B}}} . \overline{C.D} = \overline{\overline{A}.\overline{B}} . \overline{C.D} = (A+B).(\overline{C}+\overline{D}) = A.\overline{C}+A.\overline{D}+B.\overline{C}+B.\overline{D}$

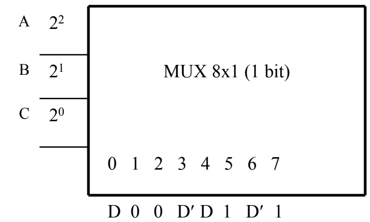
(e) f(A,B,C,D) = Sm(4,5,6,8,9,10,12,13,14)+X(7,11)

AB \ CD	00	01	11	10
00	(0) 0	(1) 0	(3) 0	(2) 0
01	(4) 1	(5) 1	(7) x	(6) 1
11	(12) 1	(13) 1	(15) 0	(14) 1
10	(8) 1	(9) 1	(11) x	(10) 1

C (columns 11, 10); D (columns 01, 11); A (rows 11, 10); B (rows 01, 11)

Question (6)

Which of the following logic functions is implemented by the given circuit?



SOLUTION

(e) f(A,B,C,D) = Sm(1,6,9,10,11,12,14,15)

AB \ CD	00	01	11	10
00	0	1	0	0
01	0	0	0	1
11	1	0	1	1
10	0	1	1	1

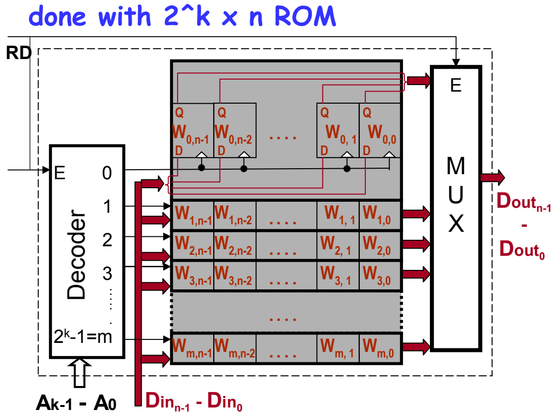
Question (7)

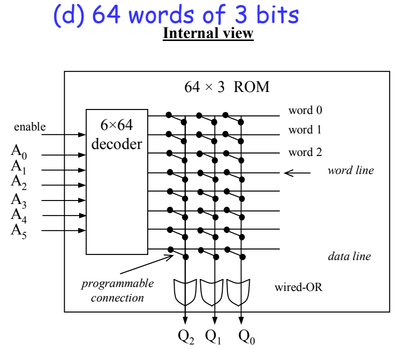
What is the capacity of a ROM, capable to implement three functions of six variables?

SOLUTION

Any combinational circuit of n functions of same k variables can be done with 2^k x n ROM

(d) 64 words of 3 bits



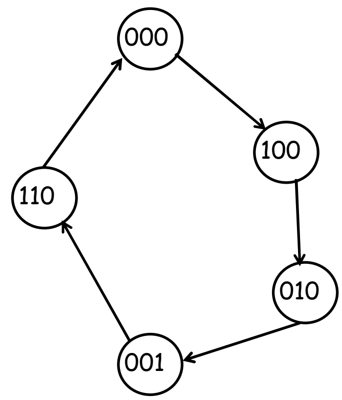


Question (8)

1) - Draw the state diagram of the sequential circuit whose state table is given below

SOLUTION

A B C	$A^+B^+C^+$	JA	KA	JB	KB	JC	KC
0 0 0	1 0 0	1	x	0	x	0	x
0 0 1	1 1 0	1	x	1	x	x	1
0 1 0	0 0 1	0	x	x	1	1	x
1 0 0	0 1 0	x	1	1	x	0	x
1 1 0	0 0 0	x	1	x	1	0	x



Question (8) (Cont.)

1) Indicate the correct set of minimized equations of the JK flip-flops inputs

SOLUTION

(c) $JA = \overline{B}$, $KA = 1$, $JB = A+C$, $KB = 1$, $JC = \overline{A}.B$, $KC = 1$.

A B C	$A^+B^+C^+$	JA	KA	JB	KB	JC	KC
0 0 0	1 0 0	1	x	0	x	0	x
0 0 1	1 1 0	1	x	1	x	x	1
0 1 0	0 0 1	0	x	x	1	1	x
1 0 0	0 1 0	x	1	1	x	0	x
1 1 0	0 0 0	x	1	x	1	0	x

Question (8) (Cont.)

2) If your circuit reaches by mistake any of the 3 states that are not used, determine their corresponding next state.

SOLUTION

(c) $JA = \overline{B}$, $KA = 1$, $JB = A+C$, $KB = 1$, $JC = \overline{A}.B$, $KC = 1$.

A B C	$A^+B^+C^+$
0 1 1	0 0 0
1 0 1	0 1 0
1 1 1	0 0 0

2) Is your circuit auto-corrective?

YES

Question (8) (Cont.)

3) Draw the time diagram and give the states of the flip-flops' outputs through the first 6 clock pulses, assuming that their initial state (at t=0) is 000 and they are triggered on the rising edge of the clock.

SOLUTION