CEG2136 Computer Architecture I
CEG2536 Architecture des ordinateurs I

uOttawa

NAME / ID#

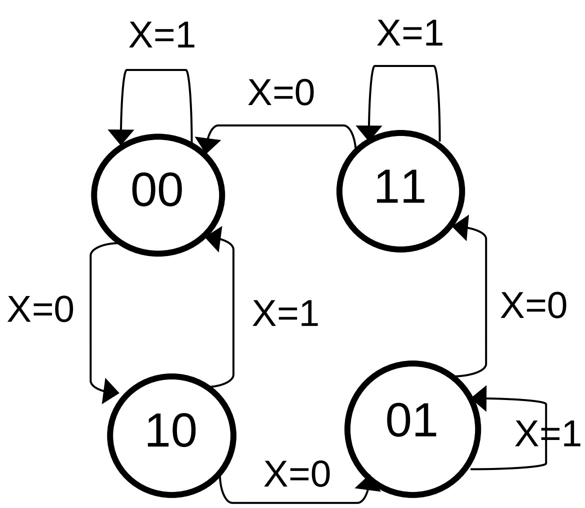
Quiz 1
Fall 2015

Even

P1. The next figure shows the state diagram of a logic circuit which has a unique one-bit external input x.

1. [12 points] Start off by deriving the state table of the circuit. Then, assuming that JK flip-flops are to be used in the implementation, extend the state table with the excitation table of the circuit.
2. [12 points] Find simplified expressions for each flip-flop inputs.

2.



	A^n	B^n	X	A^{n+1}	B^{n+1}	J_A	K_A	J_B	K_B
(0)	0	0	0	1	0	1	x	0	x
(1)	0	0	1	1	1	1	x	1	x
(2)	0	1	0	1	1	1	x	x	0
(3)	0	1	1	0	1	0	x	x	0
(4)	1	0	0	0	1	x	1	1	x
(5)	1	0	1	0	0	x	1	0	x
(6)	1	1	0	0	0	x	1	x	1
(7)	1	1	1	1	1	x	0	x	0

SOLUTION:

Recall:

A) the "copy & paste recipe:"

[1] J = next state if **present state is 0**
[2] J = don't care (x) if ***present state is 1***
[3] K = don't care (x) if **present state is 0**
[4]. K = complement of the next state if present state is 1

… or B) The JK FF Excitation Table, i.e.:

	if $Q^n = 0$	if $Q^n = 1$
J =	[1] Q^{n+1}	[2] x
K =	[3] x	[4] (Q^{n+1})'

J_A

A \ BX	00	01	11	10
0	(0) 1	(1) 1	(3) 0	(2) 1
1	(4) x	(5) x	(7) x	(6) x

$J_A = B' + X'$

K_A

A \ BX	00	01	11	10
00	(0) x	(1) x	(3) x	(2) x
1	(4) 1	(5) 1	(7) 0	(6) 1

$K_A = B' + X'$

J_B

A \ BX	00	01	11	10
0	(0) 0	(1) 1	(3) x	(2) x
1	(4) 1	(5) 0	(7) x	(6) x

J_B = A xor X
$AX' + A'X$

K_B

A \ BX	00	01	11	10
00	(0) x	(1) x	(3) 0	(2) 0
1	(4) x	(5) x	(7) 1	(6) 0

$K_B = AX$

P2. [14 points] A sequential circuit has 3 data inputs DB_2, DB_1 and DB_0 and a control input "*LD*" (load data). The operation of the sequential circuit is described in the functional Table 1. Design the sequential circuit using three T flip-flops.

(P2.1.) Provide the *next state functions* of the T flip-flops $\{Q_i^{n+1},\ i = [0, 1, 2]\}$, either by filling out column Q_i^{n+1} of Table 2, or by writing directly its logic expression $Q_i^{n+1} = \delta(LD, Q_i^n, D_i^n)$

(P2.2.) Find the excitation equations $\{T_i = f(LD, Q_i, D_i),\ i = [0, 1, 2]\}$ of the T flip-flops

(P2.3.) Draw the logic diagram of the circuit that you designed; explain your work.

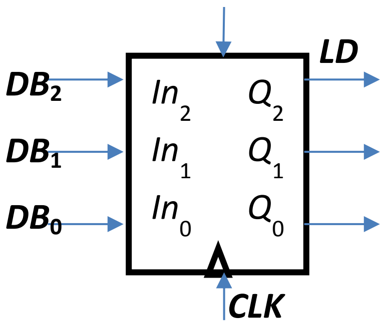


Table 1

LD	Q_i^{n+1} (next state)
0	Q_i^n (present state)
1	DB_i^n (data input)

(P2.1.)

$Q_i^{n+1} = LD'\, Q_i^n, + LD\, D_i^n$

$i = \{0, 1, 2\}$

Table 2.

LD	Q_i^n	DB_i^n	Q_i^{n+1} P2.1	T_i P2.2
0	0	**0**	0	0
0	0	**1**	0	0
0	1	**0**	1	0
0	1	**1**	1	0
1	0	**0**	**0**	0
1	0	**1**	**1**	1
1	1	**0**	**0**	1
1	1	**1**	**1**	0

For **(P2.2)** *Use the T FF's excitation table:*

Q^n	Q^{n+1}	T^n
0	0	0
0	1	1
1	0	1
1	1	0

…

or excitation equation:

$$T = \overline{Q^n} \cdot Q^{n+1} + Q^n \cdot \overline{Q^{n+1}}$$

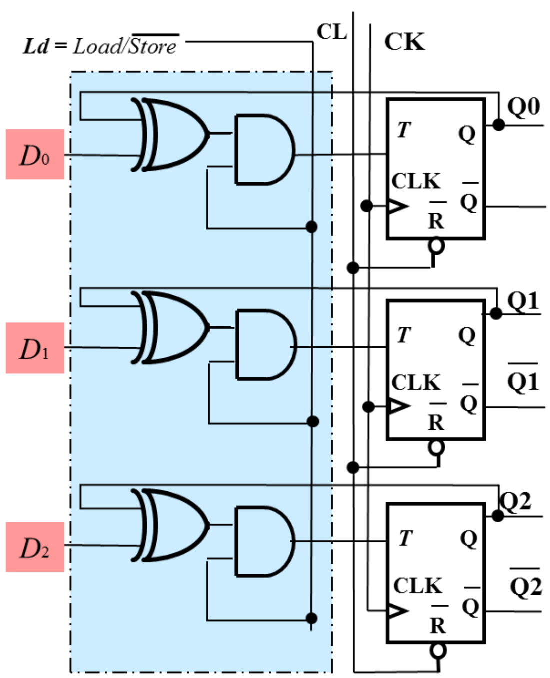
$$T = Q^n \oplus Q^{n+1}$$

Then from Table 2:

$$T_i = LD \cdot \overline{Q_i} \cdot DB_i + LD \cdot Q_i \cdot \overline{DB_i}$$

$$T_i = LD \cdot (Q_i \oplus DB_i), \mathrm{i} = \{0,1,2\}$$

The circuit can be implemented with gates only or using a 2-input multiplexor controlled by LD



OR