4.1

(a) $T_1 = B'C$, $T_2 = A'B$, $T_3 = A + T_1 = A + B'C$,

$T_4 = D \oplus T_2 = D \oplus (A'B) = A'BD' + D(A + B') = A'BD' + AD + B'D$

$F_1 = T_3 + T_4 = A + B'C + A'BD' + AD + B'D$

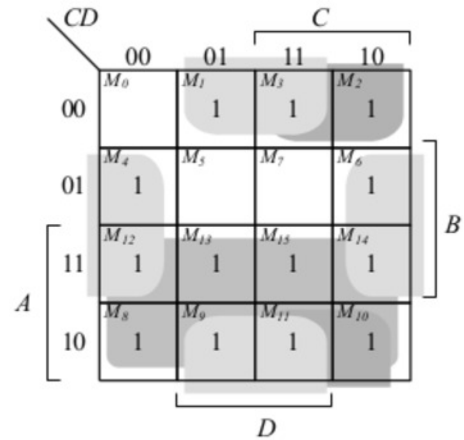
With $A + AD = A$ and $A + A'BD' = A + BD'$:

$F_1 = A + B'C + BD' + B'D$

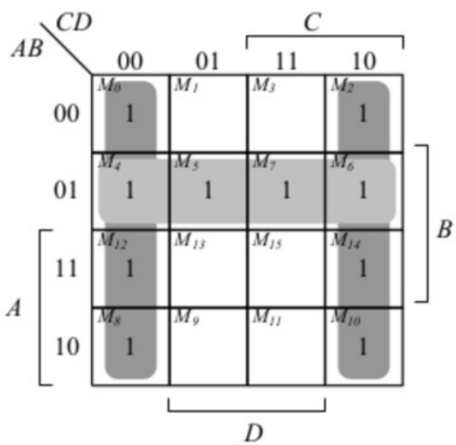
Alternative cover: $F_1 = A + CD' + BD' + B'D$

$F_2 = T_2 + D' = A'B + D'$

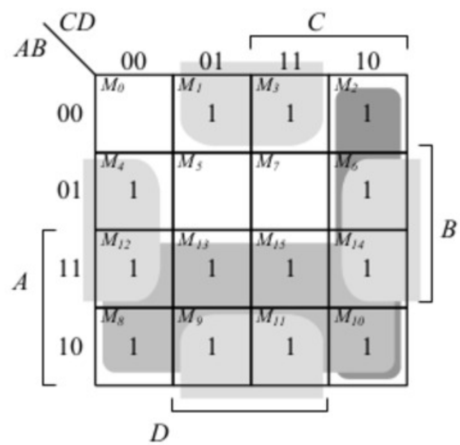
$ABCD$	T_1	T_2	T_3	T_4	F_1	F_2
0000	0	0	0	0	0	1
0001	0	0	0	1	1	0
0010	1	0	1	0	1	1
0011	1	0	1	1	1	0
0100	0	1	0	1	1	1
0101	0	1	0	0	0	1
0110	0	1	0	1	1	1
0111	0	1	0	0	0	1
1000	0	0	1	0	1	1
1001	0	0	1	1	1	0
1010	1	0	1	0	1	1
1011	1	0	1	1	1	0
1100	0	0	1	0	1	1
1101	0	0	1	1	1	0
1110	0	0	1	0	1	1
1111	0	0	1	1	1	0



$F_1 = A + B'C + B'D + BD'$



$F_2 = A'B + D'$



$F_1 = A + CD' + B'D + BD'$

4.5

The Truth table of combinational circuit is as shown in Table below.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

Determine the Boolean expression for the binary output *A*:

Clearly from the Table

$$\begin{aligned}A &= x'yz + xyz' + xyz \\ &= x'yz + xy(z' + z) \\ &= x'yz + xy(1)\end{aligned}$$

$A = y(x'z + x)$ ...... (1)

Apply distributive law to equation (1).

$$\begin{aligned}A &= y(x' + x)(z + x) \\ &= y(1)(z + x)\end{aligned}$$

$A = xy + yz$ ...... (2)

Determine the Boolean expression for the binary output *B*:

Clearly from the Table

$$\begin{aligned}B &= x'y'z + x'yz' + xy'z' + \underline{xy'z} \\ &= x'y'z + x'yz' + xy'z' + xy'z + xy'z \qquad (\text{Since } X + X = X) \\ &= (x' + x)y'z + x'yz' + xy'(z' + z) \\ &= (1)y'z + x'yz' + xy'(1)\end{aligned}$$

$B = xy' + y'z + x'yz'$ ...... (3)

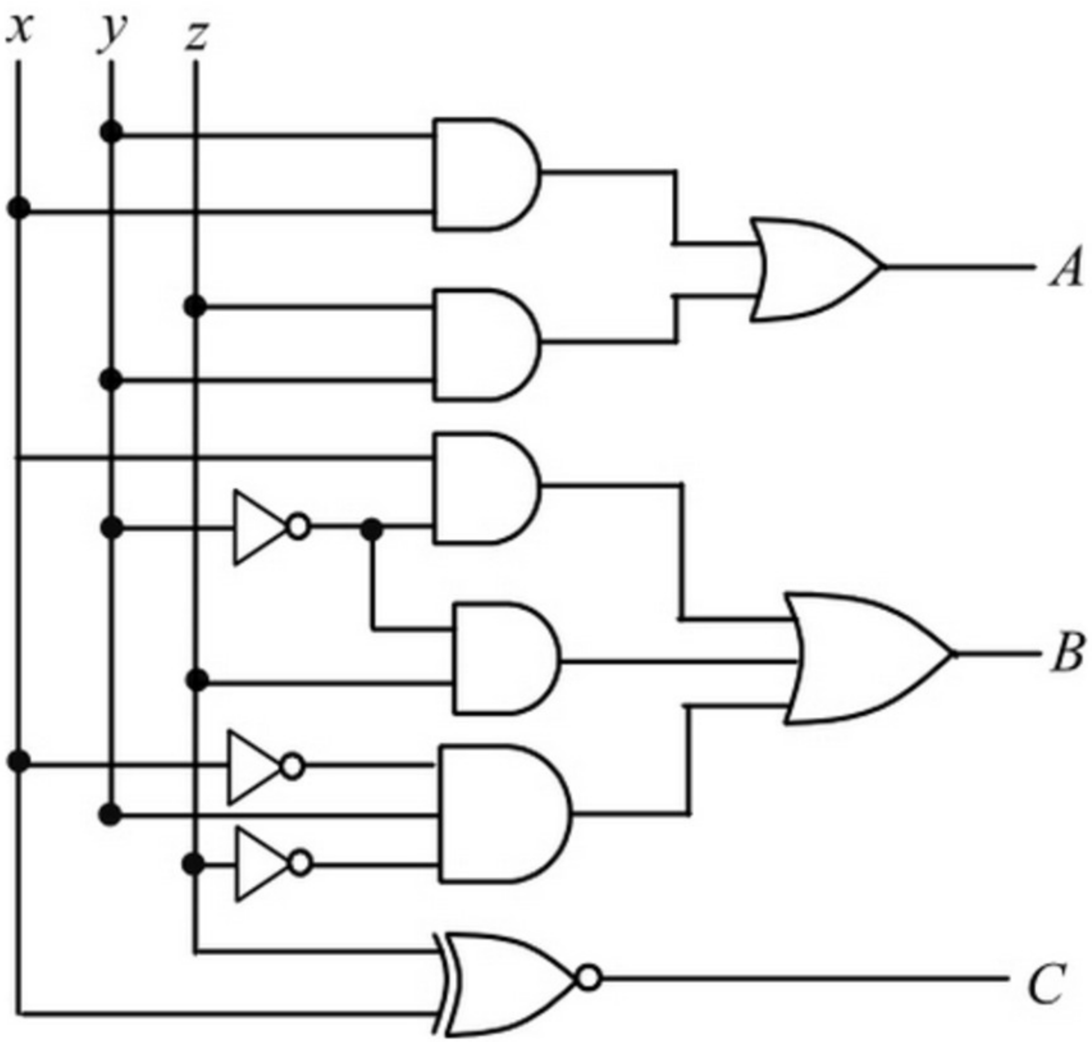
Determine the Boolean expression for the binary output *C*:

Clearly from the Table

$$
\begin{aligned}
C &= x'y'z' + x'yz' + xy'z + xyz \\
&= x'z'(y' + y) + xz(y' + y) \\
&= x'z'(1) + xz(1) \\
&= x'z' + xz
\end{aligned}
$$

$C = (x \oplus z)'$ ...... (4)

Use the Boolean expressions of equations (2), (3) and (4), to design the combinational circuit. The combinational logic circuit is shown below.



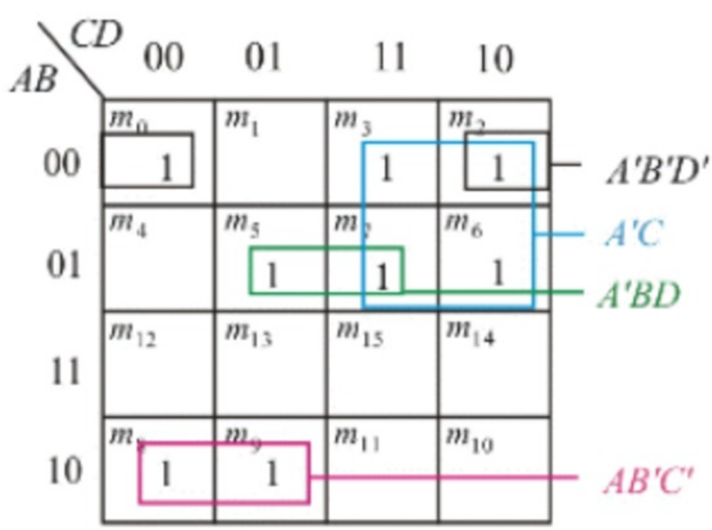
Alternatively, the simplification of expressions can be done using Karnaugh maps

4.9

From the given numerical designation for display draw a table as

ABCD	a	b	c	d	e	f	g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	1	0	1	1

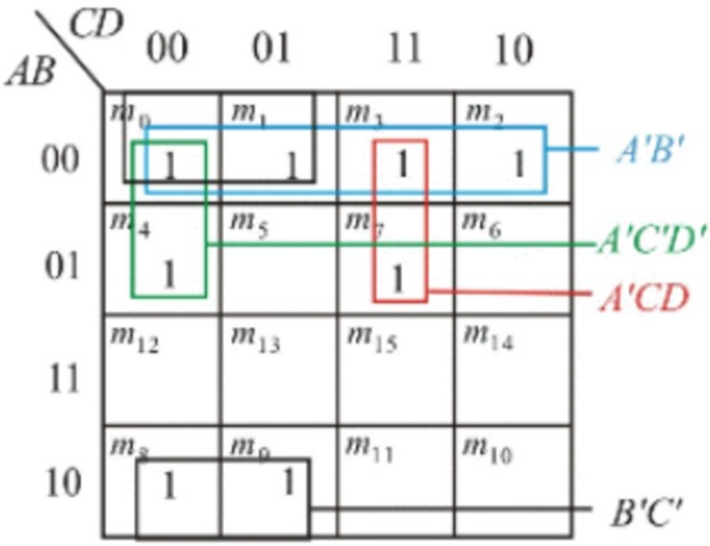
Now draw the K-map for *a* as



Thus, we get

$$\boxed{a = A'C + A'BD + AB'C' + A'B'D'}$$

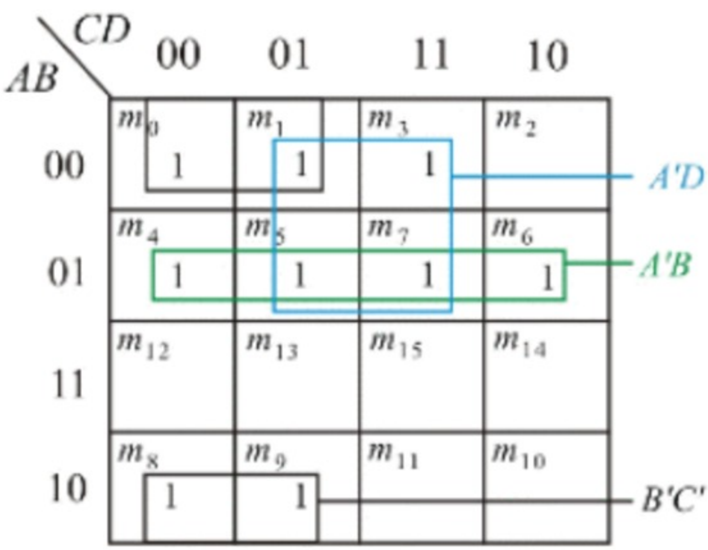
Now draw the K-map for b as



Thus, we get

$$\boxed{b = A'B' + A'CD + B'C' + A'C'D'}$$

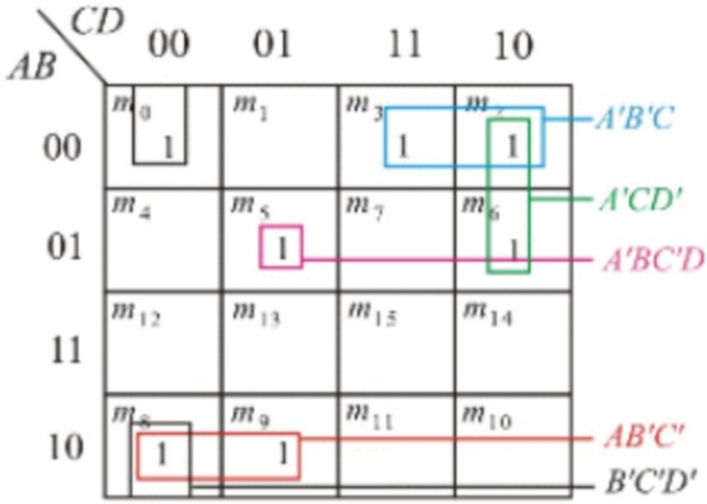
Now draw the K-map for c as



Thus, we get

$$\boxed{c = A'D + A'B + B'C'}$$

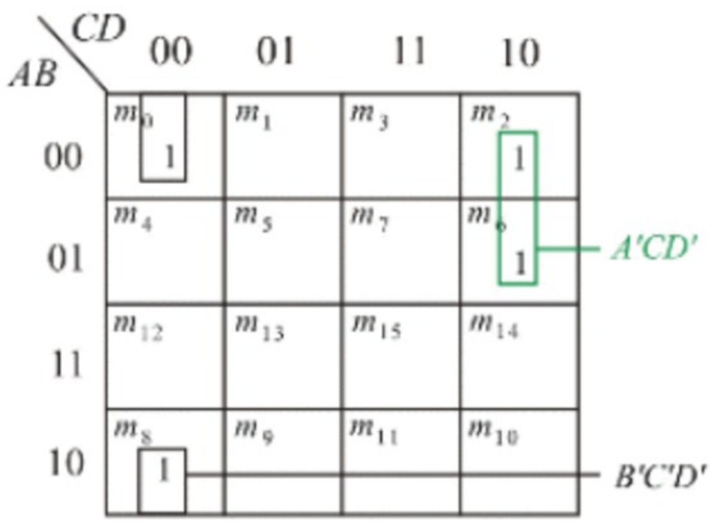
Now draw the K-map for *d*.



Thus, we get

$$\boxed{d = A'BC'D + AB'C' + A'B'C + A'CD' + B'C'D'}$$

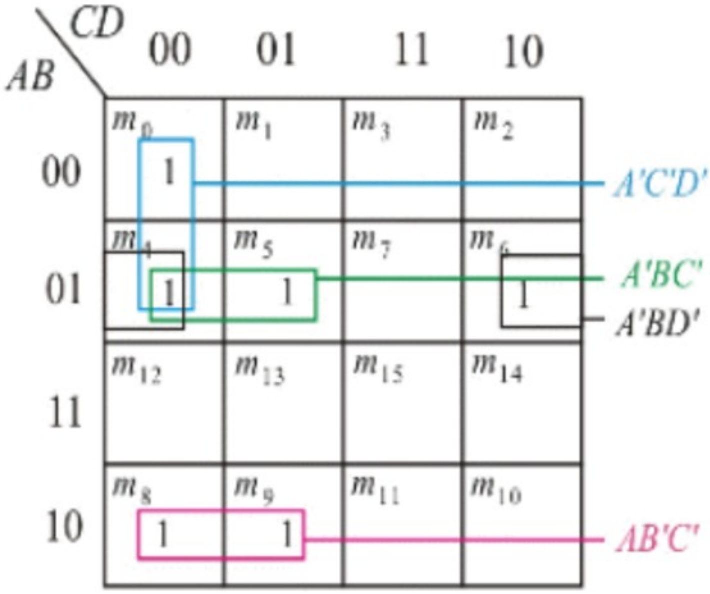
Now draw the K-map for *e* as



Thus, we get

$$\boxed{e = A'CD' + B'C'D'}$$

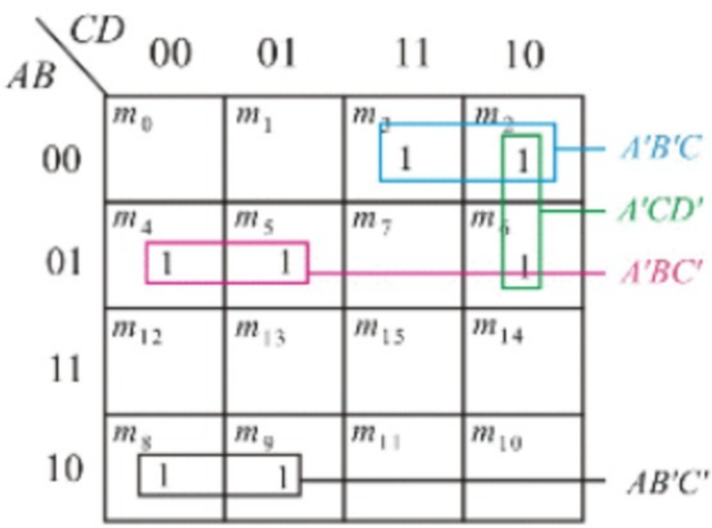
Now draw the K-map for f as



Thus, we get

$\boxed{f = A'BC' + AB'C' + A'BD' + A'C'D'}$

Now draw the K-map for g as



Thus, we get

$\boxed{g = A'BC' + AB'C' + A'B'C + A'CD'}$

4.21

The truth table of exclusive-NOR satisfies the given condition.

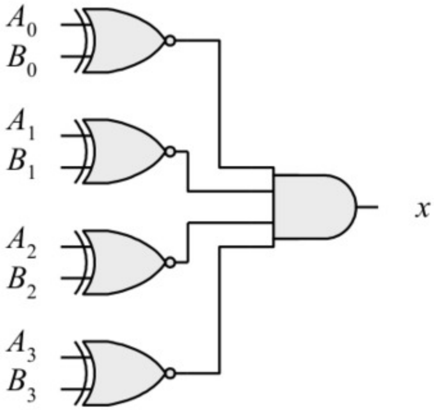
The expression for exclusive-NOR is $x = (A \oplus B)'$

The truth table of exclusive-NOR is shown below.

A	B	x
0	0	1
0	1	0
1	0	0
1	1	1

AND gate output is 1 when all inputs are 1, i.e AND gate output is 1 when all corresponding bits are same (given four bit numbers are equal).
AND gate truth table is:

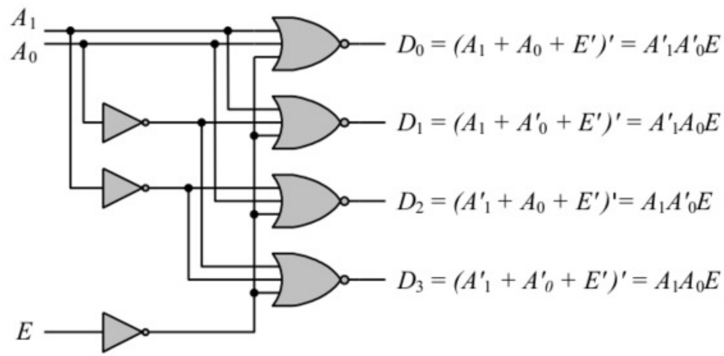
A	B	x
0	0	0
0	1	0
1	0	0
1	1	1

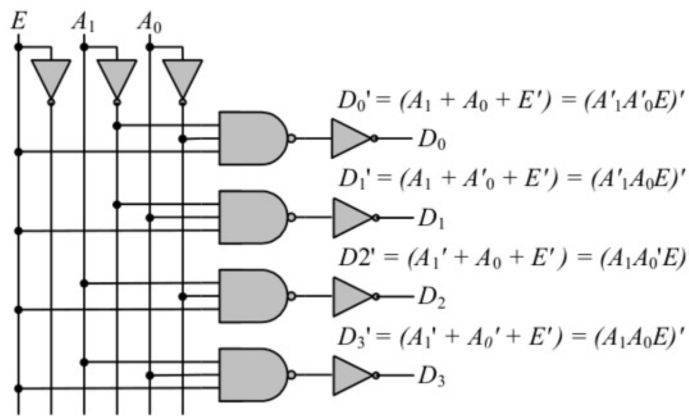


$$x = (A_0 \oplus B_0)'(A_1 \oplus B_1)'(A_2 \oplus B_2)'(A_3 \oplus B_3)'$$

4.23

D0 = A1'A0' = (A1 + A0)' (NOR) D0' = (A1'A0')' (NAND)
D1 = A1'A0 = (A1 + A0')' (NOR) D1' = (A1'A0)' (NAND)
D2 = A1A0' = (A1' + A0)' (NOR) D2' = (A1A0')' (NAND)
D3 = A1A0 = (A1' + A0')' (NOR) D3' = (A1A0)' (NAND)

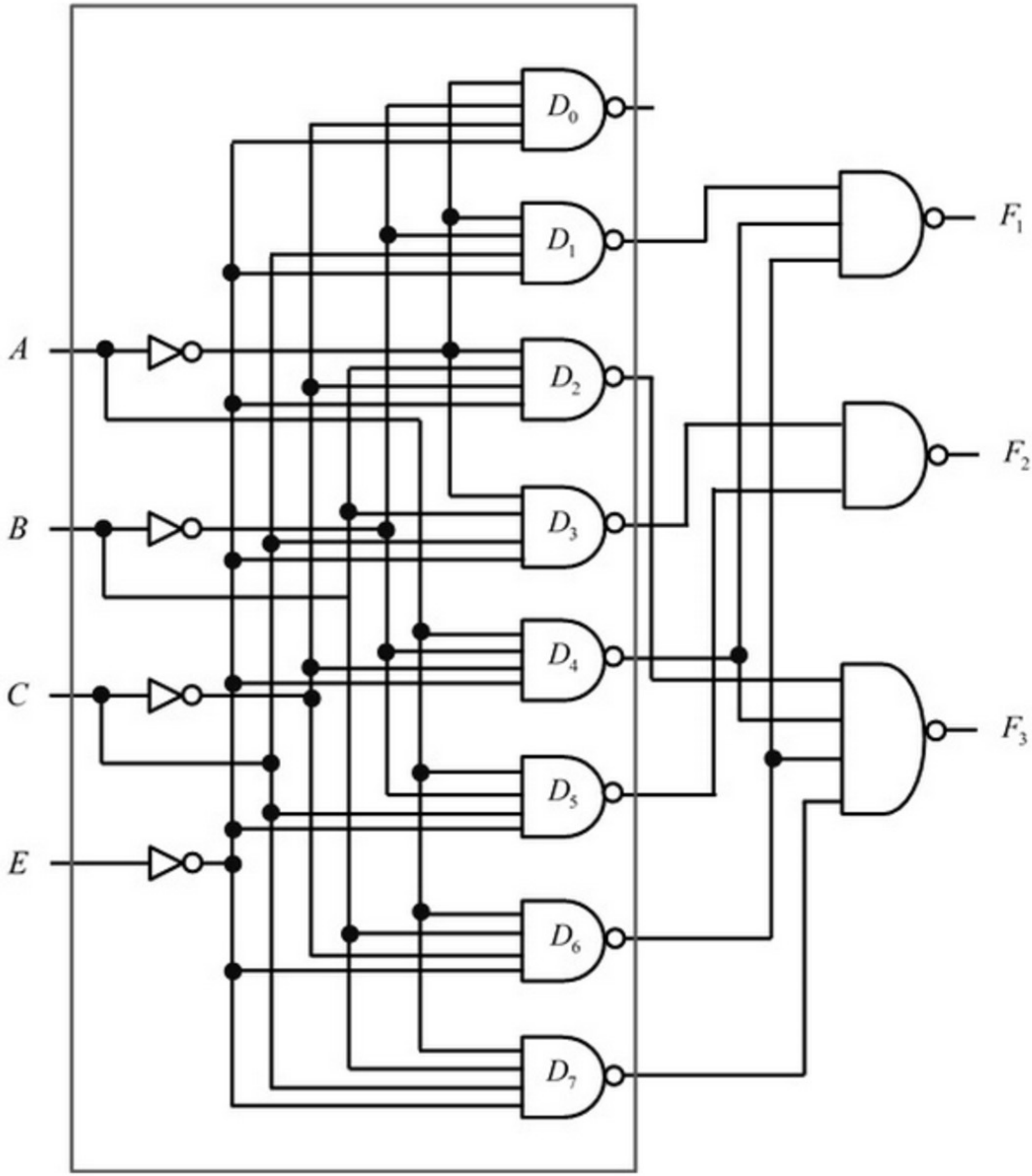




4.27

The implemented decoder circuit constructed with NAND gates is shown below

3 x 8 Decoder



4.28

a)

The Boolean functions that defines the combinational circuit are,

$$F_1(x,y,z) = x'yz' + xz$$

$$F_2(x,y,z) = xy'z' + x'y$$

$$F_3(x,y,z) = x'y'z' + xy$$

Express the Boolean function F_1 in terms of sum of min terms.

$$\begin{aligned} F_1(x,y,z) &= x'yz' + xz \\ &= x'yz' + xz(y+y') \\ &= x'yz' + xy'z + xyz \\ &= m_2 + m_5 + m_7 \end{aligned}$$

$F_1(x,y,z) = \sum(2,\ 5,\ 7)$ …… (1)

Express the Boolean function F_2 in terms of sum of min terms.

$$\begin{aligned} F_2(x,y,z) &= xy'z' + x'y \\ &= xy'z' + x'y(z+z') \\ &= xy'z' + x'yz' + x'yz \\ &= m_4 + m_2 + m_3 \end{aligned}$$

$F_2(x,y,z) = \sum(2,\ 3,\ 4)$ …… (2)

Express the Boolean function F_3 in terms of sum of min terms.

$$\begin{aligned} F_3(x,y,z) &= x'y'z' + xy \\ &= x'y'z' + xy(z+z') \\ &= x'y'z' + xyz' + xyz \\ &= m_0 + m_6 + m_7 \end{aligned}$$

$F_3(x,y,z) = \sum(0,\ 6,\ 7)$ …… (3)

4.28 (b)

The Boolean functions that defines the combinational circuit are,

$$F_1(x,y,z)=(y'+x)z$$

$$F_2(x,y,z)=y'z'+x'y+yz'$$

$$F_3(x,y,z)=(x+y)z$$

Express the Boolean function F_1 in terms of sum of min terms.

$$\begin{aligned}F_1(x,y,z)&=(y'+x)z\\&=y'z+xz\\&=(x+x')y'z+x(y+y')z\\&=xy'z+x'y'z+xyz+xy'z\\&=m_5+m_1+m_7+m_5\end{aligned}$$

The Boolean function F_1 in terms of sum of min terms is,

$$F_1(x,y,z)=\sum(1,\ 5,\ 7)$$ ...... (4)

Express the Boolean function F_2 in terms of sum of min terms.

$$\begin{aligned}F_2(x,y,z)&=y'z'+x'y+yz'\\&=(x+x')y'z'+x'y(z+z')+(x+x')yz'\\&=xy'z'+x'y'z'+x'yz+x'yz'+xyz'+x'yz'\\&=m_4+m_0+m_3+m_2+m_3+m_2\end{aligned}$$

$$F_2(x,y,z)=\sum(0,\ 2,\ 3,\ 4,\ 6)$$ ...... (5)

Express the Boolean function F_2 in terms of sum of min terms.

$$\begin{aligned}F_3(x,y,z)&=(x+y)z\\&=xz+yz\\&=x(y+y')z+(x+x')yz\\&=xyz+xy'z+xyz+x'yz\\&=m_7+m_5+m_7+m_3\end{aligned}$$

$$F_3(x,y,z)=\sum(3,\ 5,\ 7)$$ ...... (6)

4.33

$$S(x, y, z) = \Sigma(1, 2, 4, 7)$$
$$C(x, y, z) = \Sigma(3, 5, 6, 7)$$

S	I_0	I_1	I_2	I_3
x'	0	1	2	3
x	4	5	6	7
	x	x'	x'	x

C	I_0	I_1	I_2	I_3
x'	0	1	2	3
x	4	5	6	7
	0	x'	x'	1