

CPSC 359 – Spring 2015
Assignment 1 – Digital Logic
Time Division Multiplexing
Due May 29th @11:59 PM

Objective: In this assignment, you will design a circuit applying Time Division Multiplexing (TDM) on a Wireline.

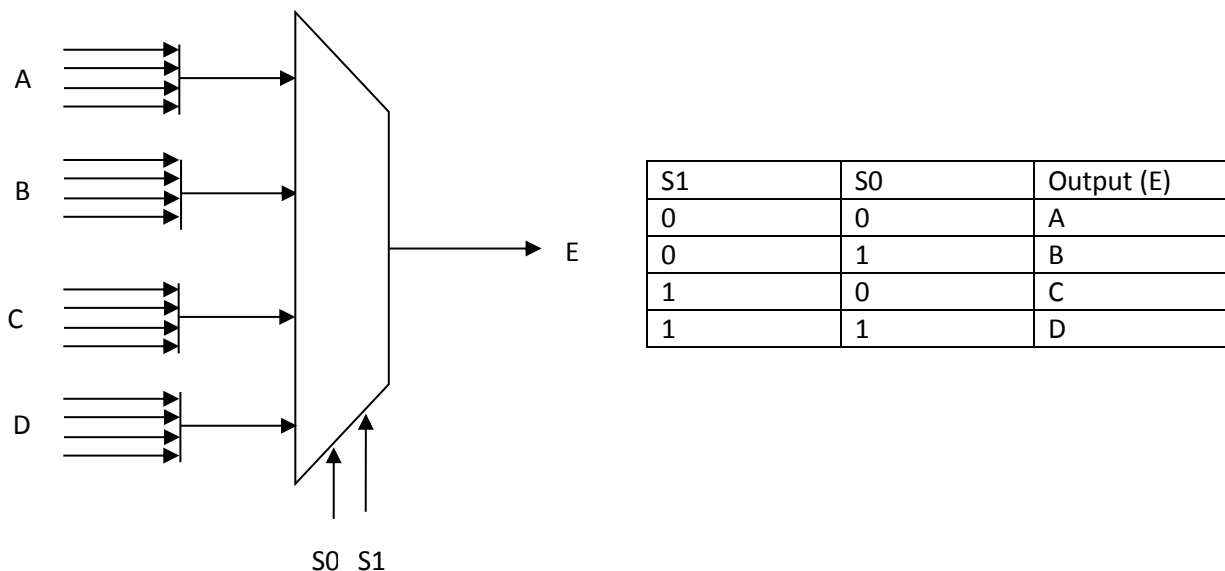
Background: TDM is a type of multiplexing that allows multiple users share a common medium (such as a telephone line) in order to transmit data to multiple destinations on the same medium. TDM is widely used in fields such as telecommunications, especially digital telephony.

The main components of TDM are a Multiplexer (MUX) & a De-multiplexer (DMX). As discussed in the lectures, one of the input lines in a multiplexer can be selected (via selector lines) to be forwarded to the single output line. In a DMX, the single input line is forwarded (via a selector) to one of the output lines. In TDM, the transmitter uses a MUX and the receiver uses a DMX. Multiplexing and de-multiplexing need to be synchronized properly.

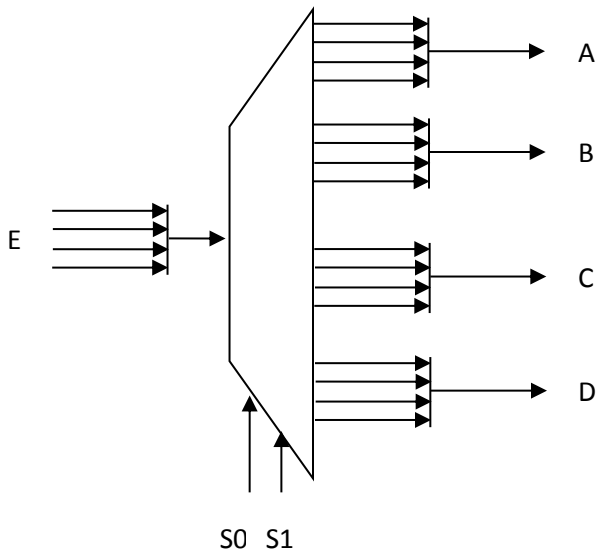
In this assignment you will design a 4-channel (4-user) digital telephony line of 4 bits.

Components:

- **4-bit, 4-1 multiplexer** : A multiplexer having 4 inputs and one output, input and output lines are 4 bits each:



- **4-bit, 1-4 De-Multiplexer (DMX):** This is a de-multiplexer having one input and 4 output lines of 4 bits each:

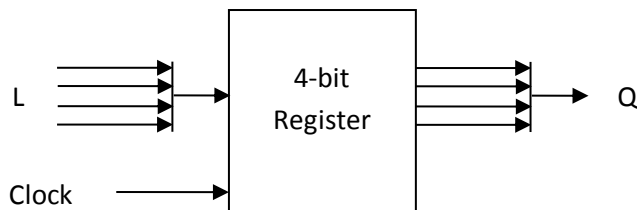


S1	S0	A	B	C	D
0	0	E	0	0	0
0	1	0	E	0	0
1	0	0	0	E	0
1	1	0	0	0	E

- **2-bit counter:** Counts from 0 - 3 adding one at a rising edge of a clock, reset at overflow:

Time	O1	O2
1	0	0
2	0	1
3	1	0
4	1	1
5	0	0

- **4-bit register:** Stores 4-bits of data input on the rising edge of a clock.

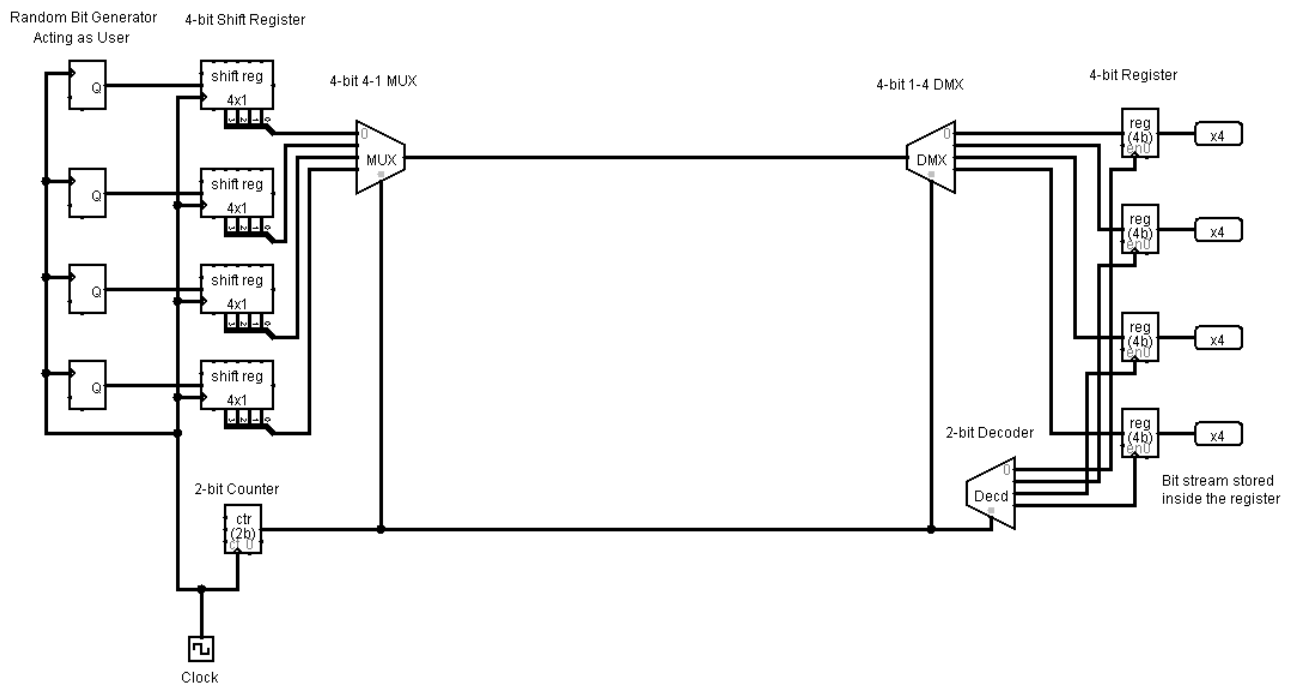


- **4-bit shift register and a 2-bit Decoder.**

At the transmitter side: a random sequence of bits is generated 1-bit at a time, the **4-bit shift register** will act as an input buffer; every 4 cycles of the clock the value stored in the **4-bit shift register** will be transmitted by the **multiplexer** to the receiver side. This means that at every rising edge of the clock, one of the multiplexed lines will be available for transmission to the other side.

At the receiver side: the **de-multiplexer** receives the 4 bits transmitted by the **multiplexer**, forward the received 4 bits to one of the 4 output lines according to what channel is the **multiplexer** sending and the value will be saved in a **4-bit register** connected to the corresponding output line at every rising edge of the clock. The **2-bit decoder** will act as a clock input which has one high tick every 4 ticks for a selected **4-bit register**. One **2-bit counter** will act as the selector line for **MUX, DMX & 2-bit decoder** for synchronization.

Note: Using the available components in Logisim is not permitted except for wiring, gates, shift registers, and the random bit generator.



Deliverables:

1. Design and implement the corresponding circuit in Logisim.
2. Use building blocks to create the corresponding components.
3. MUX, DMX & Register data & output line should be bundled to a single 4-bit line inside the block of the circuit (use splitters).

Marking Guide:

4-bit Multiplexer	4 points
4-bit De-multiplexer	4
2-bit counter	2
4-bit register	2
Using building blocks	3
Labeling	2
Overall circuit function	3
Total	20

Teams: You are advised to work with another student in class in order to complete the assignment, but you are not required to do so. Peer evaluation in teams may be conducted.

Submission: Submit your .circuit file to the dropbox on D2L.

Late Submission Policy: Late submissions will be penalized as follows:

-12.5% for each late day or portion of a day for the first two days

-25% for each additional day or portion of a day after the first two days

Hence, no submissions will be accepted after 5 days (including weekend days) of the announced deadline

Academic Misconduct: Any similarities between assignments will be further investigated for academic misconduct. While you are encouraged to discuss the assignment with your colleagues, your final submission must be your own original work.