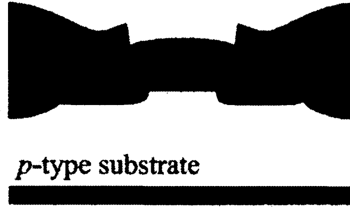
Student #:______________________

1. The cross section of a simple substrate MOSFET structure is illustrated below.



a) How many patterning steps are required to make the structure above?

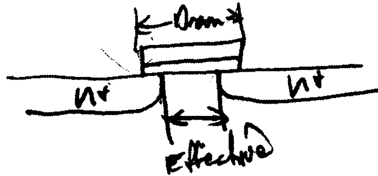
1 - field oxide (or well)
2 - poly gate
3 - contact cut
4 - metal pattern
} 4 total

b) How many additional steps would be needed if we wanted to fabricate a *p*-channel device on a *p*-type substrate?

We would need to implant/diffuse an n-well but the field oxide can be used to define this so no additional patterning is req'd.

c) What is the difference between "drawn channel length" and "effective channel length"?

Drawn channel = width of gate poly (as 'drawn')
Effective channel = width of gate poly − source + drain diffusion under gate



d) Why is the gate oxide grown using "dry" oxidation rather than "wet" oxidation?

A high quality oxide is required for the gate oxide. It must be very thin, uniform and dense.

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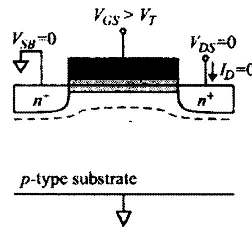
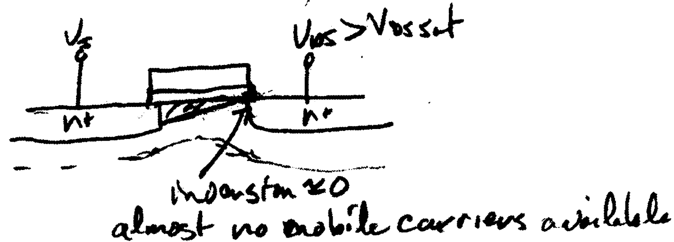
2. The cross section of a simple substrate n-channel MOSFET biased above threshold is illustrated below.



a) What is meant by "inversion" in a MOSFET and how does it form a conductive channel?

Inversion occurs when carriers are drawn to the region under the gate by the applied transverse field until the density of minority carriers dominates the behaviour. This forms a channel because there is no longer a junction at the source and drain and sufficient mobile carriers are available.

b) Redraw the diagram above illustrating how the channel region is changed at pinch-off, when $V_{DS} > V_{DSsat}$?



c) A gate bias is applied that causes the MOSFET channel to have a uniform induced carrier density of $n = 5 \times 10^{17}$ cm^{-3} and thickness of 0.2 µm. For an effective channel length of 2 µm and width of 10 µm, what is the channel current, I_D, for $V_{DS} = 1.5$V ?

$$\sigma = q n \bar{\mu}_n$$
$$= 1.602 \times 10^{-19} \cdot 5 \times 10^{17} \cdot 520$$
$$= 41.65 \text{ S/cm}$$

$$\mathcal{E} = \frac{V_{DS}}{L_{eff}} = \frac{1.5}{2 \times 10^{-4}} = 7.5 \times 10^3 \text{ V/cm}$$

$$J = \sigma \mathcal{E} = 41.65 \times 7.5 \times 10^3 = 3.12 \times 10^5 \text{ A/cm}^2$$

$$I = AJ = 0.2 \times 10^{-4} \cdot 10^{-3} \cdot 3.12 \times 10^5 = 6.25 \times 10^{-3} \text{ A} = 6.25 \text{ mA}$$

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3. There are three voltage components in the equation used to calculate the threshold voltage, V_T, for MOSFET.

$$V_T = V_{FB} + 2\phi_B - \frac{\hat{Q}_{dep}}{\hat{C}_{ox}}$$

(a) Briefly describe where each component comes from.

V_{FB} - voltage needed to compensate for the band bending in the silicon caused by the difference in work function between the gate & the silicon.

$2\phi_B$ - Twice the separation of E_i and E_F. This makes the induced carrier density under the gate the same magnitude but opposite sign to the substrate doping

$-\frac{\hat{Q}_{dep}}{\hat{C}_{ox}}$ - The potential drop across the gate oxide.

(b) If the work function for intrinsic silicon ($E_F = E_i = E_g/2$) is $\Phi_{S0} = 3.51\,\text{eV}$, what is the work function if $N_A = 10^{17}/\text{cm}^3$? ($T = 300$ K).

$$E_F - E_V = kT \ln\left(\frac{N_V}{N_A}\right)$$
$$= kT \ln\left(\frac{1.08 \times 10^{19}}{10^{17}}\right) = 0.1213\,V$$

$$\therefore \Phi_S = \Phi_{S0} + \frac{E_g}{2} - 0.1213 = 3.51 + 0.54 - 0.1213 = 3.929$$

(c) Aluminum has a work function of $\Phi_{Al} = 4.1\,\text{eV}$. If we made a silicon MOSFET using aluminum as the gate material and $N_A = 10^{17}/\text{cm}^3$ as in (b), what voltage would need to be applied to the gate to achieve the flat band condition, V_{FB}?

$$V_{FB} = \frac{\Phi_m - \Phi_S}{q} = \frac{4.1 - 3.929}{q} = 0.171\,V$$

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4. (a) What do we mean by drift conduction?

Drift conduction is caused by the motion of carriers under the influence of an electric field.

(b) In the MOSFET square law model what is the assumption made about the depletion charge under the gate?

In the MOSFET square law model the depletion charge under the gate is assumed not to change going from the source to the drain. It is assumed to be fixed at the source value

(c) If a silicon MOSFET has a substrate doping of $N_A = 2 \times 10^{16}$ cm^{-3}, oxide thickness of t_{ox} = 20 nm, a flat band voltage of V_{FB} = -0.8 V and a source to bulk voltage of V_{SB} = 2 V, what is the threshold voltage, V_T? (T = 300K)

$$\hat{C}_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \cdot 8.854 \times 10^{-14}}{20 \times 10^{-7}} = 1.727 \times 10^{-7} \text{ F/cm}^2$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{\hat{C}_{ox}} = \frac{\sqrt{2 \cdot 1.602 \times 10^{-19} \cdot 11.7 \times 8.854 \times 10^{-14} \cdot 2 \times 10^{16}}}{1.727 \times 10^{-7}} = 0.4718 \text{ V}^{1/2}$$

$$V_{T0} = V_{FB} + 2\phi_B + \frac{\sqrt{2q\varepsilon_{si}N_A(2\phi_B)}}{C_{ox}} \; ; \; \phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 0.0259\ln\left(\frac{2 \times 10^{16}}{1.45 \times 10^{10}}\right) = 0.366$$

$$= -0.8 + 2(0.366) + 0.4718 \cdot \sqrt{2 \cdot 0.366}$$

$$= -0.8 + 0.732 + 0.404$$

$$= 0.336 \text{ V}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right)$$

$$= 0.336 + 0.4718\left(\sqrt{0.732 + 2} - \sqrt{0.732}\right)$$

$$= 0.712 \text{ V}$$

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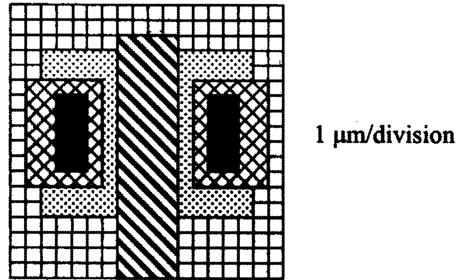
5. A MOSFET has a layout as illustrated in the diagram below.



1 μm/division

(a) If the lateral diffusion under the gate is 0.25 μm and the oxide thickness is t_{ox} = 30 nm what is total gate capacitance, C_{ox} (NOT per unit area)?

The as-drawn gate is 4μm × 11μm so $L = 4 - 2(0.25) = 3.5\mu m$ $W = 11\mu m$

$$\Rightarrow C_{ox} = \frac{\varepsilon_{ox} W \cdot L}{t_{ox}}$$

$$= \frac{3.9 \cdot 8.854\times10^{-14} \cdot 11\times10^{-4} \cdot 3.5\times10^{-4}}{30\times10^{-7}}$$

$$= 4.4\times10^{-14} F$$

$$= 44 fF$$

(b) Using the same values for lateral diffusion under the gate of 0.25 μm and the oxide thickness of t_{ox} = 30 nm, if $N_A = 3\times10^{16}$ cm^{-3} what is the drain current I_D, for V_{SB} = 1V, V_{GS} = 2V and V_{DB} = 4V, V_T = 1V ? (Assume no channel shortening.)

There is no channel shortening so $\lambda = 0$

$V_{DS} = V_{DB} - V_{SB} = 3V$, $V_{DS,sat} = V_{GS} - V_T = 2 - 1 = 1$ ∴ in saturated mode

$$\hat{C}_{ox} = \frac{3.9 \cdot 8.854\times10^{-14}}{30\times10^{-7}} = 1.151\times10^{-7} F/cm^2$$

$$I_D = \mu_n \hat{C}_{ox} \frac{W}{L}\left(\frac{(V_{GS}-V_T)^2}{2}\right)$$

$$= 520 \cdot 1.151\times10^{-7} \cdot \frac{11}{3.5} \cdot \frac{(2-1)^2}{2}$$

$$= 0.94\times10^{-4} A.$$

$$= 94 \mu A$$

Student #:______________________

6. (a) What is the cause of channel shortening in a MOSFET?

Channel shortening in a MOSFET is caused by the formation of a high field region near the drain which reduces the effective length of the inversion layer.

(b) A MOSFET is biased to operate with a transconductance of $g_m = 10$ mS in the absence of channel shortening effects. What would the g_m be if the channel shortening parameter was $\lambda = 0.02\ V^{-1}$?

$$g_m\big|_{\lambda=0} = 10\,mS = \mu_n \hat{C}_{ox} \frac{W}{L}(V_{GS}-V_T)$$

$$g_m\big|_{\lambda=0.02V^{-1}} = \mu_n \hat{C}_{ox} \frac{W}{L}(V_{GS}-V_T)(1+\lambda V_{DS})$$

$$g_m\big|_{\lambda=0.02V^{-1}} = 10^{-2}(1+0.02\,V_{DS})$$

$$= 2\times 10^{-4}\,V_{DS} + 10^{-2}$$

$$= 10.60\,mS \quad \text{for } V_{DS}=3V.$$

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7. (a) We have looked at the MOSFET small signal parameters g_m and g_0 for saturated mode. Derive what the expressions for these parameters would be for a MOSFET in <u>triode</u> mode.

For triode mode $I_D = \mu_n \hat{C}_{ox} \frac{W}{L}\left((V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right)(1+\lambda V_{DS})$

$$g_m = \frac{dI_D}{dV_{GS}}\Big|_{V_{DS}} = \mu_n \hat{C}_{ox}\frac{W}{L} V_{DS}(1+\lambda V_{DS})$$

$$g_o = \frac{dI_D}{dV_{DS}}\Big|_{V_{GS}} = \mu_n \hat{C}_{ox}\frac{W}{L}\left[\left((V_{GS}-V_t)-V_{DS}\right)(1+\lambda V_{DS}) + \left((V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right)\lambda\right]$$

$$= \mu_n \hat{C}_{ox}\frac{W}{L}\left[(V_{GS}-V_t) - V_{DS}\left(1-2\lambda(V_{GS}-V_t) + \frac{3V_{DS}}{2}\lambda\right)\right]$$

or $$= \mu_n \hat{C}_{ox}\frac{W}{L}\left[(V_{GS}-V_t)(1+2\lambda V_{DS}) - V_{DS}\left(1+\frac{3V_{DS}}{2}\lambda\right)\right]$$

(b) Why are MOSFETs not generally used as amplifiers in triode mode?

MOSFETs are not normally used in triode mode mainly because the output conductance, g_o, is higher which limits the obtainable gain. The g_m is also smaller reaching it's saturated value at $V_{DS} = V_{GS} - V_T$.

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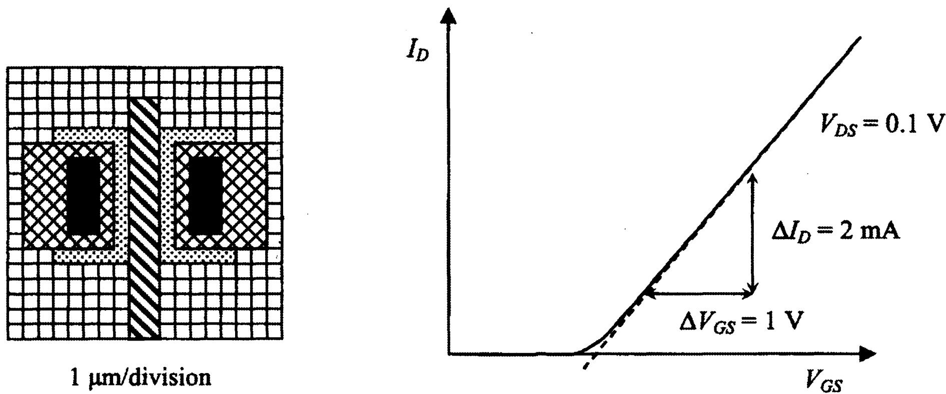
8. The I_D versus V_{GS} curve for a MOSFET with $V_{SB} = 0$ V and small V_{DS} is illustrated below.



(a) If the lateral diffusion under the gate is 0.1 µm and the oxide thickness is 50 nm calculate the effective channel mobility, $\overline{\mu}_n$.

The transistor is biased in triode mode so

$$\left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}} = \overline{\mu}_n \hat{C}_{ox} \frac{W}{L} V_{DS}(1+\lambda V_{DS})$$

$$\approx \overline{\mu}_n \hat{C}_{ox} \frac{W}{L} V_{DS} \quad \text{for } \lambda V_{DS} \ll 1$$

$$= \overline{\mu}_n \cdot \frac{3.9 \times 8.854 \times 10^{-14}}{50 \times 10^{-7}} \cdot \frac{19 \times 10^{-4}}{1.8 \times 10^{-4}} \cdot 0.1$$

$$= \overline{\mu}_n \cdot 3.45 \times 10^{-8}$$

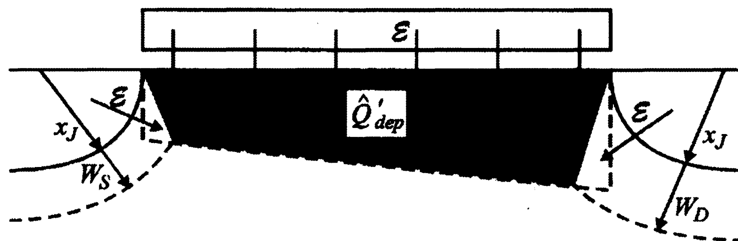
$$\Rightarrow \quad \overline{\mu}_n = \frac{2 \times 10^{-3}}{3.45 \times 10^{-8}} = 5.79 \times 10^{4}\ \text{cm}^2/\text{V-sec}$$

(b) How would you extract the value of the threshold voltage from the curve above?

For small V_{DS} $I_D \approx \overline{\mu}_n \hat{C}_{ox} \frac{W}{L}(V_{GS}-V_T)V_{DS}$ which is linear in $(V_{GS}-V_T)$ so when the extrapolated line intersects the V_{GS} axis at $I_D = 0$, $V_{GS} = V_T$.

Student #:____________________

9. A diagram illustrating the trapezoidal threshold voltage model for a MOSFET is shown below.



(a) What is the cause of the short channel effect on threshold voltage in MOSFETs?

The short channel effect is caused by the source and drain fields controlling some of the charge under the gate reducing the amount directly under control of the gate. This causes V_T to go down as the channel length is reduced.

(b) The substrate above is unbiased ($V_{SB} = 0$ V) and doped at $N_A = 10^{17}$ cm^{-3}. If the contact implants have $x_J = 0.5$ µm and the effective gate length is $L = 1.5$ µm what would the change in threshold voltage, ΔV_T, be if $V_{DS} = 3$ V?

$$\Delta V_T = -\frac{\hat{Q}_{dep}}{C_{ox}} + \frac{\hat{Q}'_{dep}}{C_{ox}} \quad ; \quad \phi_B = 0.0259 \ln\left(\frac{10^{17}}{1.45\times10^{10}}\right) = 0.4078\text{ V}$$

$$= \frac{\sqrt{2q\varepsilon_{Si} N_A (2\phi_B)}}{C_{ox}}\left[1 - \left\{1 - \frac{x_J}{2L}\left(\sqrt{1+\frac{2W_S}{x_J}} + \sqrt{1+\frac{2W_D}{x_J}} - 2\right)\right\}\right]$$

$$= \sqrt{2q\varepsilon_{Si} N_A (2\phi_B)}\,\frac{x_J}{C_{ox}2L}\left(\sqrt{1+\frac{2W_S}{x_J}} + \sqrt{1+\frac{2W_D}{x_J}} - 2\right)$$

$$W_S = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}2\phi_B} = 1.026\times10^{-5}\text{ cm} \quad W_D = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}(2\phi_B + V_{DS})} = 2.221\times10^{-5}\text{ cm}$$

$$\therefore \Delta V_T = \frac{1.645\times10^{-7}}{C_{ox}} \cdot \frac{0.5\times10^{-4}}{2\cdot1.5\times10^{-4}}\left(\sqrt{1+\frac{2\cdot1.026\times10^{-5}}{0.5\times10^{-4}}} + \sqrt{1+\frac{2\cdot2.221\times10^{-5}}{0.5\times10^{-4}}} - 2\right)$$

$$= \frac{2.742\times10^{-8}}{C_{ox}}(1.1881 + 1.374 - 2)$$

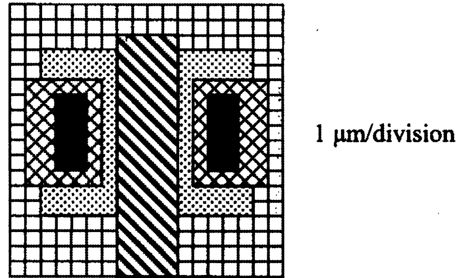
$$= \frac{1.541\times10^{-8}}{C_{ox}}$$

$$= 0.0446\text{ V} \qquad \text{for } t_{ox} = 10\text{ nm}$$

$$= 44.6\text{ mV}$$

Student #:____________________

10. A MOSFET has a layout as illustrated in the diagram below.



(a) What are the three types of capacitance present in a MOSFET structure?

Depletion copacitance
Extrinsic copacitance
Intrinsic copacitance

(b) The intrinsic capacitances, C_{GS} and C_{GD} change with biasing condition. Under what biasing conditions are they equal? What is their value as a function of C_{ox} under these conditions?

$C_{GS} = C_{GD}$ when $V_{DS} = 0$

$$C_{GS} = C_{GD} = \frac{2}{3} C_{ox} \left[1 - \left(\frac{(V_{GS} - V_T)}{2(V_{GS} - V_T)} \right)^2 \right]$$

$$= \frac{2}{3} C_{ox} \cdot \frac{3}{4}$$

$$= \frac{C_{ox}}{2} \text{ for } V_{DS} = 0$$

(c) If $t_{ox} = 25$ nm, if $N_A = 5\text{x}10^{16}$ cm^{-3} what is C_{GS} for the structure above if the lateral diffusion extends 0.3 μm under the gate for $V_{DS} > V_{DS,sat}$?

Above $V_{DS,sat}$, $C_{GS} = \frac{2}{3} C_{ox}$

$$\therefore C_{GS} = \frac{2}{3} \frac{C_{ox}}{t_{ox}} W \cdot L$$

$$= \frac{2}{3} \frac{3.9 \cdot 8.854 \times 10^{-14}}{25 \times 10^{-7}} \cdot (11 \times 10^{-4})(3.4 \times 10^{-4})$$

$$= 3.44 \times 10^{-14} F.$$

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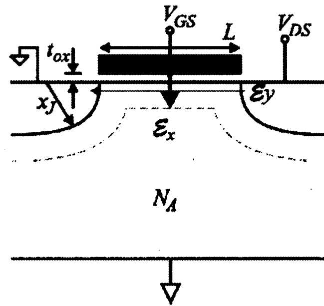
11. A MOSFET is illustrated in the diagram below showing the various parameters and applied biases.



(a) How do each of the labeled parameters and biases change under "constant field scaling" with a scaling factor of ξ?

$t_{ox} \to t_{ox}/\xi$ $\quad V_{DS} \to V_{DS}/\xi$

$L \to L/\xi$ $\quad V_{GS} \to V_{GS}/\xi$

$x_J \to x_J/\xi$

$N_A \to \xi N_A$

(b) If the value of V_{DS} can't be scaled down as rapidly as the effective gate length, L, what will eventually happen to the carrier mobility? Why?

Eventually the effective mobility will go down as $\frac{\mu_0}{1+\mathcal{E}/\mathcal{E}_{crit}}$. This is a velocity saturation effect due to high fields in the material.

(c) For a transistor with an effective gate length of $L = 2.5$ μm the applied V_{DS} =5 V results in a drop of 50% in I_D with respect to the low field condition. What is the value of the critical field, $\mathcal{E}_{crit}$?

$$\frac{I_D'}{I_D} = 0.5 = \frac{1}{(1 + V_{DS}/(L\mathcal{E}_{crit}))}$$

$$\Rightarrow \quad (1 + V_{DS}/(L\mathcal{E}_{crit})) = 2$$

$$\mathcal{E}_{crit} = \frac{V_{DS}}{L} = \frac{5}{2.5\times10^{-4}} = 2\times10^4 \text{ V/cm}$$