

CARLETON UNIVERSITY
School of Computer Science

COMP 2003A Computer Organization

Fall 2004

Mid-term solution key

Question 1 [4 points] 2 marks each.

a) $\overline{A} \overline{B} + \overline{B} \overline{D}$

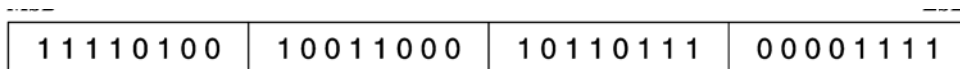
b) $\overline{A} \overline{C} + C D + C \overline{B}$

Note: 0.5 mark each is taken off if the K-map simplification method is not used.

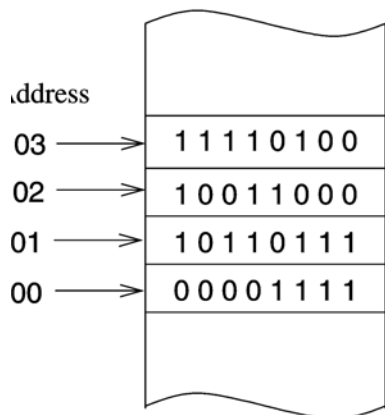
Question 2 [6 marks] Short answer questions (Use the reverse side if you need more space)

a. **(3 marks)**

When we want to store a data item that needs more than one byte, we can store it in one of two ways. In the little-endian scheme, multibyte data is stored from least significant byte to the most significant byte as shown below.



(a) 32-bit data



(b) Little-endian byte ordering

b. (3 marks)

The three-address format gives the addresses required by most operations: two addresses for the two input operands and one address for the result. However, some processors like the Pentium compromise by using the two-address format because operands in these processors can be located in memory (leading to longer addresses). This is not a problem with the modern RISC processors as they use the store/load architecture. In these processors, most instructions find their operands in registers; the result is also placed in a register. Since registers can be identified with a shorter address, using the three-address format does not unduly impact the instruction length.

Question 3 [6 marks] Short answer questions (Use the reverse side if you need more space)

a. (3 marks)

MIPS stands for millions of instructions per second. Although it is a simple metric, it is practically useless to express the performance of a system. Since instructions vary widely among the processors, a simple instruction execution rate will not tell us anything about the system. For example, complex instructions take more clocks than simple instructions. Thus, a complex instruction rate will be lower than that for simple instructions. The MIPS metric does not capture the actual work done by these instructions. MIPS performance metric is perhaps useful in comparing various versions of processors derived from the same instruction set.

b. (3 marks)

Memory can be viewed as consisting of an ordered sequence of bytes. In byte addressable memory, each byte is identified by its sequence number starting with 0. This is referred to as the memory address of the byte.

If the processor has a 26-bit address bus, it can address 2^{26} bytes (or 64 MB) of memory.

Question 4 [9 marks]

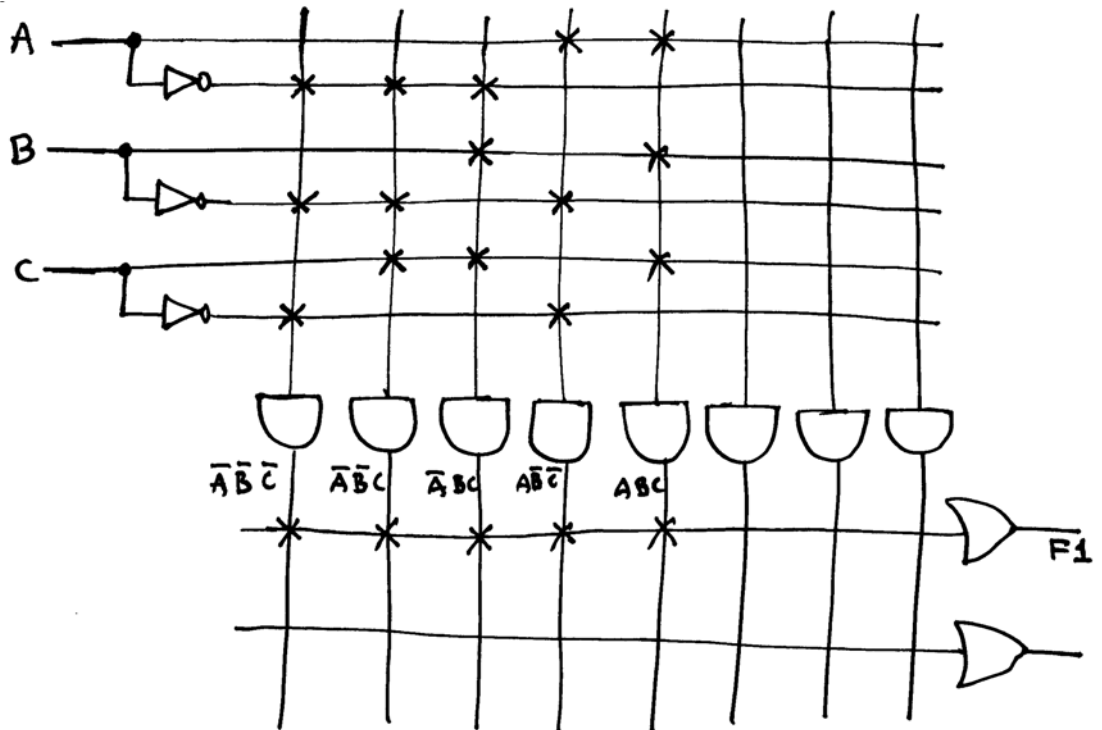
a) (1.5 marks)

$$\bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + \bar{A} B C + A \bar{B} \bar{C} + A B C$$

b) (1.5 marks)

$$(A + \bar{B} + C) (\bar{A} + B + \bar{C}) (\bar{A} + \bar{B} + C)$$

c) (6 marks)

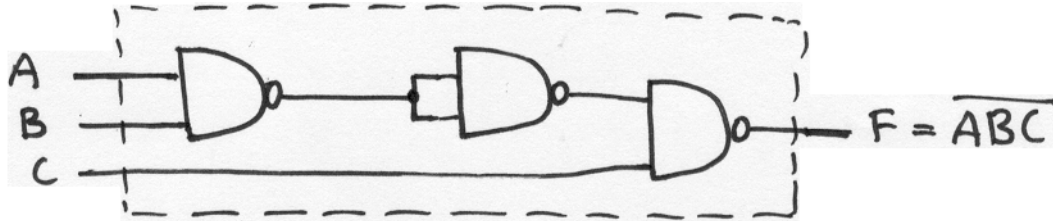


AND array connections: 4 marks

OR array connections: 2 marks

Question 5 [5 marks]

a) (2 marks)



b) (3 marks)

$$\begin{aligned}
 & (A+B) \cdot (A+\bar{B}) \cdot (\bar{A}+B) \\
 &= (\underbrace{A \cdot A}_A + B \cdot A + A \cdot \bar{B} + \underbrace{B \cdot \bar{B}}_0) (\bar{A}+B) \\
 &= (\underbrace{A(1 + \cancel{B} + \bar{B})}_A) (\bar{A}+B) \\
 &= A(\bar{A}+B) \\
 &= \underbrace{A \cdot \bar{A}}_0 + A \cdot B \\
 &= \boxed{A \cdot B}
 \end{aligned}$$