Faculty of Engineering
School of Electrical Engineering
and Computer Science

ELG5195 Digital Logic Design: Principles and Practices

uOttawa
L'Université canadienne
Canada's university

NAME / ID# (UofO /Carleton)

Quiz 2
2014

Even

Q1. The state table of a logic circuit which has a unique one-bit external input ***m*** and one output ***z*** is given below. **15 pts = 4+9+2**

1.1. Assuming that JK flip-flops are used in the implementation, extend the state table with the excitation table of the circuit (inputs of the flip-flops). **4 pts**

Use JK excitation table to find J and K columns directly for each row, or indirectly by applying these rules to parts of columns:

J <= Q^{n+1} if Q^n = 0 (*copy next state where present state is* 0)
J <= x if Q^n = 1 (*put* don't care *where present state is* 1)
K <= Q^{n+1} if Q^n = 1 (*copy complement of the next state where present state is* 1)
K <= x if Q^n = 0 (*put* don't care *where present state is* 0)

PresentState		*Input*	*Next State*		*Output*	1 pt	1 pt	1 pt	1 pt
A^n	B^n	m	A^{n+1}	B^{n+1}	z	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	x	0	x
0	0	1	0	1	0	0	x	1	x
0	1	0	0	0	0	0	x	x	1
0	1	1	1	1	0	1	x	x	0
1	0	0	x	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x	x
1	1	0	1	1	0	x	0	x	0
1	1	1	0	0	1	x	1	x	1

1 pt $z = A\,m$

1.2 Find simplified expressions for each flip-flop inputs and of the circuit's output. **9 pts**

2 pts $J_A = B\,m$

J_A	m=0	m=1
AB=00	0	0
AB=01	0	1
AB=11	x	x
AB=10	x	x

2 pts $J_B = m$;

J_B	m=0	m=1
AB=00	0	1
AB=01	x	x
AB=11	x	x
AB=10	x	x

K_A	m=0	m=1
AB=00	x	x
AB=01	x	x
AB=11	0	1
AB=10	x	x

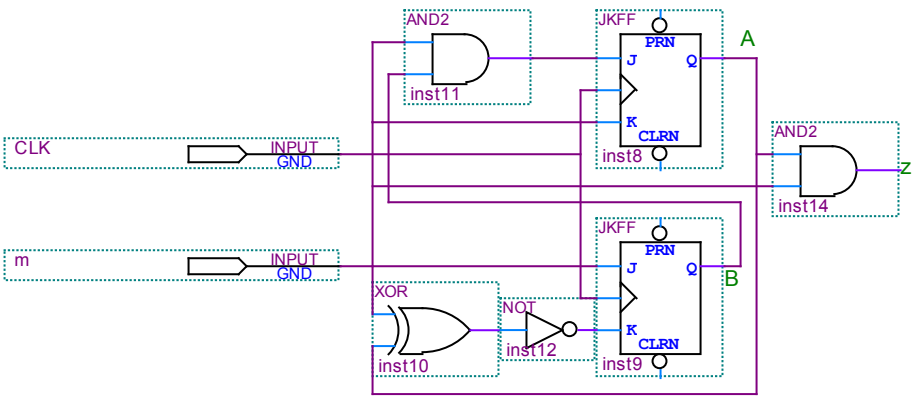
2 pts; $K_A = m$

K_B	m=0	m=1
AB=00	x	x
AB=01	1	0
AB=11	0	1
AB=10	x	x

2 pts $K_B = (m \oplus A)'$

1.3 Draw the logic diagram (schematics) of this circuit.

2 pts



Q2. Consider the incompletely specified sequential circuit with a one-bit external input ***p*** and one output ***z*** as described by the state table below. **15 pts=10+5**

present state	next state p= 0	next state p=1	output z p=0	output z p= 1
A	A	B	0	0
B	A	C	-	0
C	D	D	-	1
D	E	C	-	0
E	A	B	-	-

2.1. Reduce the incompletely specified state table using implication diagram. 10 pts = 8+2

Recall that two states p and q of an *incompletely specified sequential* network are compatible ($p \sim q$) iff for every single input X

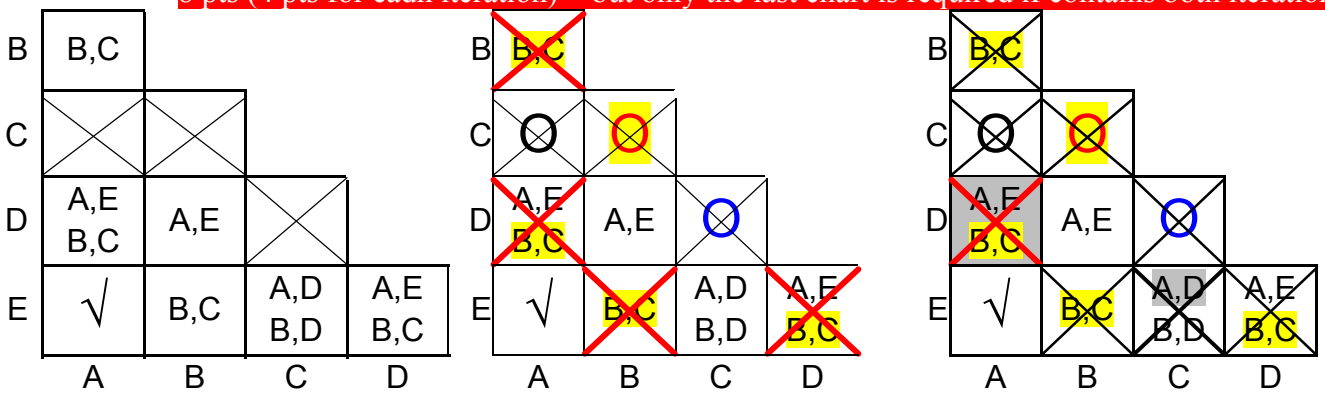
1. the outputs are the same $\boldsymbol{\lambda(p,X)= \lambda(q,X)}$ when both are specified *and*
2. the next states are *compatible* $\boldsymbol{\delta(p,X) \sim \delta(q,X)}$ if both specified

In each cell should be written:

√ if p and q are redundant, i.e., $\boldsymbol{\delta(p,X) = \delta(q,X)}$

X if p and q are incompatible (do not respect any of rules 1 or 2 *IMPLIED COMPATIBLE PAIR OF STATES (which condition compatibility of the compared states)*.

8 pts (4 pts for eadh iteration) = but only the last chart is required if contains both iterations



Can use either the Merger Diagram or the following table to find the maximal compatibilities

Compatible States	Implied Compatibilities	2 pts Maximal Compatibilities
B,D	A,E	(A,E), (B,D), C
A,E	√	S_0, S_1, S_2

present state		next state p= 0	next state p=1	output z p=0	output z p= 1
S_0	A	A	B	0	0
	E	A	B	-	-
S_1	B	A	C	-	0
	D	E	C	-	0
S_2	C	D	D	-	1

2.2. Provide the state table of the reduced machine.

5 pts = only one of the last 2 tables is required

present state		next state p= 0	next state p=1	output z	p=1
A	S_0	A S_0	B S_1	0	0
E	S_0	A S_0	B S_1	0	0
B	S_1	A S_0	C S_2	-	0
D	S_1	E S_0	C S_2	-	0
C	S_2	D S_1	D S_1	-	1

Reduced table (Mealy)

present state	next state p= 0	next state p=1	output z p=0	output z p= 1
S_0	S_0	S_1	0	0
S_1	S_0	S_2	-	0
S_2	S_1	S_1	-	1

Reduced table (Moore)

present state	next state p= 0	next state p=1	out z
S_0	S_0	S_1	0
S_1	S_0	S_2	0
S_2	S_1	S_1	1