DIGITAL DESIGN COEN 312 – FINAL EXAM
April 17th, 2013

Instructor: Dr. J. Trajkovic and Dr. S. Das

- Answer all questions.

Instructions:
- Time Allowed 3 hr.
- No calculators, phones, computers or other materials are allowed.

Question 1 (total 10 points)

2's complement is used to represent all of the following 4-bit **signed** binary in this question.

a) (2 points) Perform addition of C and D. Show all the steps.
C = 0101 D = 0110

b) (2 points) Does this addition of C and D (as specified in **a)**) generate an overflow? How could you detect it by looking at the binary values of operands and carry?

c) (2 points) Perform subtraction (E - F) of the given numbers using 2's complement of the subtrahend and addition. Convert the result to decimal system (make sure to show the sign of the result). Show all the steps.
E = 1101 F = 1100

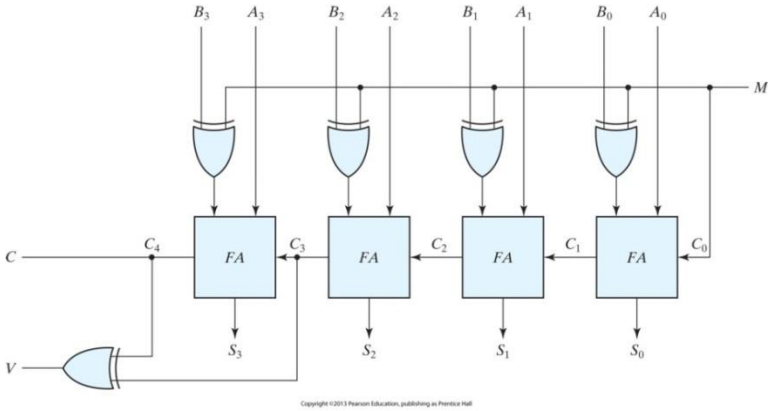


Figure 1.Four-bit adder subtractor circuit

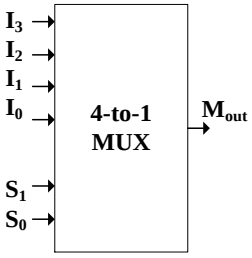
d) (2 points) Using the adder-subtractor circuit shown in the Figure 1 perform **addition** of the numbers G and H. State the values on the inputs ($B_3B_2B_1B_0$, $A_3A_2A_1A_0$, and M), and outputs ($S_3S_2S_1S_0$, C, V). What do the values C and V indicate?
G = 1010 H = 0101

e) (2 points) Using the adder-subtractor circuit shown in the Figure 1 perform **subtraction** of the numbers I and J (I - J). State the values on the inputs ($B_3B_2B_1B_0$, $A_3A_2A_1A_0$, and M), and outputs ($S_3S_2S_1S_0$, C, V). What do the values C and V indicate?
I = 0101 J = 1010

Question 2 (total 14 points)
Clearly mark all inputs, outputs, gates, wires and components.

a) (3 points) Derive the block diagram of a 4-to-1 multiplexer using multiple 2-to1 multiplexers.

S_1S_0	M_{out}
00	I_0
01	I_1
01	I_2
11	I_3



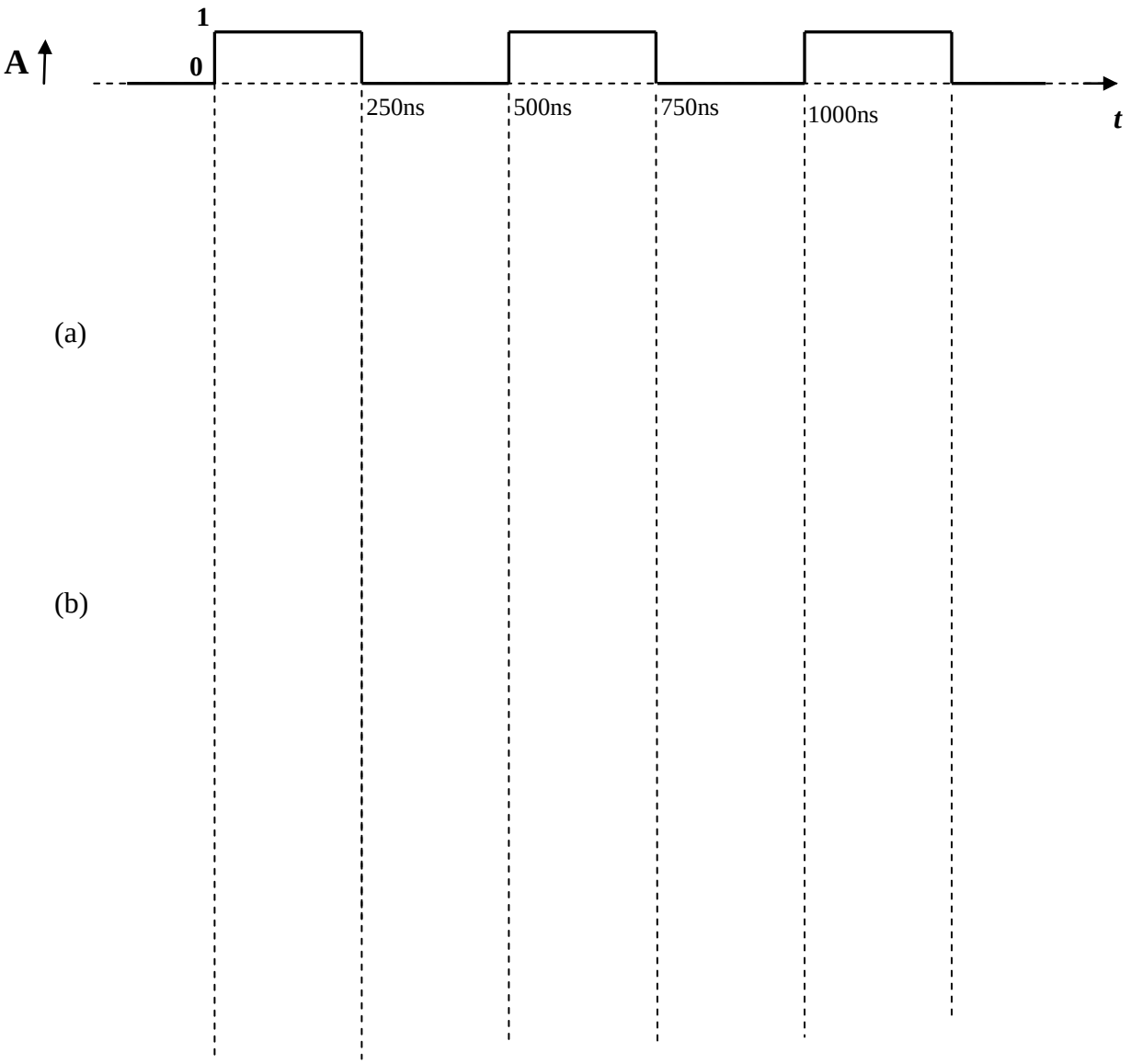
b) (3 points) Using a decoder and 2-input external gates, design a combinational circuit that performs the following Boolean function. The decoder has **active high** outputs.
$F_1(A,B,C) = AB'C' + A'C + ABC$

c) (8 points) Using *half adders, full adders and external gates* (as needed) design a circuit that calculates X^2+1. $X = X_1X_0$ is a two bit **unsigned** binary number. Derive the circuit that has the smallest total number of gates.

3. The input **A** of the circuit of Fig. 3 is a 2 MHz signal shown below. Draw the timing diagram of the output **B** assuming:

   (a) ideal gates with no propagation delay;

   (b) a propagation delay of 10 ns for the NAND gate and a delay of 20 ns for the XOR gate.



(a)

(b)

Question 4 (total 8 points)

Implement a **JK** flip-flop using a D flip-flop. For that purpose:

a) (2 points) Write the table of a JK flip-flop showing the values for (inputs) **J**, **K**, **Q(t)**, and (outputs) **Q(t+1)**, and **D.**

b) (2 points) Obtain the minimized expression for D, using K-maps.

c) (2 points) Draw a logic diagram of the resulting **JK** flip-flop implementation.

d) (2 points) Modify your implementation of part (c) replacing the logic gates by **NAND** gates only.

5. You are to implement a **JK** flip-flop using a **D** flip-flop. For that purpose:

   (a) Write the truth table of a JK flip-flop showing **J**, **K**, **Q(t)**, **Q(t+1)**, and **D** ;

   (b) Obtain the minimized expression for **D** ;

   (c) Draw the resulting **JK** flip-flop implementation;

   (d) Modify your implementation of part (c) replacing the logic gates by **NAND** gates only.

6. A state machine with a serial input **X** is used to detect a non-overlapping input pattern of '**101**' . Its output is always a '**0**' unless it detects a pattern of '**101**'. An example of the input **X** and the resulting output **Y** is given below:

X: ... 0 1 0 0 0 1 0 1 0 0 1 1 0 0 1 0 1 0 1 0 ...

Y: ... 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 ... (Mealy)

Y: ... 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 ... (Moore)

   Draw the state transition diagram of:

   (a) Mealy FSM ;

   (b) Moore FSM.

7. Design a synchronous counter with the following count sequence:

   1, 3 , 5, 7 , 1.

   To make the counter sure-starting, the unused counts (i.e. o, 2, 4, and 6) are to have the following sequence:

   0, 2, 4 , 6, 1.

   Use T flip-flops.