High Speed & Low Power VLSI

Assignment # 3

Date: 2014

Question 1

In this assignment we need to use the TSMC 90nm CMOS technology kit.

Conventional CMOS

First of all, we can build the schematic view of the circuit as showed in the figure 1.1

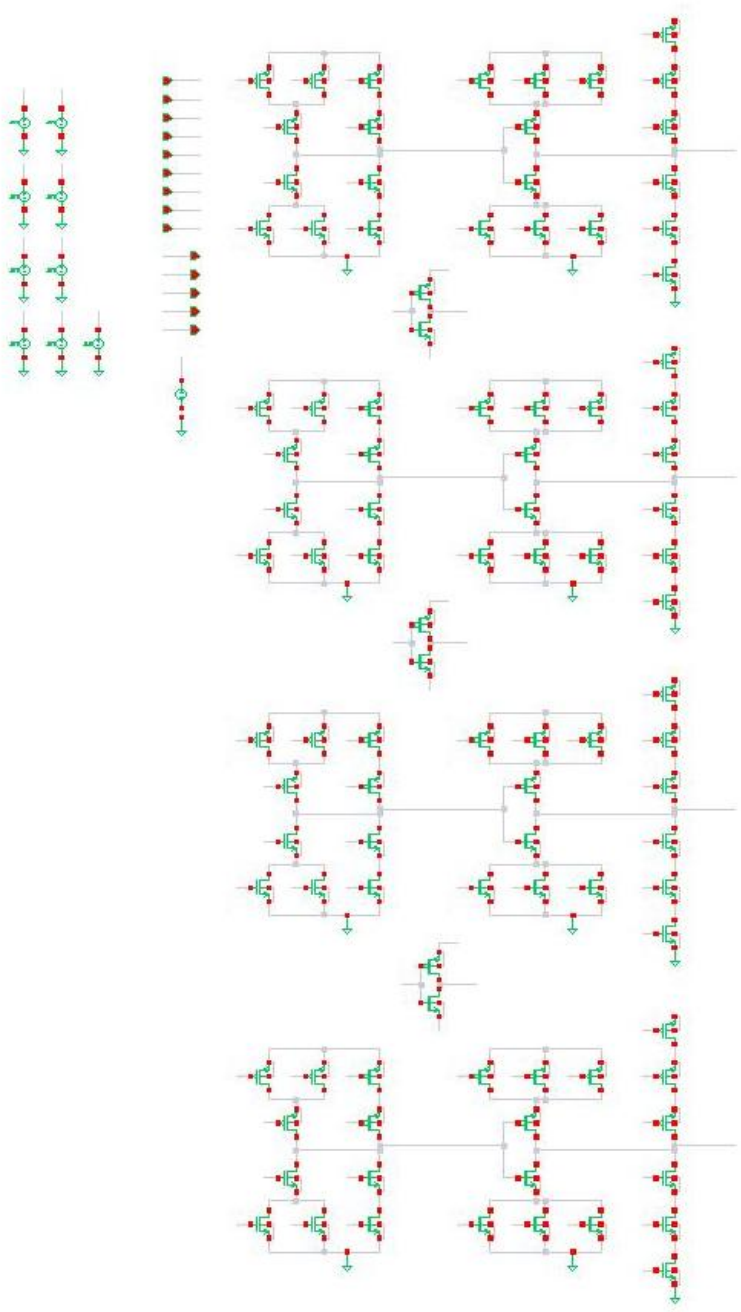


Figure 1.1 schematic view of 4 bit adder

The transistor diagram is showed in the figure 1.2

Next we need to simulate the waveform for 8 different patterns as showed in the figure 1.3

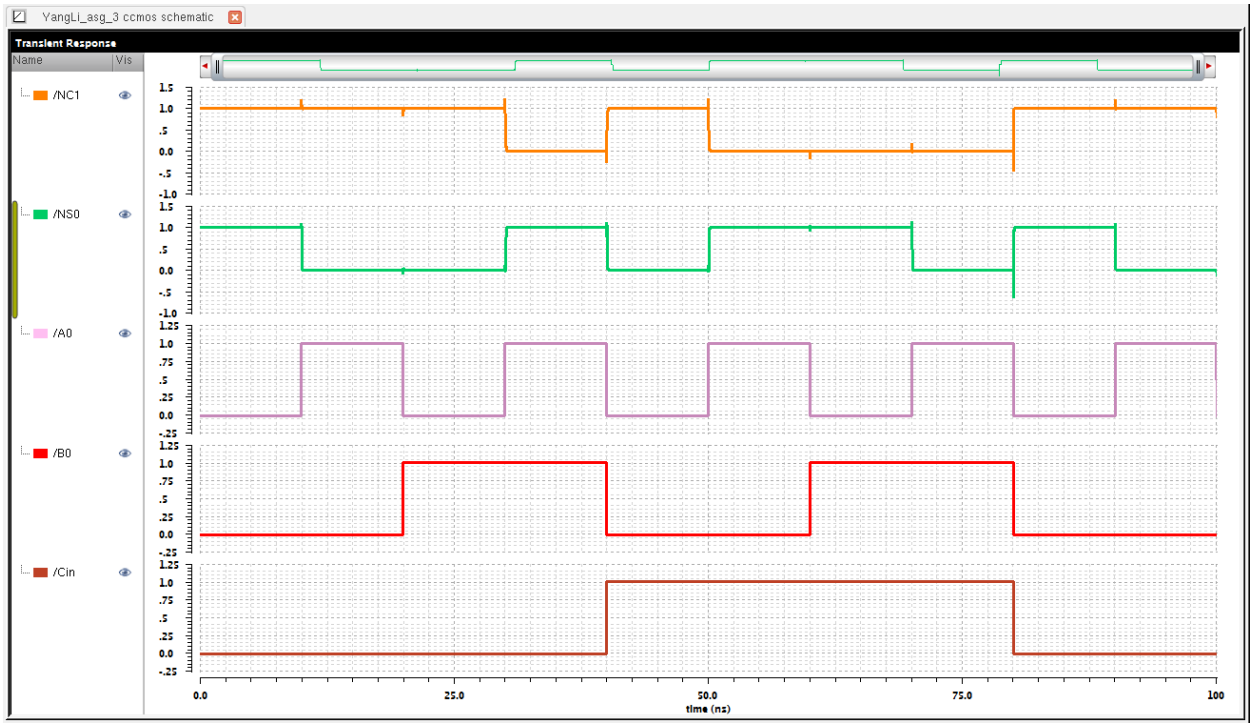


Figure 1.3 waveforms of 8 different patterns

So we can see form the figure 1.3 shows that the adder works correctly which is the same as the truth table 1.1

Table 1.1 truth table for 1-bit adder

Cin	B0	A0	C1	S0	NC1	NS0
0	0	0	0	0	1	1
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	1	1	0
1	0	1	1	0	0	1
1	1	0	1	0	0	1
1	1	1	1	1	0	0

Pass-Transistor Logic

First of all, we can build the schematic view of the circuit as showed in the figure 1.4

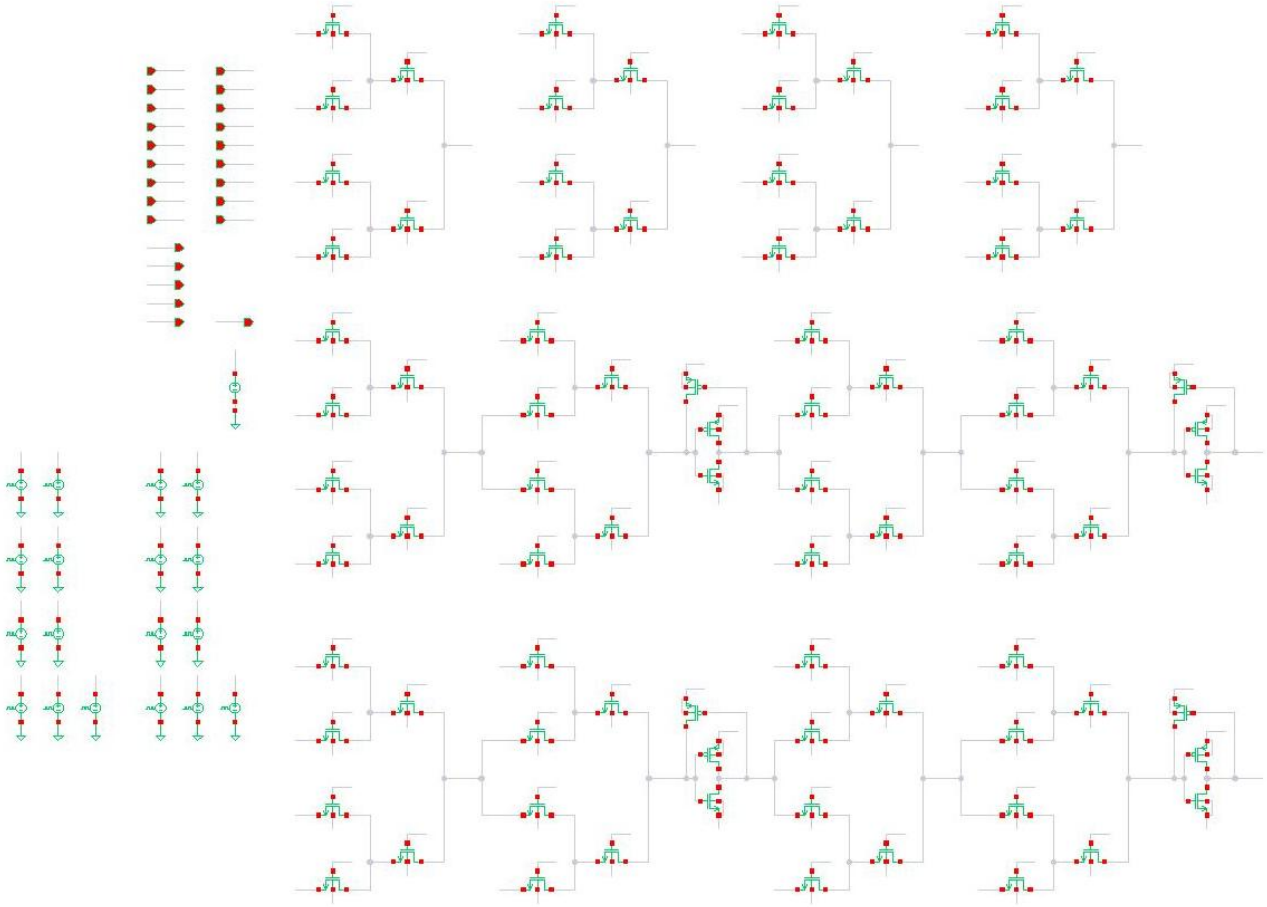


Figure 1.4 schematic view of 4 bit adder

The transistor diagram is showed in the figure 1.5

Next we need to simulate the waveform for 8 different patterns as showed in the figure 1.6

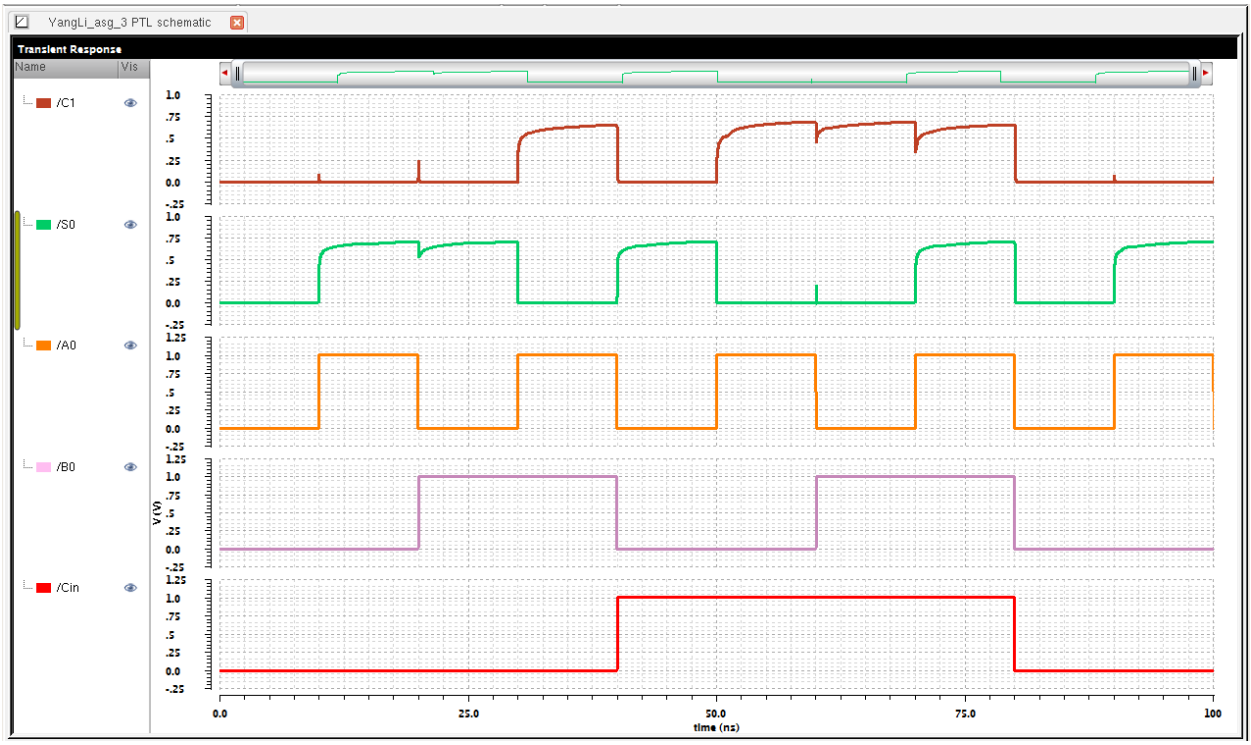


Figure 1.6 waveforms of 8 different patterns

So we can see form the figure 1.6 shows that the adder works correctly which is the same as the truth table 1.1

Domino Logic

First of all, we can build the schematic view of the circuit as showed in the figure 1.7

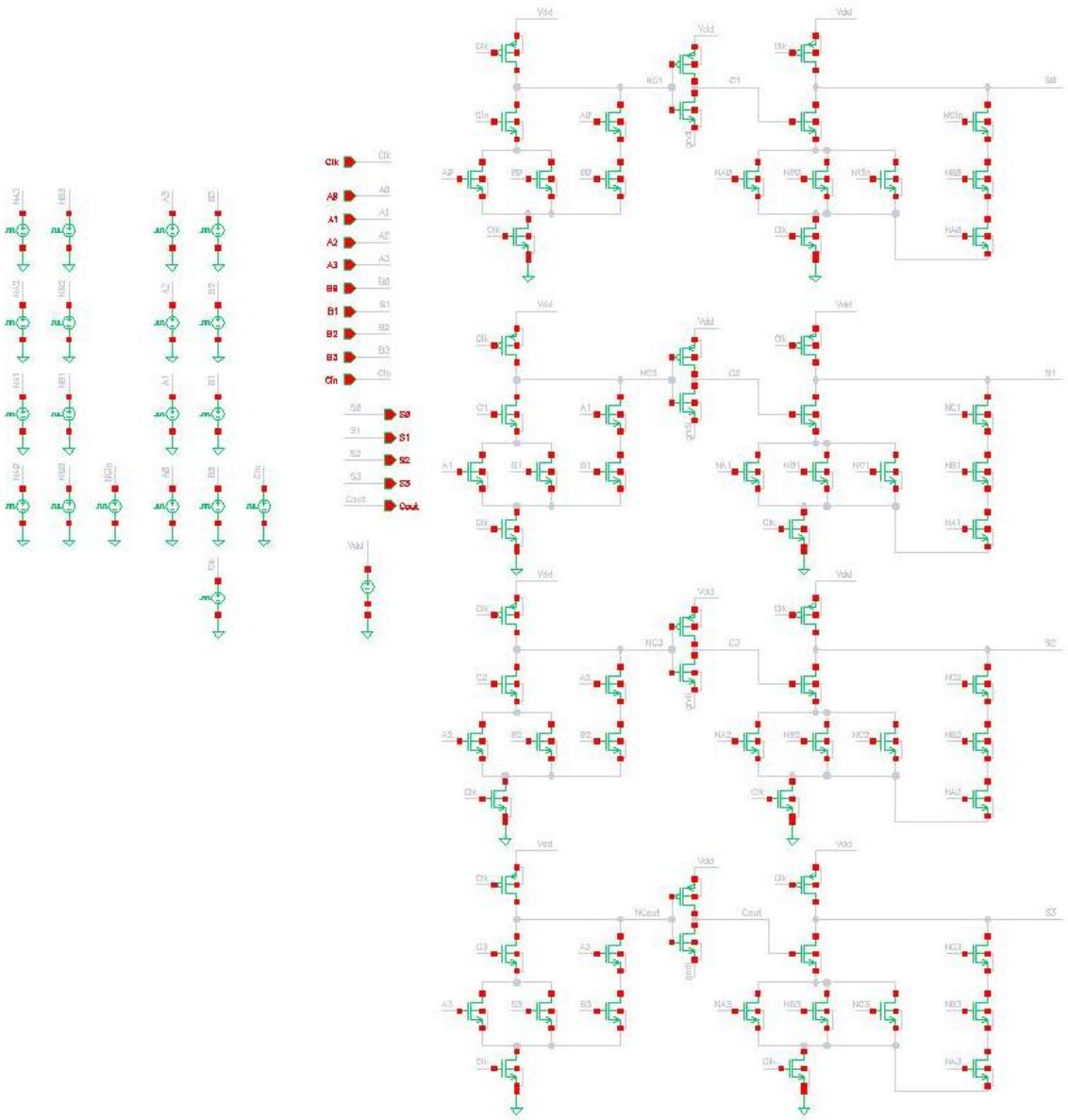


Figure 1.7 schematic view of 4 bit adder

The transistor diagram is showed in the figure 1.8

Next we need to simulate the waveform for 8 different patterns as showed in the figure 1.9

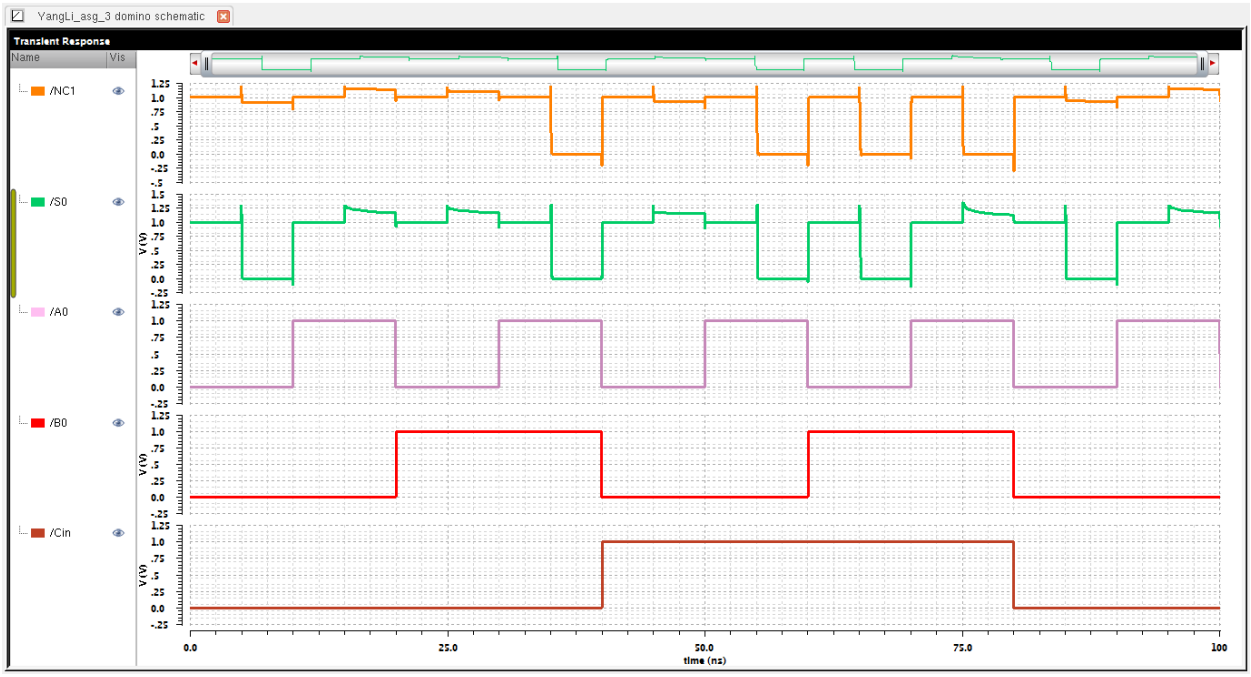


Figure 1.9 waveforms of 8 different patterns

So we can see form the figure 1.9 shows that the adder works correctly which is the same as the truth table 1.1

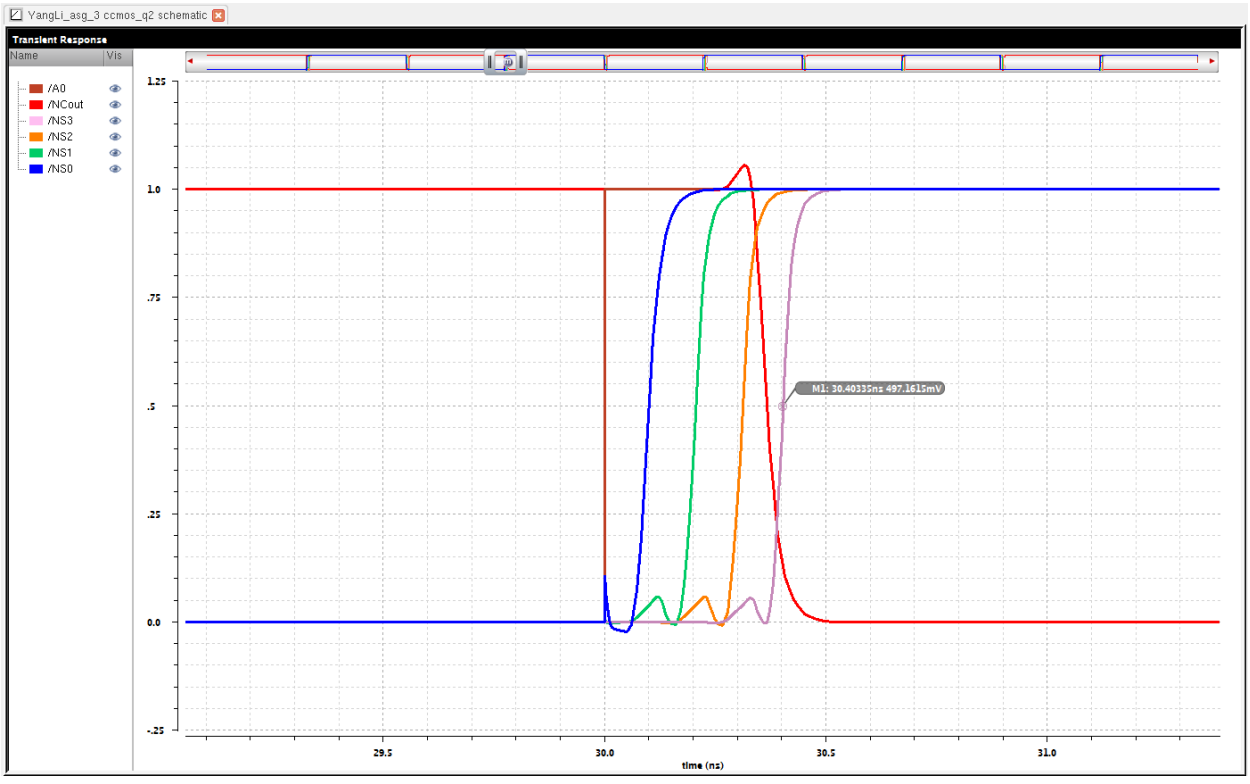
Question 2

In order to measure the worst-case delay we can set the input data like this to make it is a worse-case:

Table 2.1 worst-case delay input data

-	A3	A2	A1	A0	-
-	1	1	1	Change from 0 to 1 and change back	-
-	B3	B2	B1	B0	Cin
-	0	0	0	1	0
Cout	S3	S2	S1	S0	-
Change from 0 to 1 and change back	Change from 1 to 0 and change back	Change from 1 to 0 and change back	Change from 1 to 0 and change back	Change from 1 to 0 and change back	-

And the three results are showed in the figure 2.1 to figure 2.3



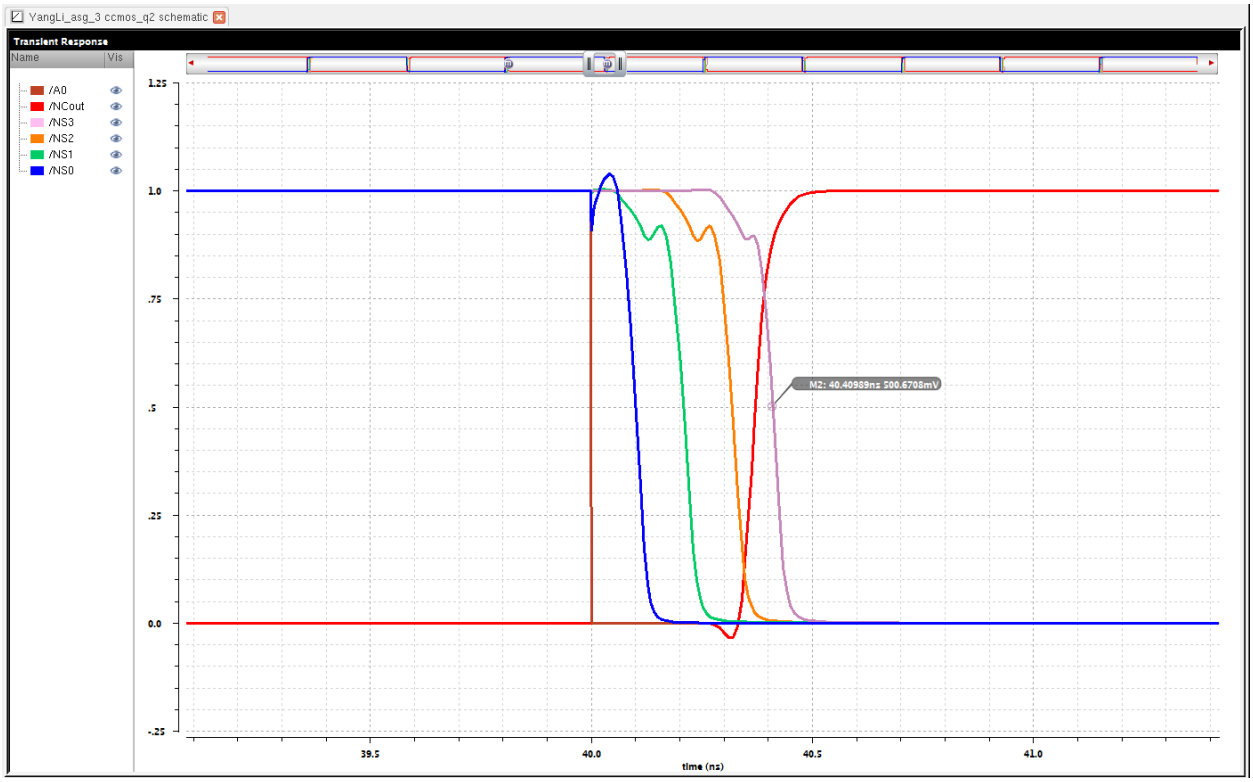
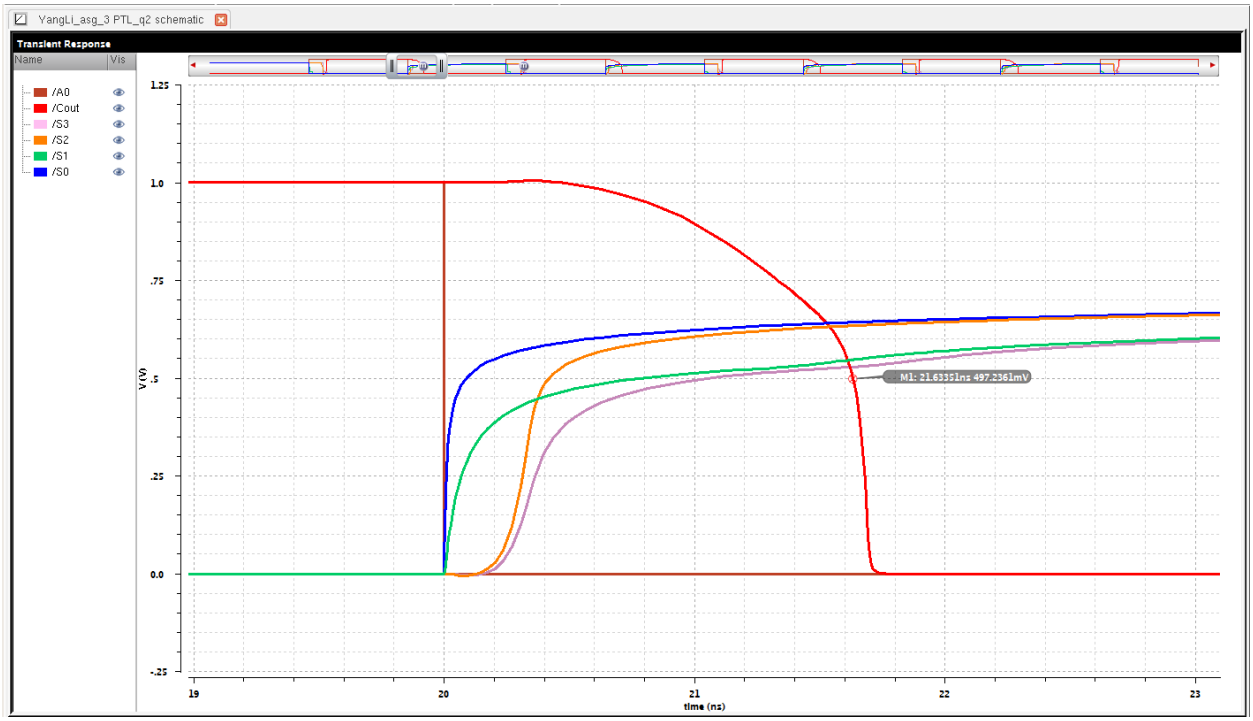


Figure 2.1 the worse-case delay for Conventional CMOS



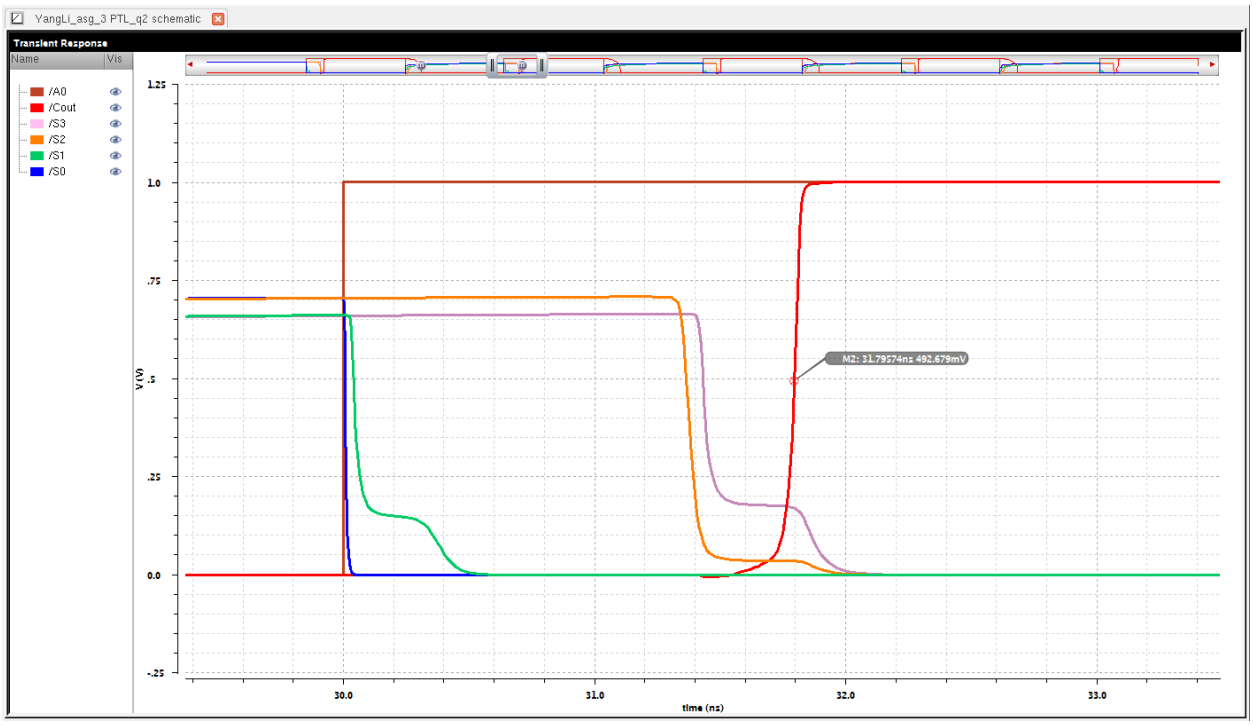


Figure 2.2 the worse-case delay for Pass-transistor logic

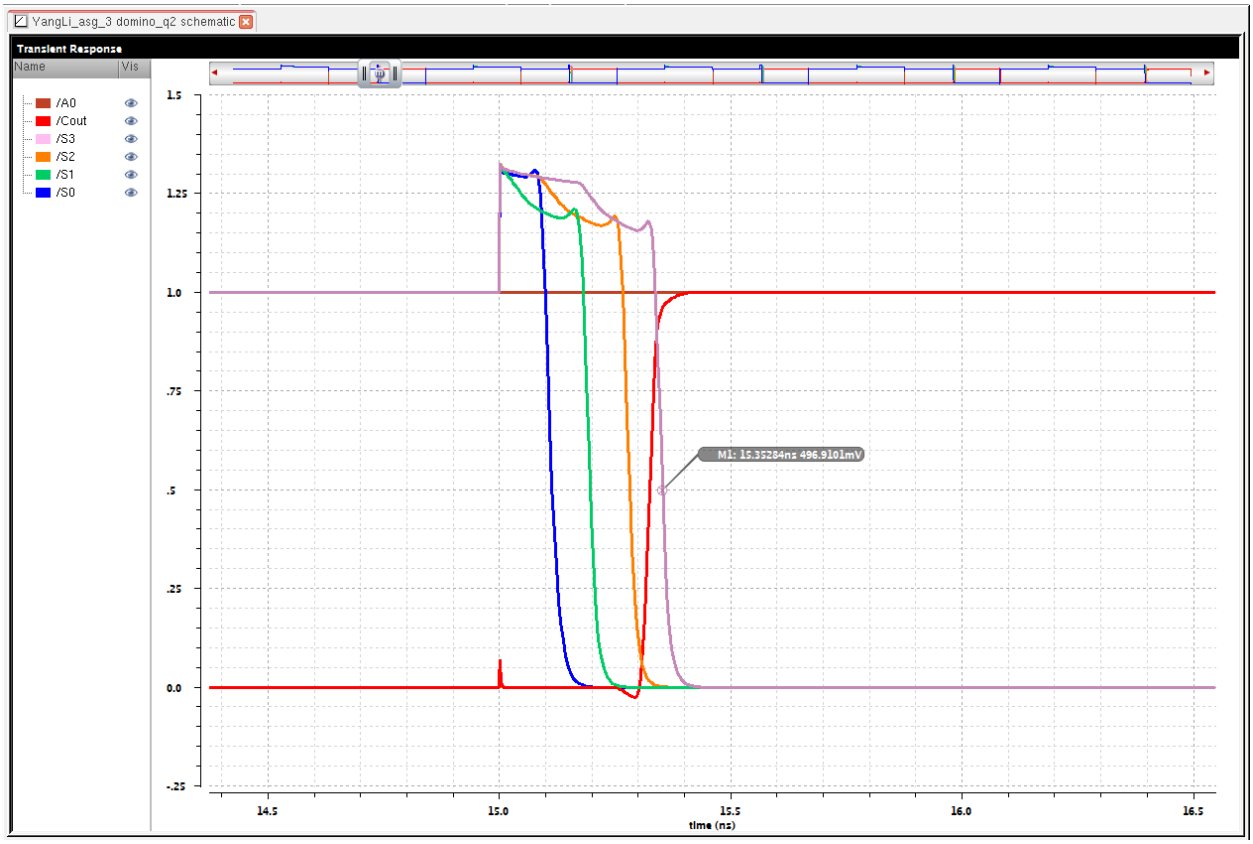


Figure 2.3 the worse-case delay for Domino logic

We can see from the figure 2.1 to figure 2.3 the delay for Conventional CMOS, Pass-transistor logic and Domino logic listed in the table 2.2

Table 2.2 worse-case delay

Type of logic	Worse-case delay of A0 change from 0 to 1 (Delay on evaluation period for Domino logic)	Worse-case delay of A0 change from 1 to 0 (Don not have delay on precharge period for Domino logic)	Worse- case delay
Conventional CMOS	0.403nS	0.409nS	0.406nS
Pass-transistor logic	1.80nS	1.63nS	1.72nS
Domino logic	0.353nS	-	0.353nS

So we can get the maximum frequency and minimum frequency for Conventional CMOS, Pass-transistor logic and Domino logic listed in the table 2.3 and in Domino logic the voltage drop due to the leak current is showed in the figure 2.4

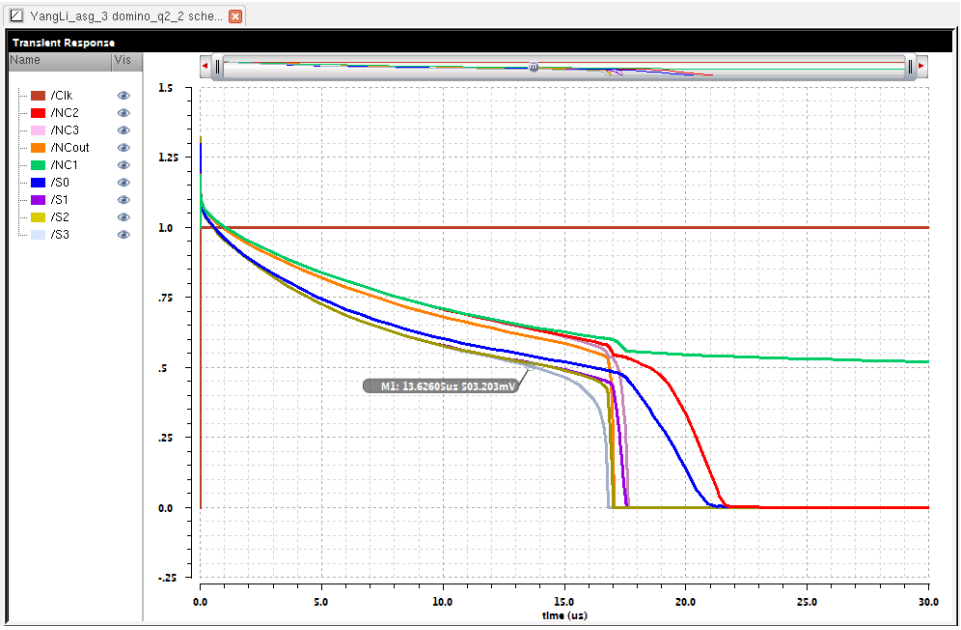


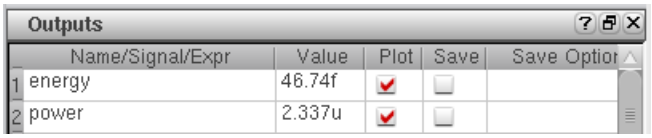
Figure 2.4 the voltage drop in Domino logic

Table 2.3 Frequency

Type of logic	Worse- case delay	Maximum frequency	Minimum frequency
Conventional CMOS	0.406nS	2.45GHz	Don not have minimum frequency for Conventional CMOS
Pass-transistor logic	1.72nS	0.58GHz	Don not have minimum frequency for Pass-transistor logic
Domino logic	0.353nS	2.83GHz	73.4KHz (Clk)

We can get the power consumption energy dissipation (while the switching activity α = 1) in the cadence listed in the table 2.4 and showed in the figure 2.4

for Conventional CMOS



for PTL

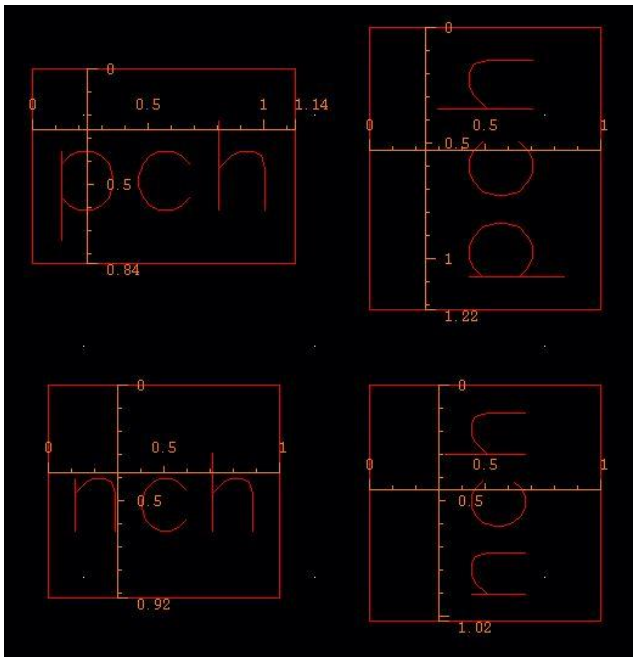
for Domino logic

Figure 2.4 power and energy results

Table 2.4 Power consumption and energy dissipation

Type of logic	Frequency	Power consumption	Energy dissipation
Conventional CMOS	50MHz (Data)	1.296uW	25.92fJ
Pass-transistor logic	50MHz (Data)	2.337uW	46.74fJ
Domino logic	100MHz (Clk)	1.179uW	11.79fJ

As for the area we can get the area for Pmos and Nmos so we can estimate the total area of the adders. The areas for single transistors are showed in the figure 2.5. The result are listed in the table 2.5



(um)

Figure 2.5 areas for single transistors

Table 2.5 Area

Type of logic	Number of Nmos (W=200nm) ($0.92um^2$)	Number of low skew inv Nmos (W=300nm) ($1.02um^2$)	Number of Pmos (W=500nm) ($1.22um^2$)	Number of keeper (Pmos) (W=120nm) ($0.96um^2$)	Total area
Conventional CMOS	51	-	51	-	$109.14um^2$
Pass-transistor logic	72	4	4	4	$79.04um^2$
Domino logic	60	-	12	-	$69.84um^2$

Summary

I listed all the result of question 2 in the table 2.6 below.

Table 2.6 results summary

Type of logic	Worse-case delay	Maximum frequency	Minimum frequency	Power consumption	Energy dissipation	Total area
Conventional CMOS	0.406nS	2.45GHz	Don not have	1.296uW	25.92fJ	$109.14um^2$
Pass-transistor logic	1.72nS	0.58GHz	Don not have	2.337uW	46.74fJ	$79.04um^2$
Domino logic	0.353nS	2.83GHz	73.4KHz	1.179uW	11.79fJ	$69.84um^2$