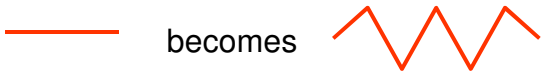
Non-ideal Behavior of Wires

Set # 2

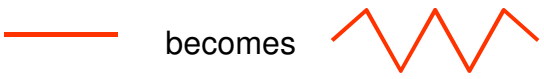
- Interference problems are typically occurred at high frequencies where circuit components such as R, L, C, and wires can have highly non-ideal behavior.
- In circuit theory (@ low frequencies), a wire is theoretically considered as a short circuit. Wire and other circuit components dimensions are not taken into consideration. However, at high frequencies a wire can exhibit significant resistance, inductance, and capacitance that depend on its physical and material properties.
- To Design an EMC device, you need to be aware of such non-ideal behavior of these components to eliminate potential EMI problems

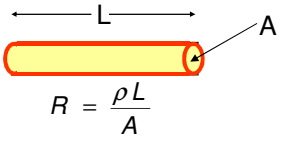


1

Non-ideal Behavior of Wires

1. Most real wires have resistance:

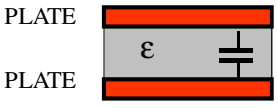




2. Real wires have capacitance

$C = \frac{Q}{V}$

(a) 2 Parallel flat wires



$C = \varepsilon A/s$

(b) 2 Parallel Wires

$C = \frac{2\pi\varepsilon}{\log\left(\frac{s}{r}\right)}$

(c) Coaxial Cable

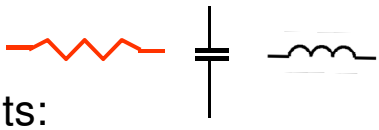
$C = \frac{2\pi\varepsilon}{\log\left(\frac{r_o}{r_i}\right)}$

3. Real wires have inductance

$L = N^2 A \mu / l$
(for a long solenoid)

- They cause time delay and loss

Lumped Versus Distributed Circuits: Lumped Circuits

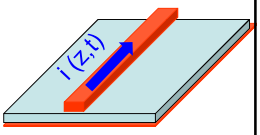


- Lumped circuit elements:
  - Resistor, capacitor, inductor ….
- Lumped circuit elements are defined by

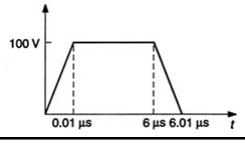
  $v = Ri, \quad v = L\, di/dt$
- Use KVL and/or KCL and involve only one variable, time.
- The travel time of the electric signal is negligible.

3

Distributed Circuits



- Travel time cannot be neglected.
- The voltages and currents in such a circuit are functions of *position* as well as *time*.
- Lumped circuit analysis is substantially simpler than distributed circuit analysis.
- Points for determining whether a circuit should be considered "lumped" or "distributed"
  - Component size versus wavelength (Freq. D.)
  - Pulse rise time versus round propagation trip time (Time domain)



4

Non-ideal Behavior of Wires

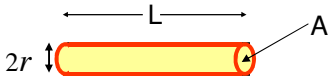
Resistance of Wires

Most *real* wires have resistance:

- R depends on material (σ: conductivity, **S**/m), length: **L**, cross section: **A**

- R causes time delay and loss
- A dc approximation is given by:

$$R = \frac{L}{\sigma A}$$



- At high frequencies, a better approximation is given by:

$$R_{HF} \cong \frac{L}{2r}\sqrt{\frac{f\mu_o}{\pi\sigma}}$$

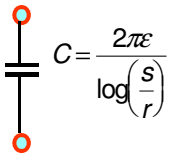
5

Examples:
(s = spacing, r = radius, A = area of plate)

(a) 2 Parallel flat wires

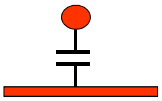
$C = \varepsilon A/s$

(b) 2 Parallel Wires



$$C = \frac{2\pi\varepsilon}{\log\left(\frac{s}{r}\right)}$$

(c) Wire above Ground Plane



$C = 2\pi\varepsilon / \log(2s/r)$

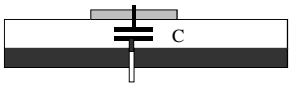
(d) Coaxial Cable

$$C = \frac{2\pi\varepsilon}{\log\left(\frac{r_o}{r_i}\right)}$$

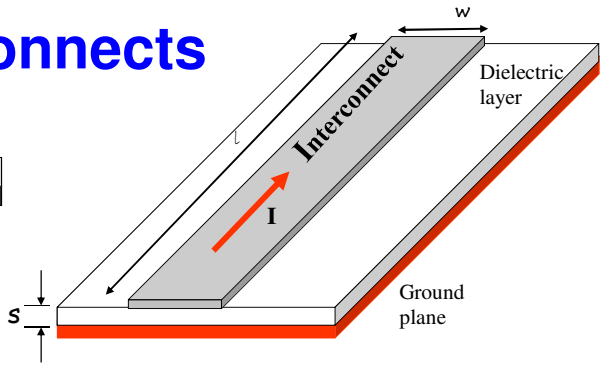
6

Interconnects

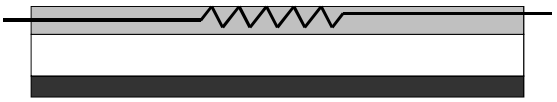
Front View



$C = \varepsilon A_c/s$
$= \varepsilon \, l \, w / s, \quad w > s$



Side View



$R = \rho \, l / A_R$
$= \rho \, l / wd$

- **IDEAL MODEL:**
  - We treat wires as entities along which the voltage is constant and signals (EM waves) as infinitely fast

⇒ No voltage drop & No time delay

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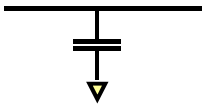
Interconnect Models

- **DISTRIBUTED MODEL**:

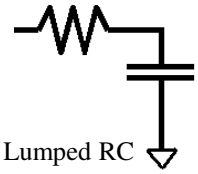
We treat wires as entities along which the voltage can be different and signals (EM waves) as having a finite speed

⇒ voltage drop & time delay

(a) Ideal wire

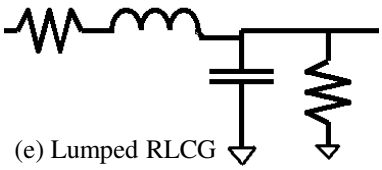


(b) Lumped C



(c) Lumped RC

(d) Lumped LC



(e) Lumped RLCG

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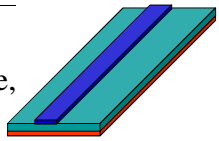
EXAMPLE



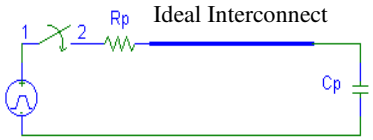
interconnect: 2 mm long, 1 μm thick, and 1.5 μm wide,
ρ = 2.8 μΩ-cm

Substrate: $\varepsilon = 3.8\ \varepsilon_o = 3.365 \times 10^{-11}$ F/cm, 100 nm thick

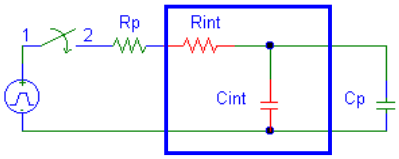
Use: $C = \varepsilon A_c/s = \varepsilon\ (lw)/s$, & $R = \rho\ l/A_R = \rho\ l/(wd)$

Calculate: $R_{int} = 37.3\ \Omega$ & $C_{int} = 1.1 \times 10^{-10}$ F

(1) Ideal circuit model for interconnected gates.



(2) circuit model including interconnect RC-lump model.



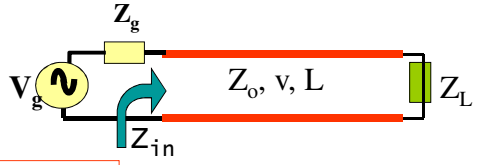
Interconnect RC-lump model.

9

Transmission Lines Equations: Review Summary

Textbook Section 4.5

For forward(+) traveling wave (direction of power flow from generator to load)



$$V(z) = V_o\ e^{-\gamma z} = V_o\ e^{-\alpha z} e^{-j\beta z}$$

where $\gamma = \sqrt{(G + j\omega C)(R + j\omega L)} = \alpha + j\beta$

$$v = \frac{\omega}{\beta} = \frac{\omega}{\omega\sqrt{LC}} = \frac{1}{\sqrt{LC}}$$

$$V(z,t) = \mathrm{Re}[V(z)e^{j\omega t}] = V_o\ e^{-\alpha z}\cos(\omega t - \beta z)$$

With V_o = real #

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o}$$

$$Z_{in} = Z_o \frac{Z_L + j Z_o \tan(\beta l)}{Z_o + j Z_L \tan(\beta l)}$$

For lossless lines:

$$\alpha = 0,\ \beta = \omega\sqrt{LC}\ \ \&\ \ Z_0 = \sqrt{\frac{L}{C}}$$

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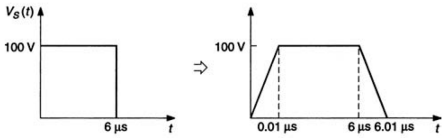
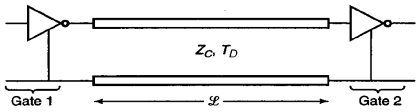
Transmission lines & Digital devices

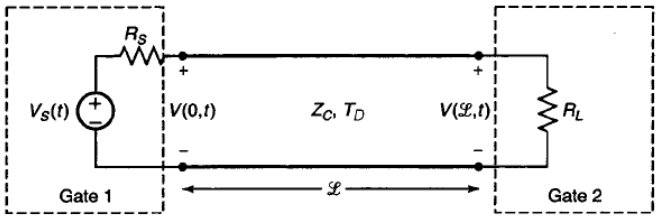


Trapezoid-shaped pulse signal



Line connecting 2 digital gates

Equivalent problem



$$Z_0 = \sqrt{\frac{L}{C}}$$

$$v = \frac{1}{\sqrt{LC}}$$

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o}$$

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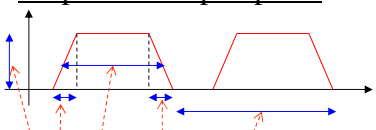
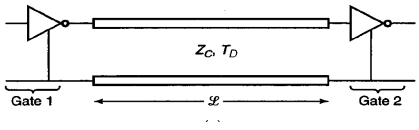
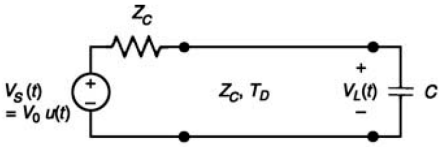
Transmission lines model in PSPICE

Trapezoid-shaped pulse

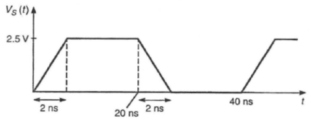


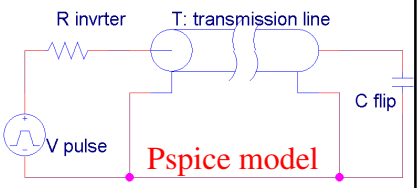
It is defined in terms of:
amplitude, pulse time delay, pulse rise-time, pulse fall-time, pulse width and period.

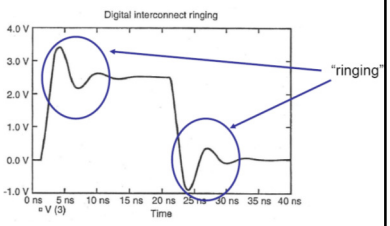




Typical equivalent circuit







Load voltage (Pspice simulation)

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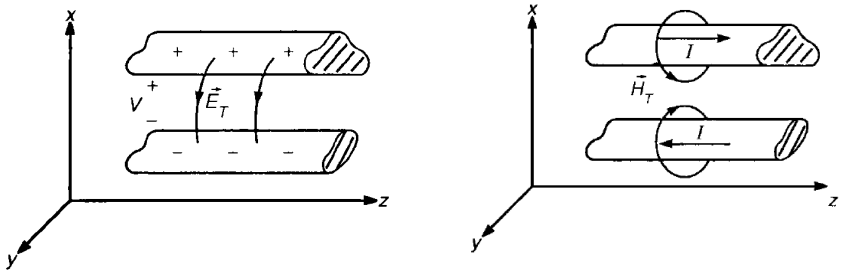
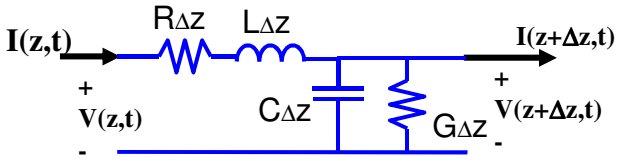
Per unit length parameters (pul) - Sec 4.2

(L, C, R & G)





Note: For lossless system, R=0 and G=0

PUL parameters: Wire-Type Structures

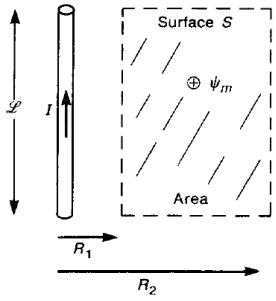
The per-unit-length external inductance is defined as the ratio of the flux penetrating a unit length surface between the wires:

$$l = \frac{\psi_m}{I}$$

Flux due to a current-carrying wire:

$$\psi_m = \int_S \vec{B}_T \cdot \vec{ds} \quad \text{where} \quad \vec{B}_T = \mu_0 \vec{H}_T$$

$$\oint_C \vec{H}_T \cdot \vec{dl} = I_{\text{enclosed}} \Rightarrow \quad H_T = \frac{I}{2\pi r}$$



∴ Flux per unit wire length

$$\psi_m = \int_{r=R_1}^{R_2} \frac{\mu_0 I}{2\pi r}\, dr = \frac{\mu_0 I}{2\pi} \ln\left(\frac{R_2}{R_1}\right)$$

Per unit length parameters (Cont.)

- For TEM wave (E_z and H_z =0), we can compute the per-unit-length inductance l using dc field computations even though the fields will be varying with time.
- If the medium surrounding the two conductors is homogeneous, then c and l are related as

$$lc = \mu\varepsilon$$

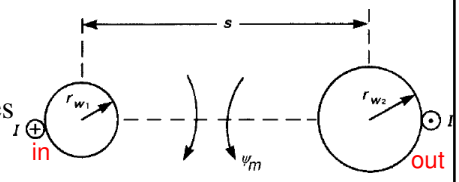
- Hence we only need to determine c or l
- For the case of an inhomogeneous medium as is the case for the microstrip and the PCB, this relations does not apply.

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

PUL parameters: Two parallel wires

A) The per-unit-length inductance

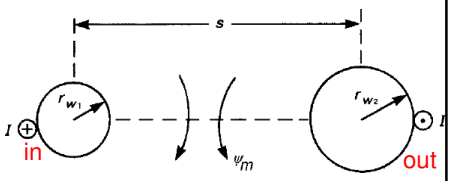
One wire carries a current I directed into the page and the other wire carries a current of the same magnitude but directed out of the page.



$$\psi_m = \frac{\mu_0 I}{2\pi}\ln\left(\frac{s - r_{w2}}{r_{w1}}\right) + \frac{\mu_0 I}{2\pi}\ln\left(\frac{s - r_{w1}}{r_{w2}}\right)$$

$$= \frac{\mu_0 I}{2\pi}\ln\left[\frac{(s - r_{w2})(s - r_{w1})}{r_{w2} r_{w1}}\right]$$

PUL parameters: Two parallel wires



For widely separated wires ($s >> r_{w1}, r_{w2}$)

$$l = \frac{\mu_0}{2\pi}\ln\left(\frac{s^2}{r_{w2}r_{w1}}\right) \quad \text{(in H/m)}$$

Special case ($r_{w1} = r_{w2} = r_w$):

$$l = \frac{\mu_0}{\pi}\ln\left(\frac{s}{r_w}\right)$$

B) The per-unit-length capacitance

$$c = \frac{\mu_0\epsilon_0}{l} \Rightarrow c = \frac{\pi\epsilon_0}{\ln(s/r_w)}$$

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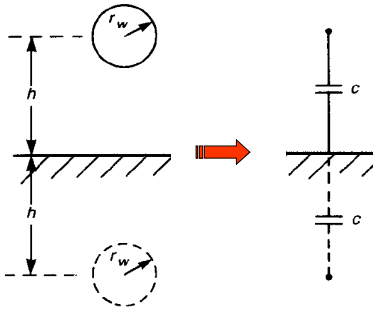
PUL Parameters: one wire above a ground plane

$$c \cong \frac{2\pi\epsilon_0}{\ln(2h/r_w)} \qquad h \gg r_w$$

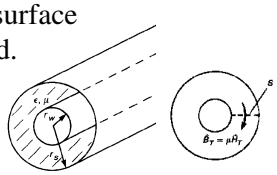
$$l \cong \frac{\mu_0}{2\pi}\ln\left(\frac{2h}{r_w}\right) \qquad h \gg r_w$$



PUL parameters: coaxial cable

- Assume the current I flows along the inner wire surface and returns along the interior surface of the shield.

$$l = \frac{\mu_0}{2\pi}\ln\left(\frac{r_s}{r_w}\right) \qquad c = \frac{\mu_0\epsilon_0}{l}$$



Cross section

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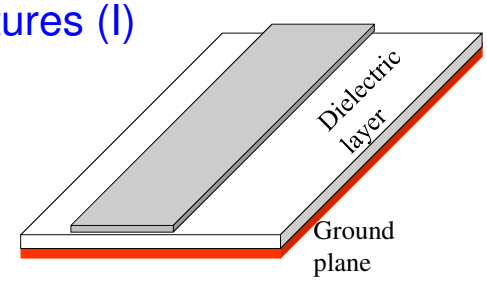
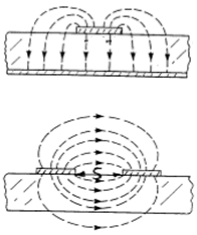
PUL parameters: Printed Circuit Board (PCB) Structures (I)

- The inductance and capacitance per unit length can be determined in terms of the characteristic impedance $\boldsymbol{Z_c}$ and velocity of propagation v as



$$c = \frac{1}{v Z_C} \qquad l = \frac{Z_C}{v} \qquad v = \frac{v_o}{\sqrt{\varepsilon_r'}}$$



v_o is the speed of light

ε'_r is the effective dielectric constant **(?)**

- Generally, the exact per-unit-length parameters cannot be determined in closed form but can be obtained as approximate relations.

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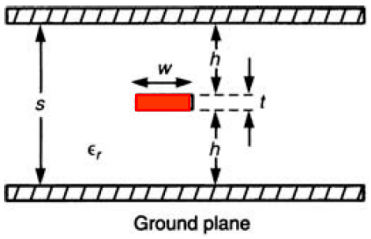
PUL parameters: PCB Structures (II)

Case 1:
A strip-line in a homogeneous medium,

$$\epsilon_r' = \epsilon_r$$



Cross section

$$Z_C = \frac{30\pi}{\sqrt{\epsilon_r}} \frac{1}{\frac{w_e}{s} + 0.441}$$

$$\frac{w_e}{s} = \begin{cases} \frac{w}{s} & \frac{w}{s} \geq 0.35 \\ \frac{w}{s} - \left(0.35 - \frac{w}{s}\right)^2 & \frac{w}{s} \leq 0.35 \end{cases}$$

$$v = \frac{v_o}{\sqrt{\varepsilon_r'}} \qquad c = \frac{1}{v Z_C} \qquad l = \frac{Z_C}{v}$$

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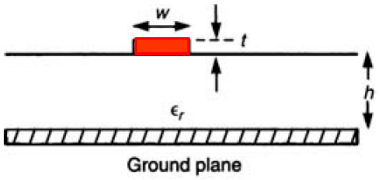
PUL parameters: PCB Structures (III)

Case 2:
The microstrip structure,



Cross section

$$\epsilon_r' = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\frac{1}{\sqrt{1 + 10h/w}}$$

$$Z_C = \begin{cases} \dfrac{60}{\sqrt{\epsilon_r'}} \ln\left[\dfrac{8h}{w} + \dfrac{w}{4h}\right] & \dfrac{w}{h} \le 1 \\ \dfrac{120\pi}{\sqrt{\epsilon_r'}\left[\dfrac{w}{h} + 1.393 + 0.667 \ln\left(\dfrac{w}{h} + 1.444\right)\right]^{-1}} & \dfrac{w}{h} \ge 1 \end{cases}$$

$$v = \frac{v_o}{\sqrt{\varepsilon_r'}} \qquad c = \frac{1}{v Z_C} \qquad l = \frac{Z_C}{v}$$

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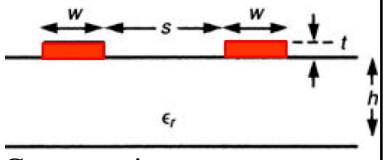
PUL parameters: PCB Structures (IV)

Case 3:
Two lands of width w placed on one side,



Cross section

$$k = \frac{s}{s + 2w}$$

$$\epsilon_r' = \frac{\epsilon_r + 1}{2}\left\{\tanh\left[0.775 \ln\left(\frac{h}{w}\right) + 1.75\right] + \frac{kw}{h}[0.04 - 0.7k + 0.01(1 - 0.1\epsilon_r)(0.25 + k)]\right\}$$

$$Z_C = \begin{cases} \dfrac{120}{\sqrt{\epsilon_r'}} \ln\left(2\dfrac{1 + \sqrt{k}}{1 - \sqrt{k}}\right) & \dfrac{1}{\sqrt{2}} \le k \le 1 \\ \dfrac{377\pi}{\sqrt{\epsilon_r'} \ln\left(2\dfrac{1 + \sqrt{k'}}{1 - \sqrt{k'}}\right)} & 0 \le k \le \dfrac{1}{\sqrt{2}} \end{cases}$$

$$v = \frac{v_o}{\sqrt{\varepsilon_r'}} \qquad c = \frac{1}{v Z_C} \qquad l = \frac{Z_C}{v}$$

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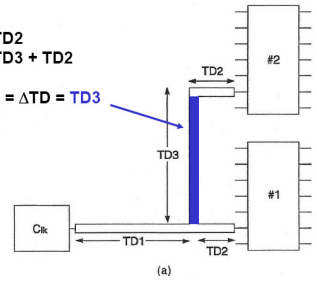
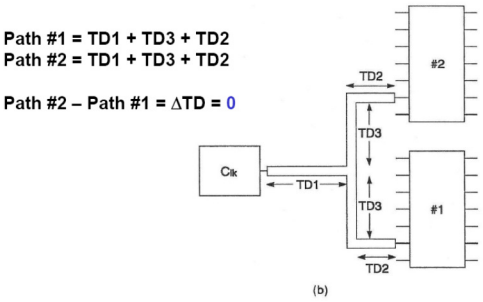
High-Speed Digital Interconnects and Signal Integrity: Section 4.4

Illustration of "clock skew" caused by unequal propagation paths

(a) unequal propagation paths



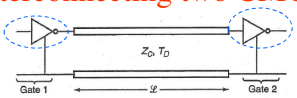


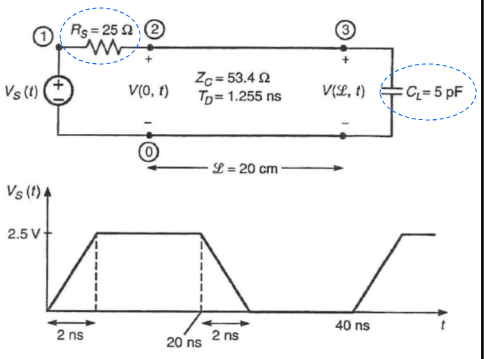
(b) equal propagation paths

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons. 23

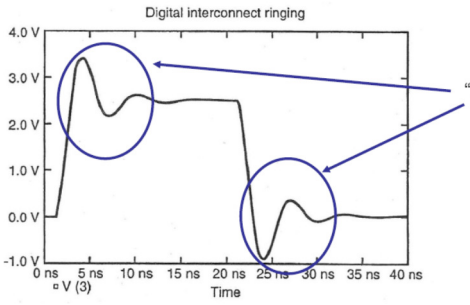
High-Speed Digital Interconnects and Signal Integrity

A typical signal integrity problem: a transmission line interconnecting two CMOS gates;





Simulate, using PSpice:



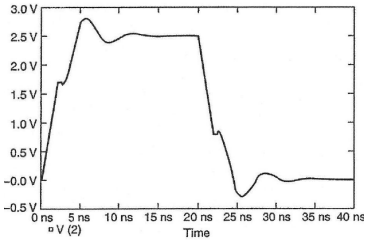
"ringing"

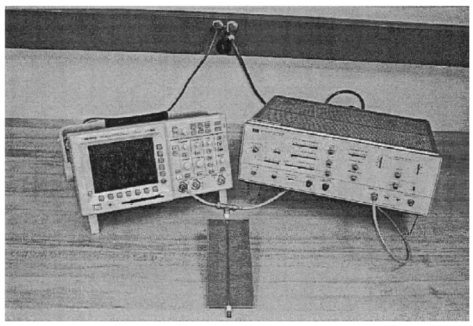
The voltage at the line output (the input to the load CMOS gate) showing the ringing that may cause logic errors.

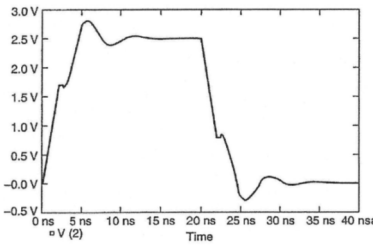
Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons. 24

High-Speed Digital Interconnects and Signal Integrity

PSPICE prediction of the voltage at the input to the line;







Measured voltage at the input to the line.

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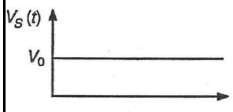
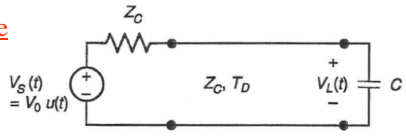
Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

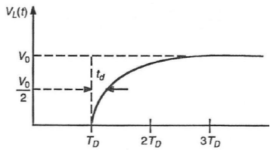
High-Speed Digital Interconnects and Signal Integrity: Termination and Matching Effects

A) Effect of Capacitive Termination

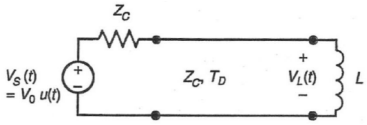


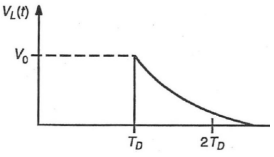
Input signal



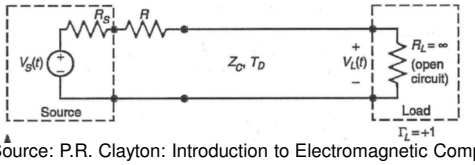


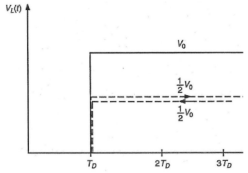
B) Effect of Inductive Termination





C) Effect of Series match

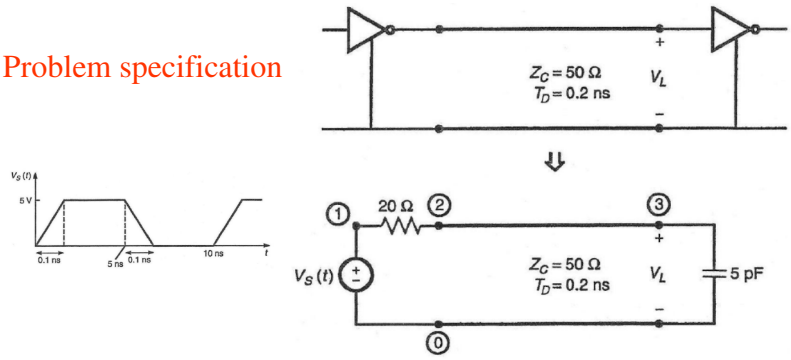




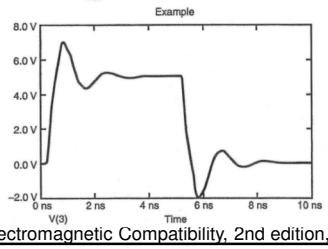
Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

High-Speed Digital Interconnects and Signal Integrity: Effectiveness of Matching Scheme

Problem specification



Pspice Results:
no series matching



Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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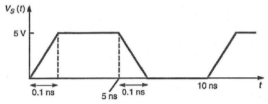
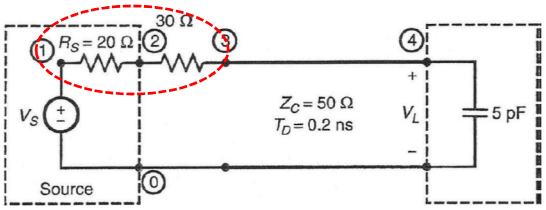
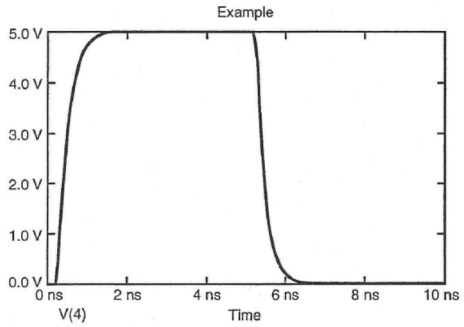
High-Speed Digital Interconnects and Signal Integrity: A) Effectiveness of Series Matching Scheme



Add 30 Ω resistor in series with the source, i.e., matching at the source

PSpice Results:
Applying the **series match** scheme shows that the ringing is eliminated.





Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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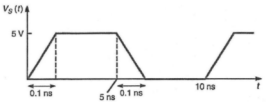
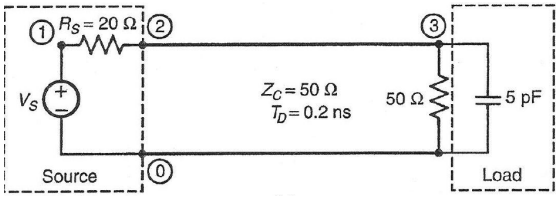
High-Speed Digital Interconnects and Signal Integrity: B) Effectiveness of Parallel Matching Scheme

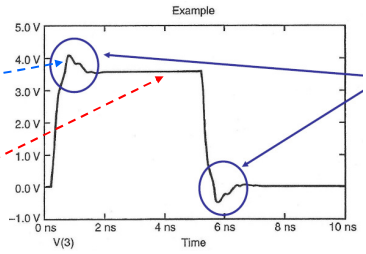




Add 50 Ω resistor in parallel with C, i.e., matching at the load

For the parallel match,

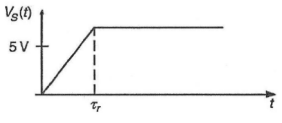
- The line is not completely matched at the load. At high frequencies, the line is not matched.
- The steady-state level the load voltage falls significantly below the desired 5-V level, and logic errors may occur.

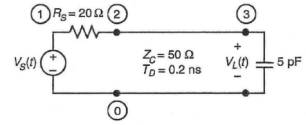


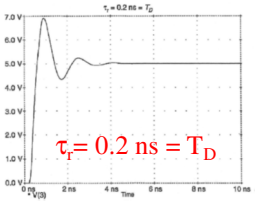
PSpice Results

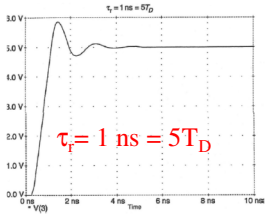
Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons. 29

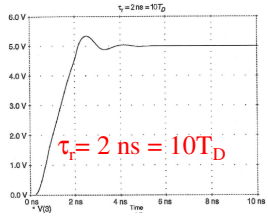
High-Speed Digital Interconnects and Signal Integrity: C) Line Length effect

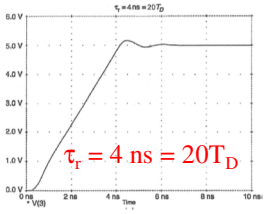












- The distributed parameter effects of the line is negligible if L is electrically short at the highest significant frequency: $L < v/(10F_{max})$, with $F_{max} = 1/\tau_r$

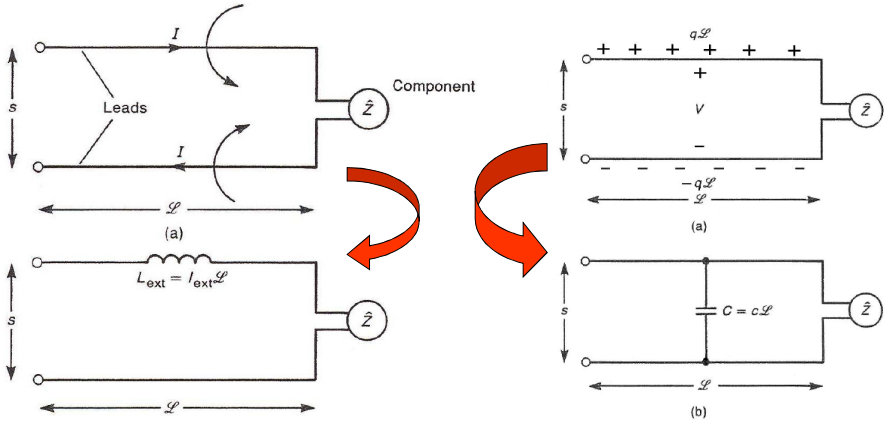
Hence the line and any mismatches should not significantly degrade the output waveform if the pulse rise time is greater than 10 one-way time delays of the line:

$$\tau_r > 10\ T_D$$

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons. 30

Effects of Component Leads: Sections 5.3-5.6

- A component is connected to the circuit via leads (bare wires)
- The high-frequency behavior of components is affected by the length of the leads.
- The length and separation of the leads cause the component to have, in addition to the ideal behavior, an inductive element and a capacitive element.



(a) physical configuration; (b) the equivalent circuit.

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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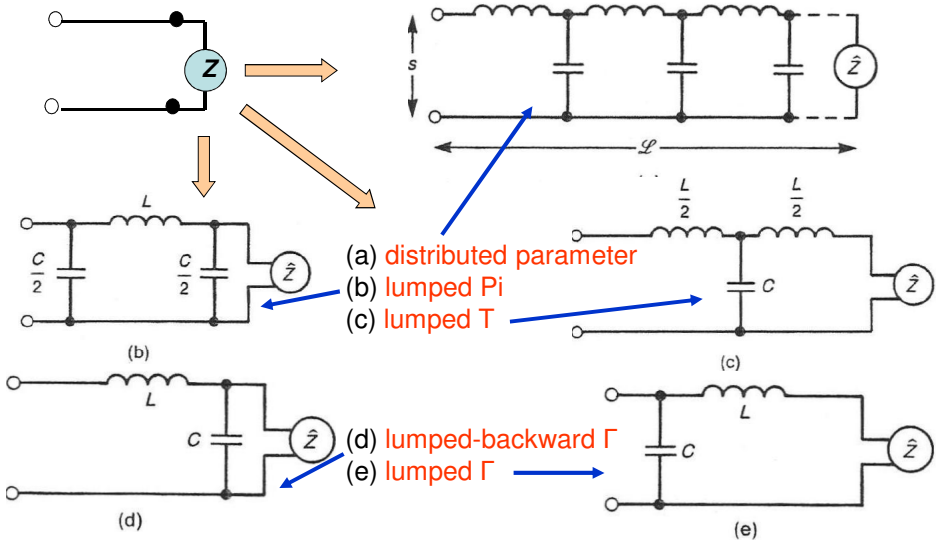
Effects of Component Leads: Equivalent Cct.

Lumped-circuit models are used when the lead length L and separation s are electrically short at the required frequency.



Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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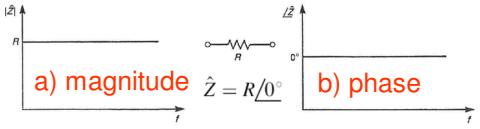
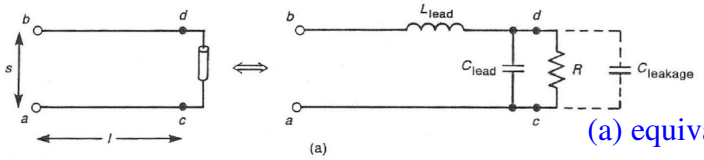
Effects of Component Leads: Resistors (5.4)

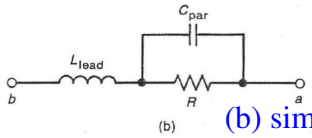
Frequency behavior of the impedance of an ideal resistor:



Non-ideal resistor:



(a) equivalent circuit



(b) simplified equivalent circuit.

The non-ideal resistor including the effects of the leads:

$$\hat{Z}(j\omega) = L_{lead}\frac{1/L_{lead}C_{par} - \omega^2 + j\omega/RC_{par}}{j\omega + 1/RC_{par}}$$

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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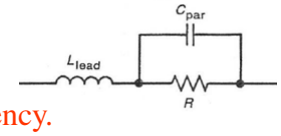
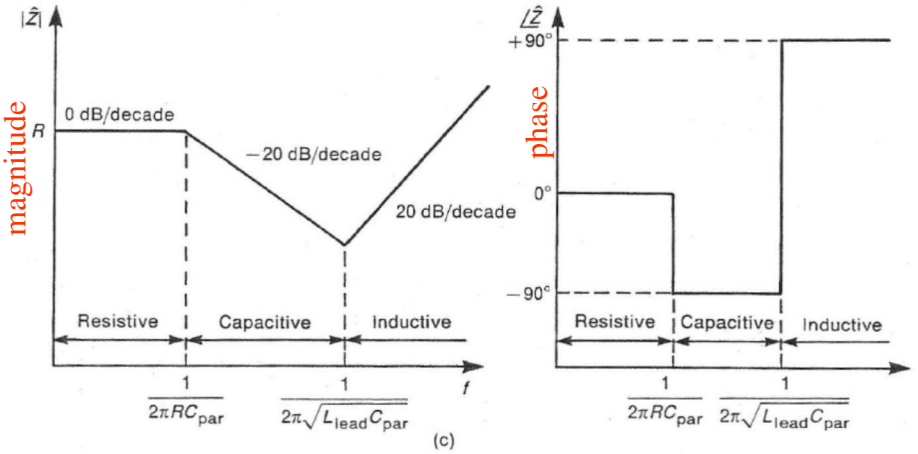
Effects of Component Leads: Resistors

Bode Plot: is a plot of magnitude and phase of a function vs frequency and typically employs log scales.



The non-ideal resistor:

Bode plots of the impedance variation with frequency.



Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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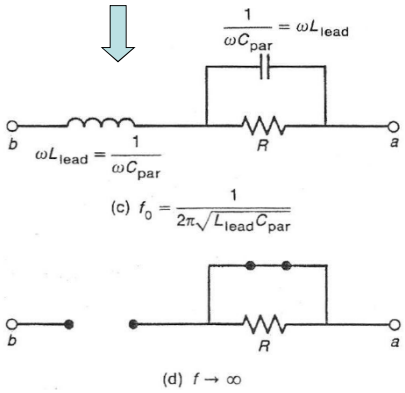
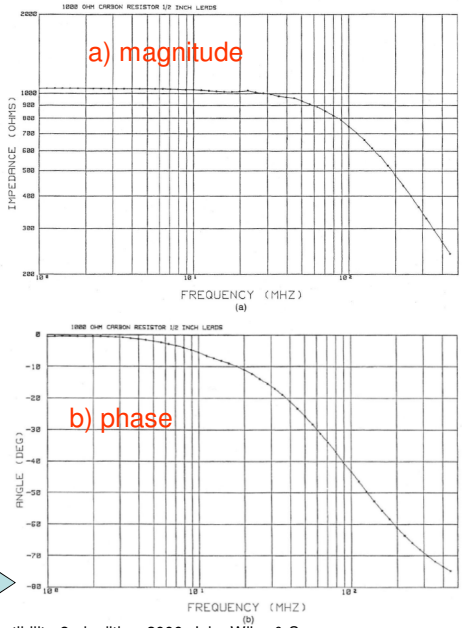
Effects of Component Leads: Resistors

Equivalent circuit of a resistor for various frequencies:





Measured impedance of a 1000-Ω carbon resistor having ½ in. lead lengths: (a) magnitude (b) phase

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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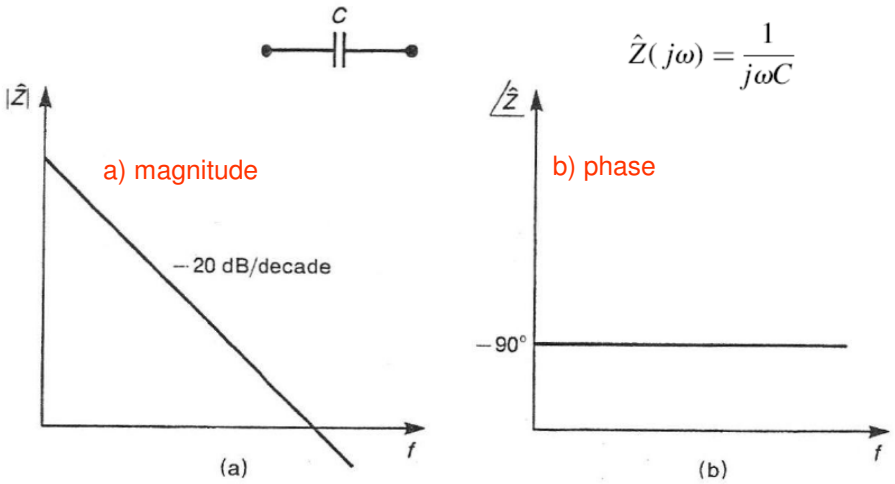
Effects of Component Leads: Capacitors (5.5)



Frequency response of the impedance of an ideal capacitor: (a) magnitude; (b) phase.

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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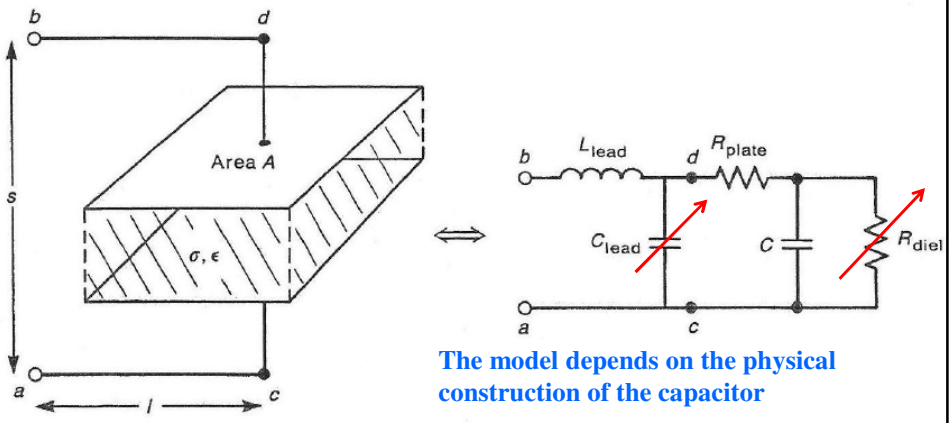
Effects of Component Leads: Capacitors



The model depends on the physical construction of the capacitor

Typically R_{diel} is very large & $C >> C_{lead}$

Modeling of a physical capacitor with an equivalent circuit.

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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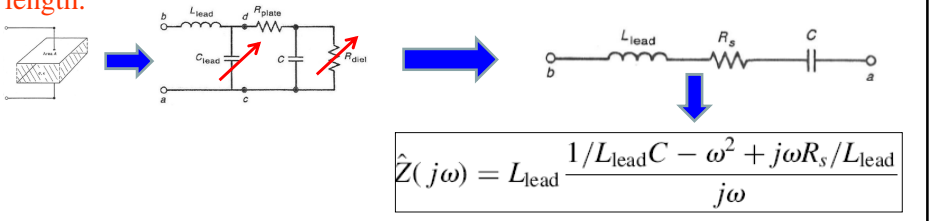
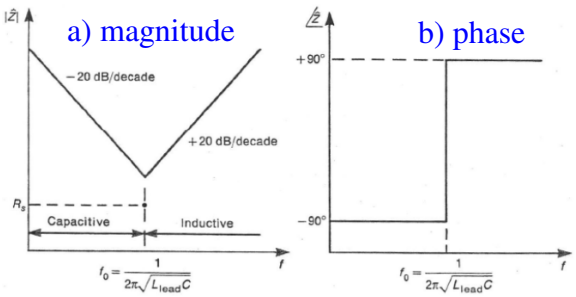
Effects of Component Leads: Capacitors

A simplified equivalent circuit of a capacitor including the effects of lead length.



$$\hat{Z}(j\omega) = L_{lead}\frac{1/L_{lead}C - \omega^2 + j\omega R_s/L_{lead}}{j\omega}$$

Bode plots of the impedance: (a) magnitude; (b) phase.



Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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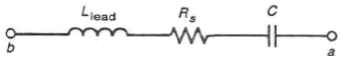
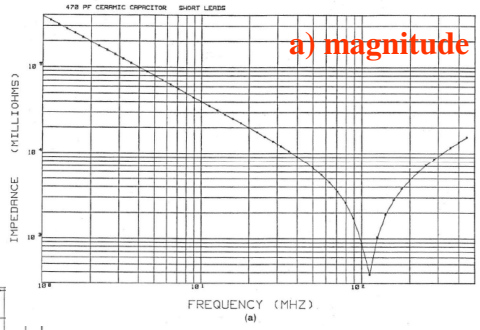
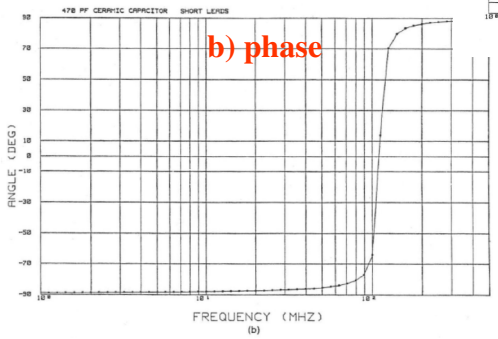
Effects of Component Leads: Capacitors

Measured impedance of a 470-pF ceramic capacitor with short lead lengths:





a) magnitude



b) phase

Note the self resonant frequency (pure resistive impedance)

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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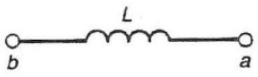
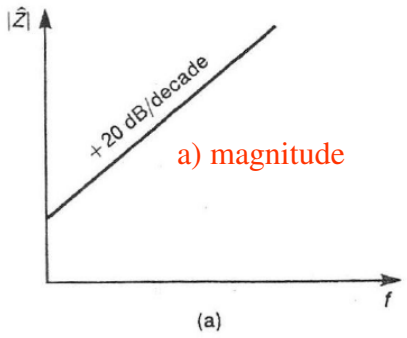
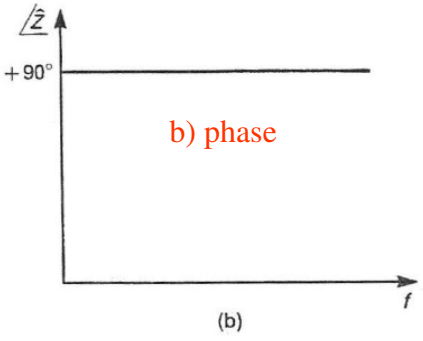
Effects of Component Leads: Inductors (5.6)



$$\hat{Z}_L = j\omega L$$



a) magnitude



b) phase

Frequency response of the impedance of an ideal inductor: (a) magnitude; (b) phase.

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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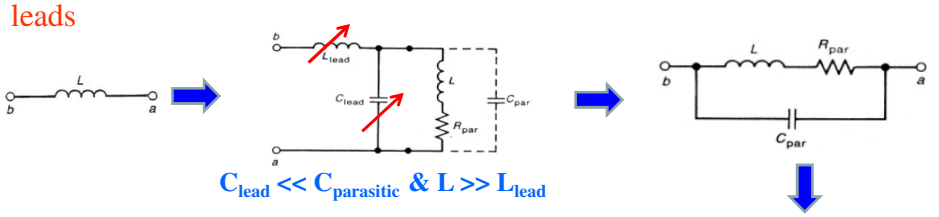
Effects of Component Leads: Inductors

A simplified equivalent circuit of an inductor including the effects of leads

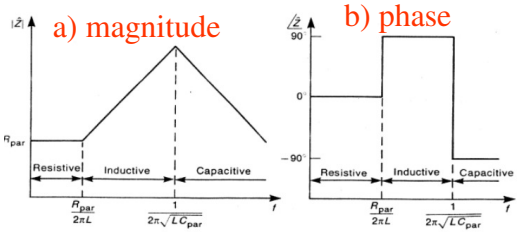


$C_{lead} << C_{parasitic}$ & $L >> L_{lead}$

The model depends on the physical construction of the inductor.

$$\hat{Z}_L(j\omega) = R_{par}\frac{1 + j\omega L/R_{par}}{1 - \omega^2 LC_{par} + j\omega R_{par}C_{par}}$$

Bode plots of the impedance:



Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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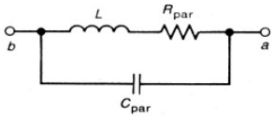
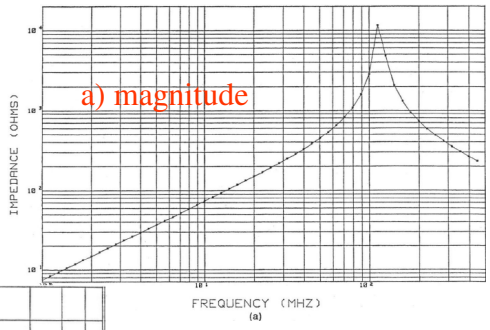
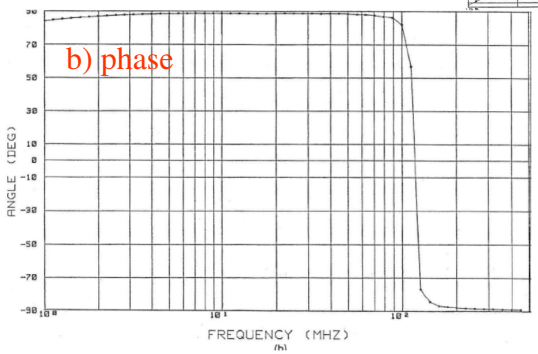
Effects of Component Leads: Inductors

Measured impedance of a 1.2 μ H inductor:







Note the self resonant frequency (pure resistive impedance)

Source: P.R. Clayton: Introduction to Electromagnetic Compatibility, 2nd edition, 2006, John Wiley & Sons.

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P5.4.1.

The magnitude of an impedance is sketched as a Bode plot

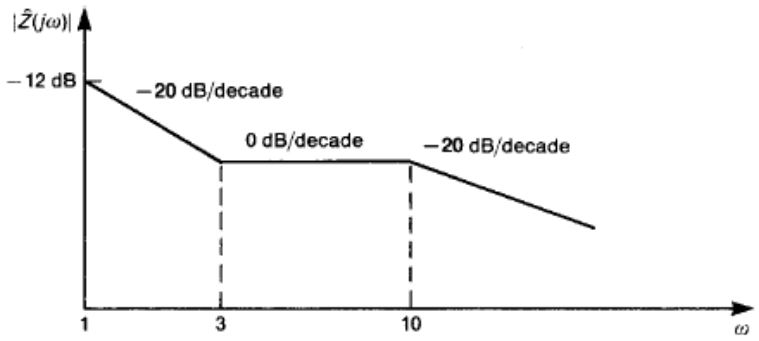

FIGURE P5.4.1

Determine one possible impedance expression for this.

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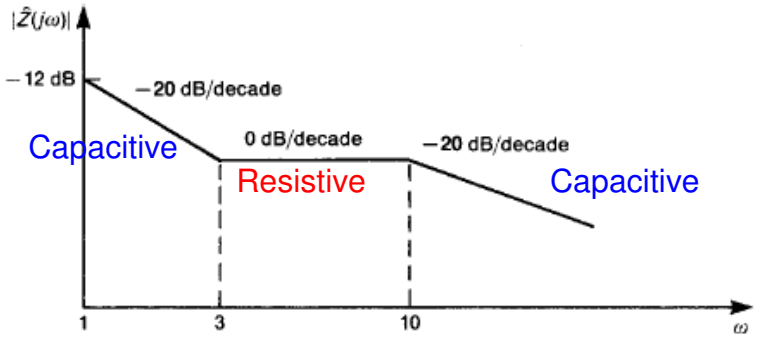
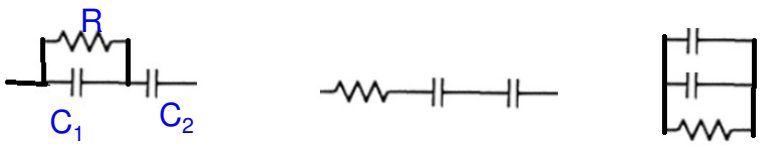


FIGURE P5.4.1

From the Bode plot
Circuit has 2 Cs and 1 R

Three possible configurations:



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