

Lab Experiment 2

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CEG 2136
Oct 2nd 2014

Design and Simulation of Sequential Logic Circuits

Purpose:

The main purpose of this is the introduction of the design of sequential circuits based on Altera's Quartus 2, their implementation and testing.

- Designing of synchronous counter using Quartus 2 graphic editor
- Assigning input-output pins and to download it on the Altera UP2 board for testing
- Testing and Simulating the counter
 - Simulating and confirming the correct outputs of counter
 - To display outputs of counters on Oscilloscope and Altera board using LEDs

Equipment and Supplies:

The equipment used during the lab is following:

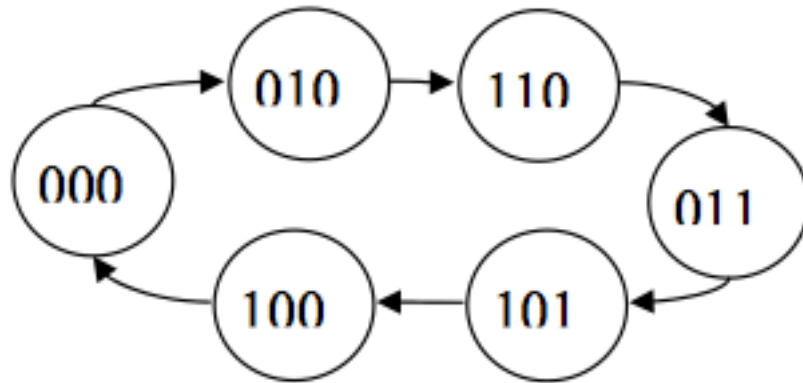
- Quartus 2
- Altera UP2 Board
 - Byte Blaster Cable
 - EMP7128S CLPD
 - Power Supply
- Wires to connect the LEDs
- Wire Stripper

Part A (Simulation)

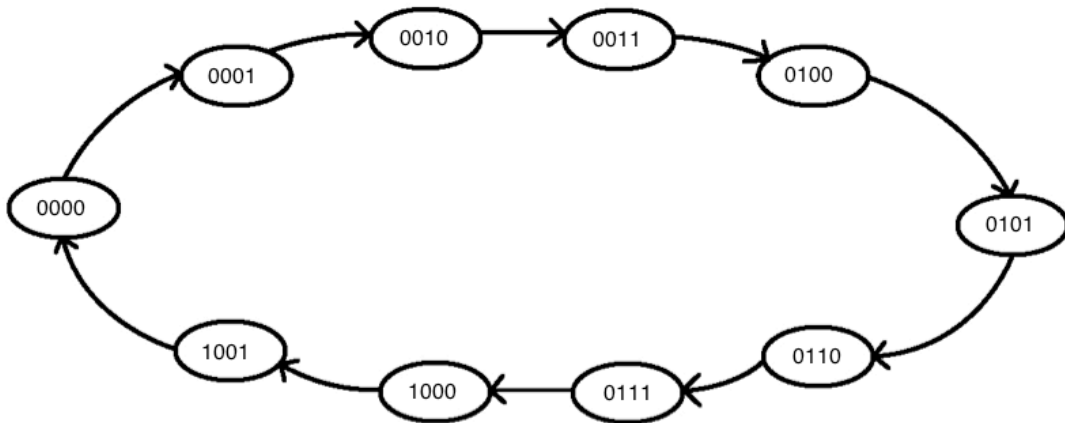
The Objective in this part of the lab is to design and simulate a 3-bit Synchronous modulo 6 counter and 4-bit Synchronous BCD counter that follows the given binary sequence in the lab manual. These binary counters are to be designed using JK Flip-Flops.

State Diagram

a) 3-bit Synchronous modulo 6 counter



b) 4-bit Synchronous BCD counter



State Table:

a) 3-bit Synchronous modulo 6 counter

Present State	Next State	Flip-Flops (Synchronous Inputs)		
		$Q_2Q_1Q_0$	$Q_2Q_1Q_0$	J K
000	010	0 X	1	0 X
001	XXX	X X	X X	X X
010	110	1 X	X 0	0 X
011	101	1 X	X 1	X 0
100	000	X 1	0 X	0 X
101	100	X 0	0 X	X 1
110	011	X 1	X 0	1 X
111	XXX	X X	X X	X X

b) 4-bit Synchronous BCD counter

Present State	Next State				Flip-flops inputs							
	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0 0 0 0	0	0	0	1	0	X	0	X	0	X	1	X
0 0 0 1	0	0	1	0	0	X	1	X	1	X	X	1
0 0 1 0	0	0	1	1	0	X	X	0	X	0	1	X
0 0 1 1	0	1	0	0	1	X	X	1	X	1	X	1
0 1 0 0	0	1	0	1	X	0	0	X	0	X	1	X
0 1 0 1	0	1	1	0	X	0	1	X	1	X	X	1
0 1 1 0	0	1	1	1	X	0	X	0	X	0	1	X
0 1 1 1	1	0	0	0	X	1	X	1	X	1	X	1
1 0 0 0	1	0	0	1	0	X	0	X	0	X	1	X
1 0 0 1	0	0	0	0	0	X	0	X	0	X	X	1

K-Maps:

a) 3-bit Synchronous modulo 6 counter

A

Q_2

	$Q_1 Q_0$	Q_1	
	00	01	11
0	0	x	1
1	x	x	x

Q_0

$J_2 = Q_1 \bar{Q}_0$

	$Q_1 Q_0$	Q_1	
	00	01	11
0	1	x	x
1	0	0	x

Q_0

$\bar{J}_1 = \bar{Q}_2$

	$Q_1 Q_0$	Q_1	
	00	01	11
0	0	x	0
1	0	x	1

Q_0

$\bar{J}_0 = Q_1 Q_2$

Q_2

	$Q_1 Q_0$	Q_1	
	00	01	11
0	x	x	x
1	0	x	1

Q_0

$K_2 = \bar{Q}_0$

	$Q_1 Q_0$	Q_1	
	00	01	11
0	x	x	0
1	x	x	0

Q_0

$K_1 = Q_0 Q_1$

	$Q_1 Q_0$	Q_1	
	00	01	11
0	x	x	0
1	x	1	x

Q_0

$K_0 = Q_2$

b) 4-bit Synchronous BCD counter

Handwritten Karnaugh maps and equations for a 4-bit Synchronous BCD counter. The maps are arranged in a 2x2 grid, with equations written below each map.

Top-Left Map (Q₁):

0	0	1	0
x	x	x	x
x	x	x	x
0	0	x	x

Equation: $J_2 = Q_1 Q_0$ ✓

Top-Right Map (Q₂):

x	x	x	x
0	0	1	0
x	x	x	x
x	x	x	x

Equation: $K_2 = Q_1 Q_0$ ✓

Bottom-Left Map (Q₃):

0	1	x	x
0	1	x	x
x	x	x	x
0	0	x	x

Equation: $J_1 = Q_0 Q_3$ ✓

Bottom-Right Map (Q₀):

x	x	1	0
x	x	1	0
x	x	x	x
x	x	x	x

Equation: $K_0 = Q_0$ ✓

Bottom-Left Map (Q₀):

1	x	x	1
1	x	x	1
x	x	x	x
1	x	x	x

Equation: $J_0 = 1$ ✓

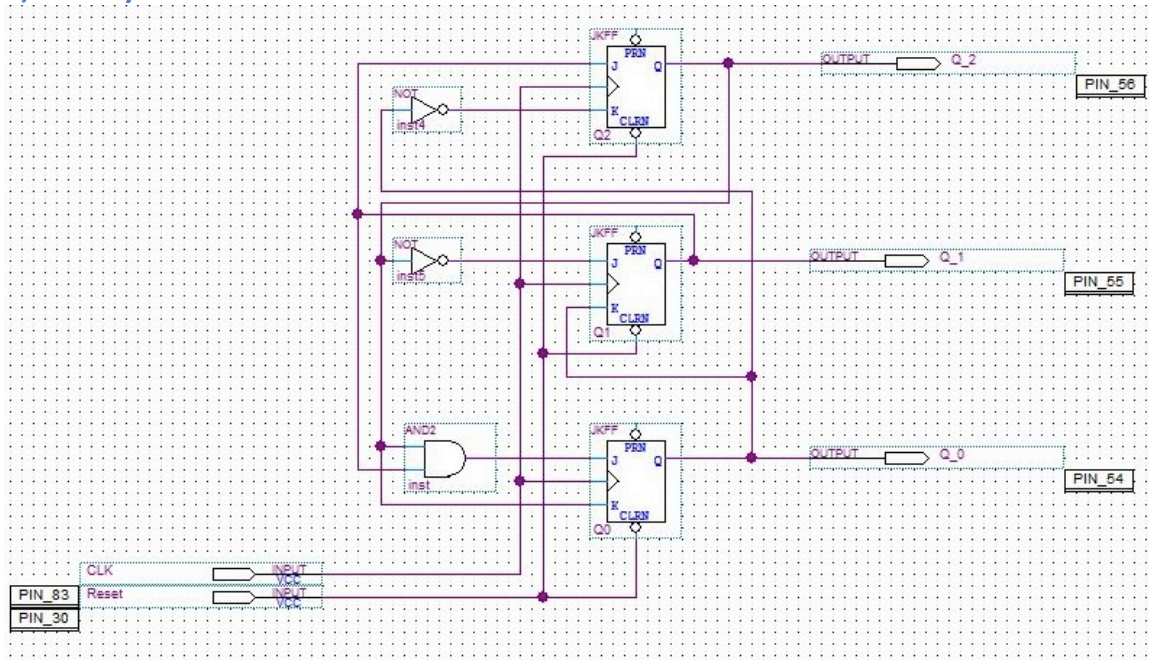
Bottom-Right Map (Q₀):

x	1	1	x
x	1	1	x
x	x	x	x
x	1	x	x

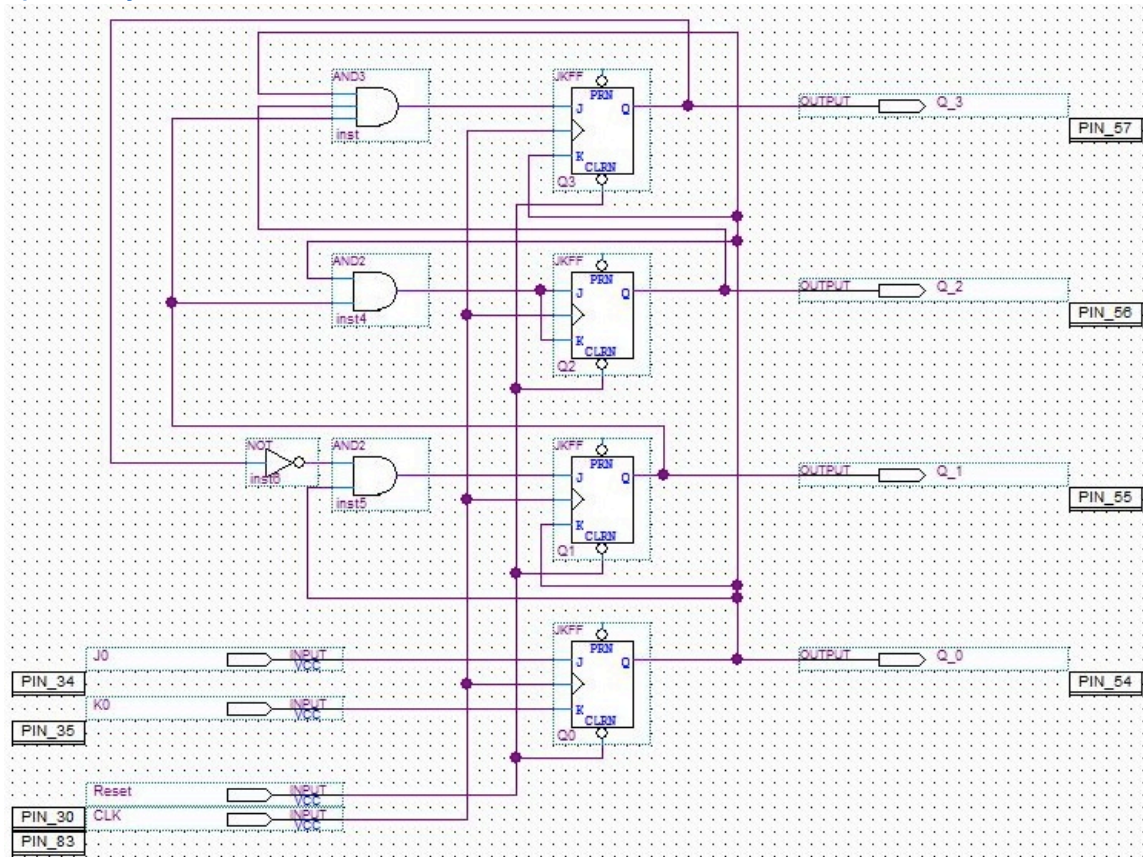
Equation: $K_0 = 1$ ✓

Circuit Diagram:

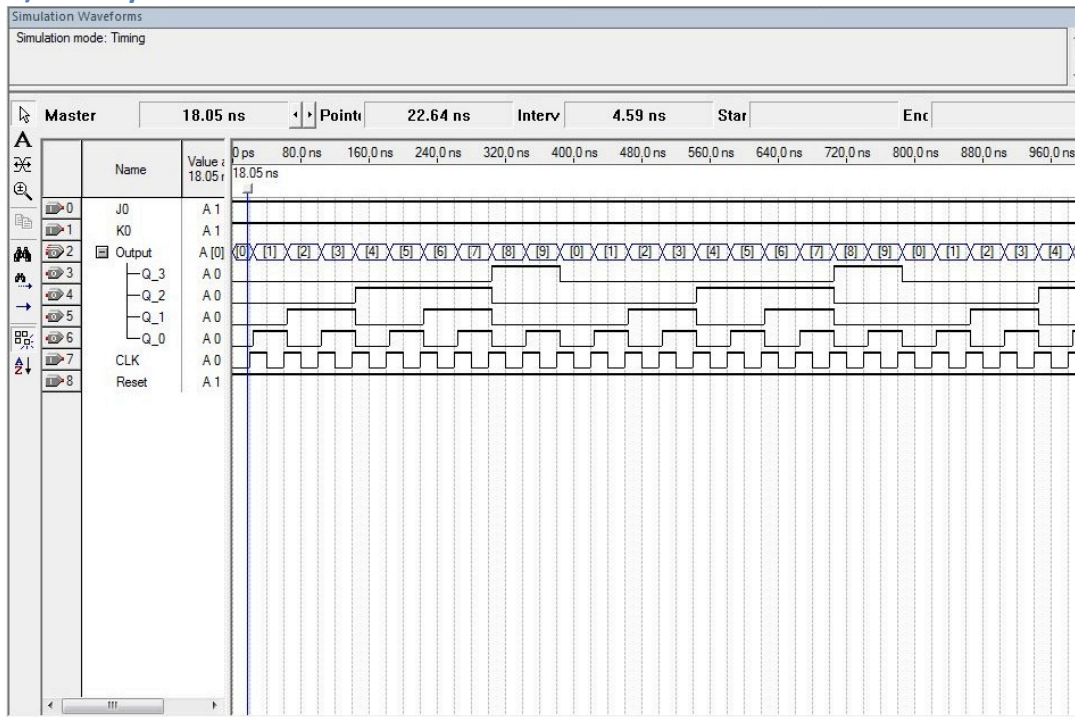
a) 3-bit Synchronous modulo 6 counter



b) 4-bit Synchronous BCD counter



b) 4-bit Synchronous BCD counter



Flow Summary	
Flow Status	Successful - Tue Sep 23 17:09:05 2014
Quartus II Version	9.0 Build 235 06/17/2009 SP 2 SJ Web Edition
Revision Name	Lab2
Top-level Entity Name	Lab2
Family	MAX7000S
Device	EPM7128SLC84-7
Timing Models	Final
Met timing requirements	Yes
Total macrocells	4 / 128 (3 %)
Total pins	12 / 68 (18 %)

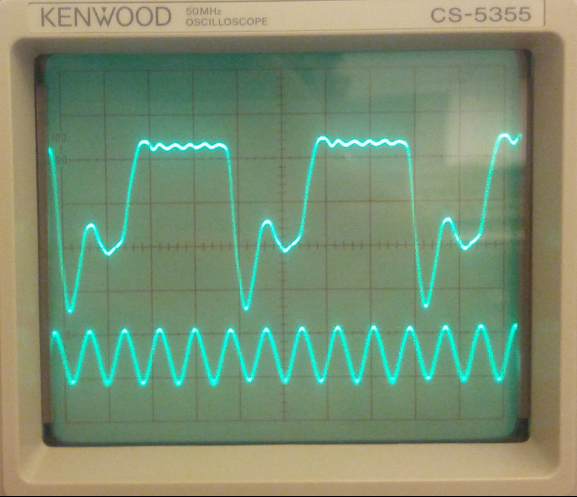
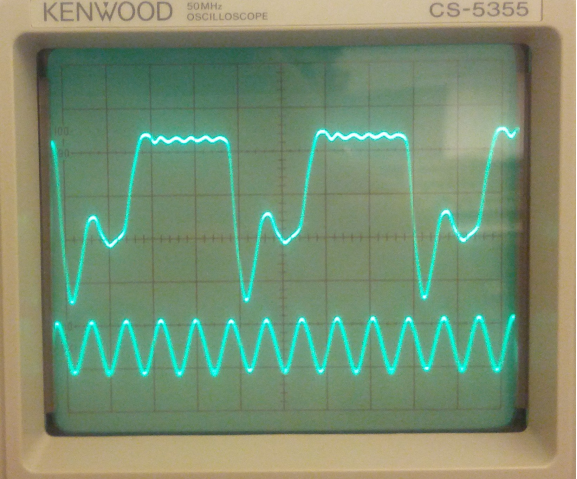
Part A (Conclusion):

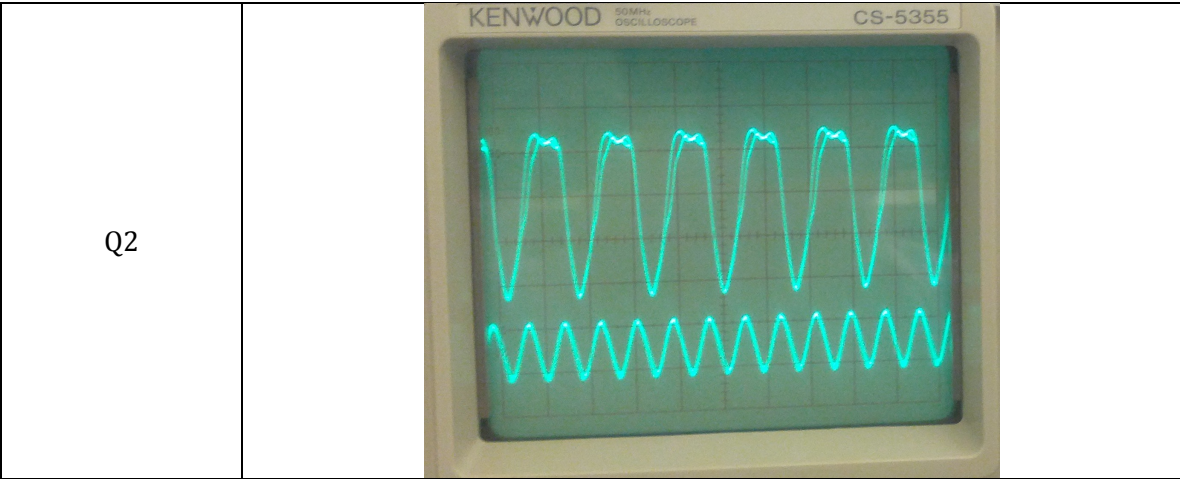
The 3-bit Synchronous modulo 6 counter and 4-bit Synchronous BCD counter was successfully compiled and simulated. Therefore the Objectives of lab's Part A were successfully achieved.

Part B (Testing)

a) Automatic free running counter

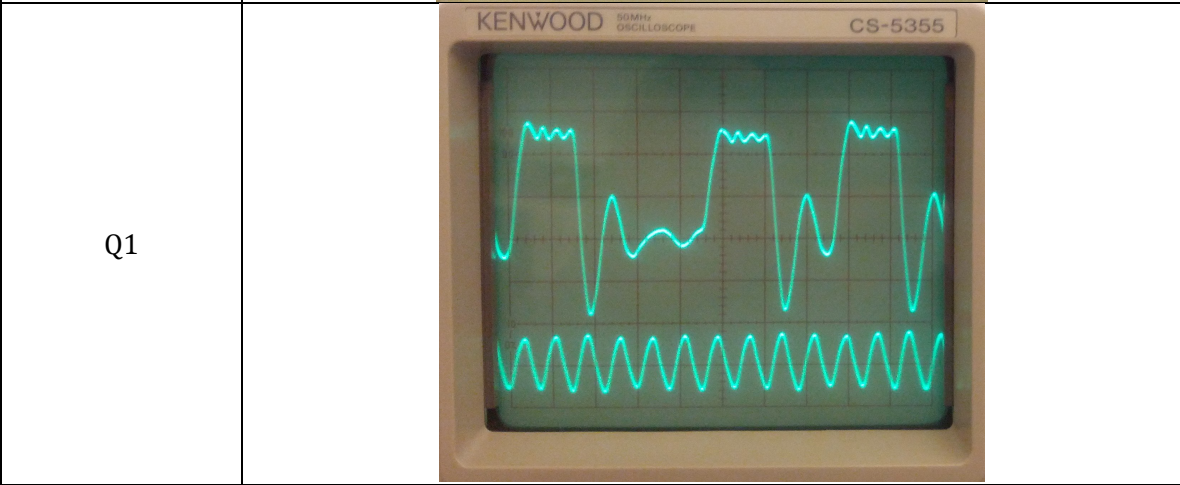
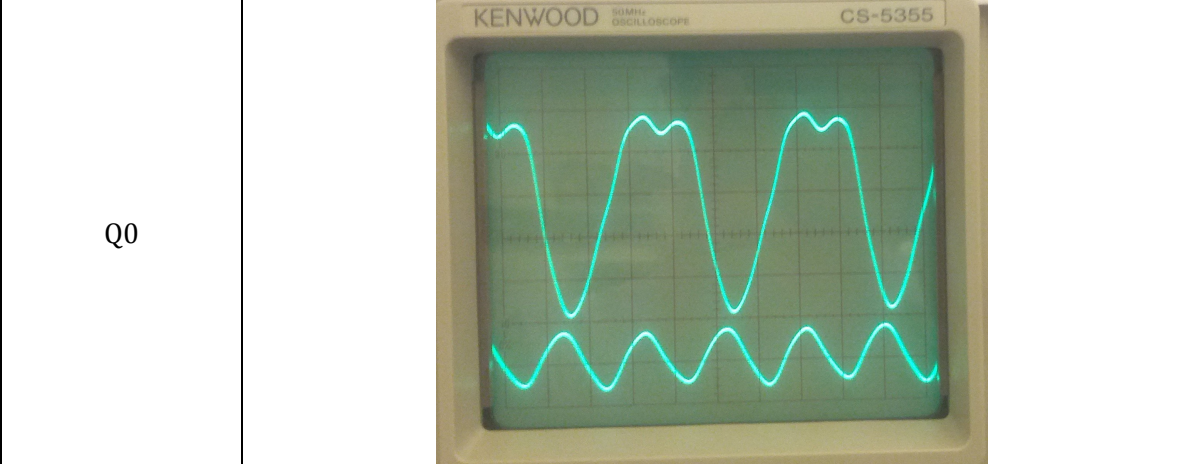
In this method the counter clock is connect to the General Clock (GCLK1) and the signal to the counter clock is generated automatically. In the outputs of the counters are observed with the help of oscilloscope because of the General Clock running at very high speeds.

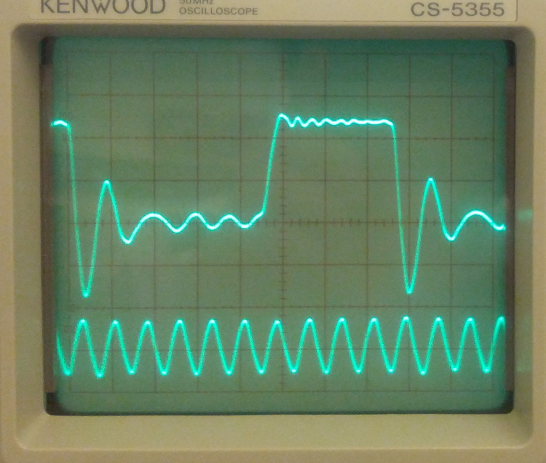
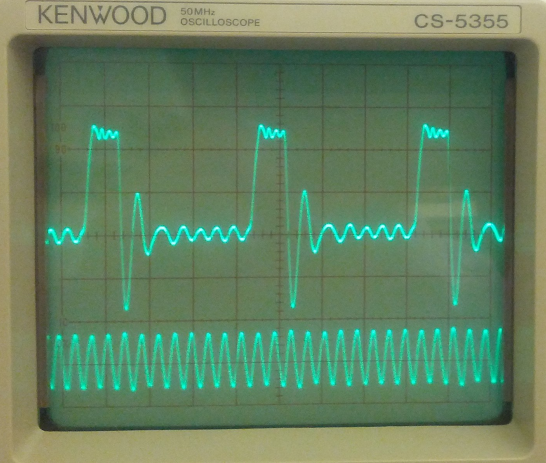
3-bit Synchronous modulo 6 counter	
Outputs	Oscilloscope
Q0	
Q1	



4-bit Synchronous BCD counter

Outputs	Oscilloscope
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Q2			
Q3			

b) Manual Control

In this method the clock of the system was simulated using a push button on the Altera UP2 board. Each time the button is pushed the counter goes from the present state to the next state. The outputs of the counters were displayed on the LEDs present on the Altera UP2 board. This test was successful completed and all the result matched the state diagram.

Discussion:

The circuits were designed according to the formulas that were obtained from the K-maps. Both compiled and simulated successfully. Then, the circuits were downloaded to the Altera UP2 board and tested them. The results were exactly the same as the theoretical results obtained in the pre-lab.