Université d'Ottawa
Faculté de génie

École de science informatique
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uOttawa
L'Université canadienne
Canada's university

University of Ottawa
Faculty of Engineering

School of Electrical Engineering
and Computer Science

CEG2136: Computer Architecture I
CEG2536: Architecture des Ordinateurs I

Duration: 1 hour and 30 minutes

- Closed book exam. All electronic devices including calculators are not allowed.
- If in doubt how to interpret a question, make an assumption and elaborate your solution based on this hypothesis. Explain all your assumptions and well define the symbols used.
- If you finish 10 minutes or less before the due time, remain seated until the end of the exam.

Question 1

1.1 (12 x 1.5 point)

Fill out each row of the following table with the corresponding representation in other bases of the number given in that row; show the details of your calculations**.**

decimal	binary	hexadecimal	octal
25.5			
	1010.01		
		1A	
			32

1.2 (4 points)

In the 8-bit signed 2's complement representation, the number of distinct numbers is:

(a) 256
(b) 128
(c) 255
(d) None of these

1.3 (6+6+8 = 20 points)

7-bit registers are used in this question to store numbers expressed in 2's complement representation.

(a) Convert the following two signed numbers to binary observing the above assumption:

$A = (-31)_{10}$

$B = (+63)_{10}$

(b) Find the 2's complement of the signed binary numbers A and B, and give your results in decimal, too:

(c) Perform the following arithmetic operations in signed-2's complement representation, using a 7-bit ALU; show operations and results (including intermediary steps), both in binary and in decimal. Are there any overflows? How can a computer detect overflow?

$(+63)_{10} + (-31)_{10}$

$(-63)_{10} - (-31)_{10}$

Are there any overflows? How can a computer detect overflow?

Question 2

2.1 (4x1.5 point)

You have a SRAM memory chip with a capacity of 8k x 4

a) How many input-output data lines does it have?

Answer a) .....

b) How many address lines does it have?

Answer b) .....

c) What is its capacity expressed in "*bit*s"?

Answer c) .....

2.2 (2x6 = 12 points)

What is wrong with the following transfer statements (RTL)?

a) xT: AR ← AR', AR ← 0

b) yT: PC ← AR, PC ← PC + 1

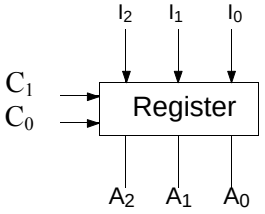
Question 3 (20 points)

Design a 3-bit multi-function register A ($A_2A_1A_0$) whose operation is described in the following table, where C_1 and C_0 are two control bits.

Use in your design JK flip flops, logic gates and any digital components (encoders, decoders, multiplexers, etc.); draw a detailed diagram of the logic circuit of the multi-function register.

Function table of 3-bit register A.

Clock	C_1	C_0	Operation
↑	0	0	No change
↑	0	1	Increment by 3
↑	1	0	Decrement by 3
↑	1	1	Loading external inputs, say I_2 I_1 I_0



Question 4 (20 points)

Design a 4-bit arithmetic circuit, with two selection variables *x* and *y*; the 1-bit variable *z* is an input of full adder. The circuit generates the following eight arithmetic operations under control of *x*, *y* and *z*:
(Note: *X*' is the 1's complement of *X*)

x y	***z* = 0**	***z* = 1**
0 0	F = A+B (add)	F = A+B+1
0 1	F = A (transfer)	F = A+1 (increment)
1 0	F = B' (complement)	F = B'+1 (negate)
1 1	F = A+B'	F = A-B (subtract)

Draw the logic diagram of the two least significant bits of your arithmetic circuit, *only*.
Use full adders and other logic circuits (multiplexer, gates) as required.