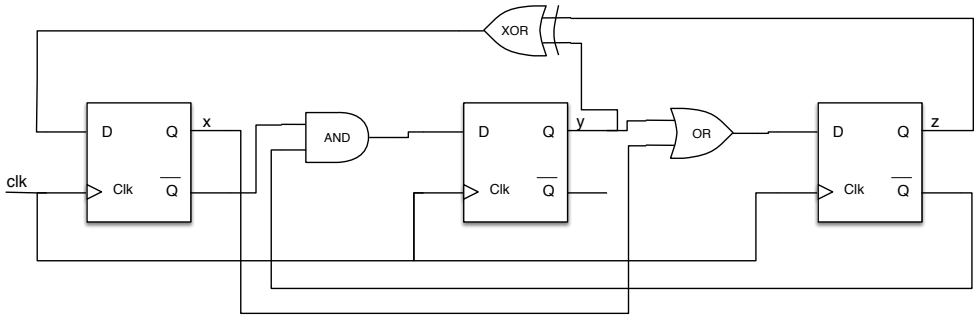
ELEC 2607 ('14) **Assignment 3** 10 Marks

1. Plot the timing diagram for the following circuit for 6 clk cycles. Assume that initially xyz=000. Plot the clk, x, y, and z signals. 2 marks



2. Design a circuit made of rising-edge-triggered flip-flops and inverter(s) such that its output has one-sixth (1/6) of the clock frequency. Verify your design by a timing diagram. The timing diagram should include the clk signal and the outputs of the flip-flops and logic gates. 2 marks

3. Design a circuit that outputs prime numbers between 0 and 10 in ascending order and repeats. Try to use the minimum number of flip-flops possible in your design. Show your state-graph, state-table, next-state and output equations, and the final circuit. 4 marks

4. Design and draw the state-graph of an FSM that detects the input sequence '1101' including overlaps. The sequence appears at the input from left to right. The output becomes 1 as soon as the final bit in the sequence starts. It is not necessary to show the state-table, K-Maps or the circuit. 2 marks