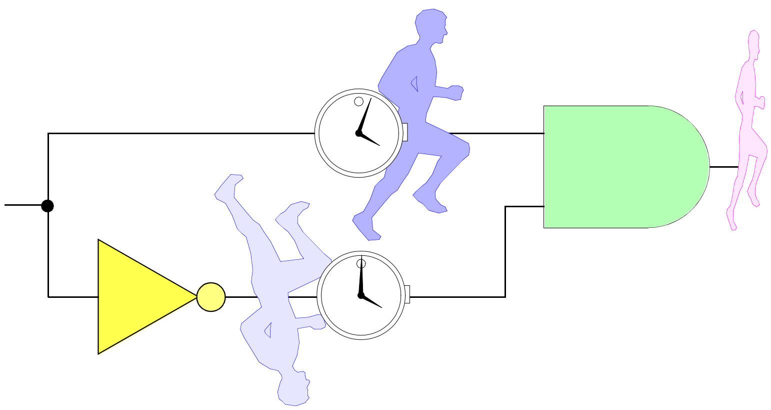
Glitches and Hazards in Digital Circuits



"*After a moment you change your mind*"

Hazards

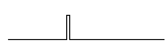
Glitches and a Hazards

A *glitch* is a fast "spike" usually unwanted

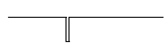
A *hazard* is a circuit which may produce a glitch.
We will see this happens if the propagation delays are unbalanced.

The Classification of Hazards by the Glitch They May Produce

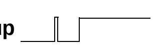
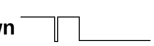
***static-zero hazard*;**

signal is static at zero, glitch rises. 

***static-one hazard*;**

signal is one, glitch falls. 

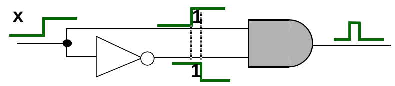
***dynamic hazard*;**

signal is changing, up  **or down** 

The Two Basic Static-Hazard Circuits

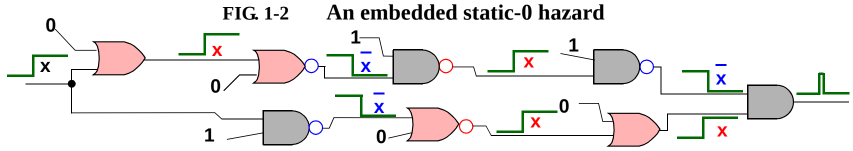
Basic Static-Zero Hazard Circuit

FIG. 1-1 Basic static-0



Any circuit with a static-0 hazard must reduce to the equivalent circuit of FIG. 1-1, if other variables are set to appropriate constants.

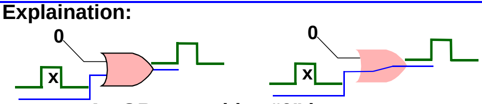
FIG. 1-2 An embedded static-0 hazard



Static-zero Hazard's Characteristics

- Two parallel paths for x.
- One inverted.
- Reconverge at an AND gate.

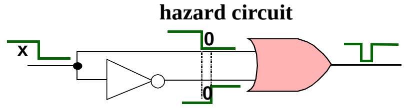
Explaination:



An OR gate with a "0" input passes the other input like a wire

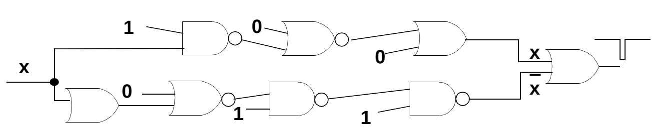
Basic Static-One Hazard Circuit

FIG. 1-3 Basic static-1 hazard circuit



Any circuit with a static-1 hazard must reduce to the equivalent circuit of FIG. 1-3

t FIG. 1-4 An embedded static-1 hazard



Static-One Hazard's Characteristics

- Two parallel paths for x.
- One inverted.
- Reconverge at an OR gate.

The Two Basic Dynamic-Hazard Circuits

Basic Dynamic Hazard Circuits

A static hazard with an extra gate for the static level change.

Three parallel paths, one containing a static hazard.

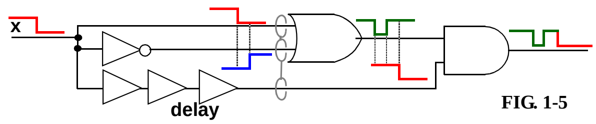


FIG. 1-5 **The basic dynamic hazard circuit with its imbedded static-1 hazard.**

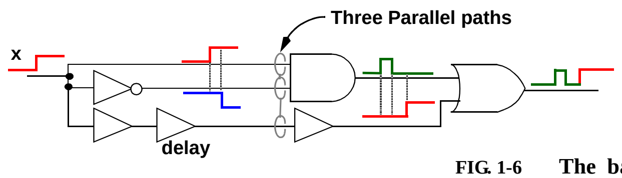


FIG. 1-6 **The basic dynamic hazard circuit with its imbedded static-0 hazard.**

Note that a dynamic hazard always has three parallel paths.

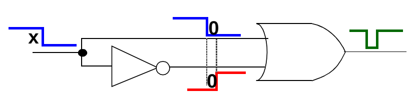
Glitches and Hazards in Digital Circuits ■ The Two Basic Dynamic-Hazard Circuits

Adding Delay to Hazards

Adding delay can remove hazards, if one has good control of propagation delays.

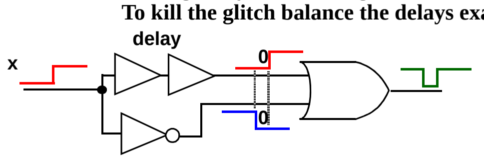
The original circuit with the delay in the inverter.

FIG. 1-7 **Basic static-1 hazard circuit from FIG. 1-3. Note the hazard appears on the falling edge of x.**



- **Adding an equal delay in the other path removes the falling-edge glitch.**
- **Adding too much delay will make the glitch appear on the rising edge.**

FIG. 1-8 **Adding delay, moves the glitch from x to x. To kill the glitch balance the delays exactly, if you can!**

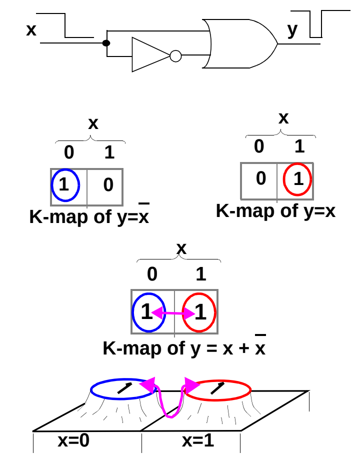


At the silicon layout level, one might balance delays closely enough to suppress the glitch.
With standard cells and field-programmable arrays, balancing is harder.

But see "Summary Of Hazards" on page 39.

Hazards on a Karnaugh Map

Adjacent but nonoverlapping circles on the map are hazards.



An interpretation of the K-map of y.

FIG. 1-9

Map of a static-1 hazard.
On the Σ of Π map, each OR gate input is a separate circle.

Standing on top of a hill gives a "1." Changing hills causes a "0" glitch as one crosses the valley.

The ↔ shows the hazard.

A Static-1 Hazards on a Map

Σ of Π maps can only show static-1 hazards, not static-0 or dynamic hazard.

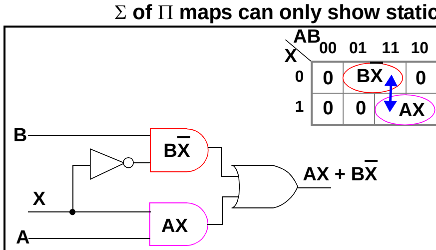


FIG. 1-10

AND gates have been added to the hazard.

The hazard is still the inverter and the OR gate.

The hazard appears only when A = 1, B = 1.

Then signal X travels right through the ANDs.

Masking a Hazard.

To mask static-1 hazards add a gate that stays high across the ↔ transition. This gate is logically redundant.

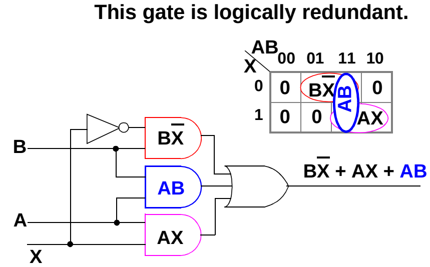


FIG. 1-11

The equation
$F = B\overline{X} + AX$
has redundant term AB added
$F = B\overline{X} + AX + AB$
This fills the valley between terms $B\overline{X}$ and AX.

DeMorgan's General Theorem (Review)

Simple form of DeMorgan's Theorems

$A\cdot B = \overline{\overline{A}+\overline{B}}$ $\qquad \overline{A\cdot B} = \overline{A}+\overline{B}$ $\qquad \overline{D+E} = \overline{D}\cdot\overline{E}$ $\qquad D+E = \overline{\overline{D}\cdot\overline{E}}$

The general form

$$\overline{F(A,B,C,\ldots+,\cdot)} = F(\overline{A},\overline{B},\overline{C},\ldots,\cdot,+)$$

$$F = [\overline{A}\cdot B\cdot C + D\cdot(A\cdot B+C)]\cdot\overline{A}$$

a) Take the dual of F

i) Bracket all groups of ANDs

$$F = \{[\{\overline{A}\cdot B\cdot C\}+\{D\cdot(\{A\cdot B\}+C)\}]\cdot\overline{A}\}$$

ii) Change AND to OR and OR to AND

$$F_{DUAL} = \{[\{\overline{A}+B+C\}\cdot\{D+(\{A+B\}\cdot C)\}]+\overline{A}\}$$

Clean brackets

$$F_{DUAL} = \{\overline{A}+B+C\}\cdot\{D+\{A+B\}\cdot C\}+\overline{A}$$

b) Invert all variables

$$\overline{F} = \{A+\overline{B}+\overline{C}\}\cdot\{\overline{D}+\{\overline{A}+\overline{B}\}\cdot\overline{C}\}+A$$

Examples

$F = \overline{A}\cdot B\cdot C$ ⇒	$\{\overline{A}\cdot B\cdot C\}$ ⇒	$\overline{F} = \{A+\overline{B}+\overline{C}\}$
$F = \overline{A}\cdot B\cdot C + A\cdot\overline{B}$ ⇒	$\{\overline{A}\cdot B\cdot C\} + \{A\cdot\overline{B}\}$ ⇒	$\overline{F} = \{A+\overline{B}+\overline{C}\}\cdot\{\overline{A}+B\}$
$F = \overline{A}\cdot B\cdot(C + \overline{A\cdot B})$ ⇒	$\{\overline{A}\cdot B\}\cdot(C+\{\overline{A\cdot B}\})$ ⇒	$\overline{F} = \{A+\overline{B}\}+(\overline{C}\cdot\{\overline{A}+\overline{B}\})$

Getting a Π of Σ Map from an Equation

Take a Π of Σ equation F

$$F = (X + B)\cdot(\overline{X} + A)$$

The Π of Σ map is found by

1. Apply ' to F
   This gives a formula for $\overline{F}$.

$$F = (X + B)\cdot(\overline{X} + A)$$

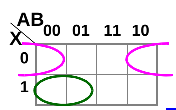
$$F_{DUAL} = (X\cdot B) + (\overline{X}\cdot A)$$

Place bars over single letters

$$\overline{F} = (\overline{X}\cdot\overline{B}) + (X\cdot\overline{A})$$

2. Map $\overline{F}$ on a Karnaugh map
   This is a Σ of Π which is easy to map.

$$\overline{F} = \overline{X}\cdot\overline{B} + X\cdot\overline{A}$$



Σ of Π Map of $\overline{F}$

3. Change this $\overline{F}$ map into a map of F:
   write 0 in the circled squares,
   write 1 in the uncircled squares.

Map of F with "0"s circled.

X \ AB	00	01	11	10
0	0	1	1	0
1	0	0	1	1

Π of Σ map for F

$$F = (X + B)\cdot(\overline{X} + A)$$

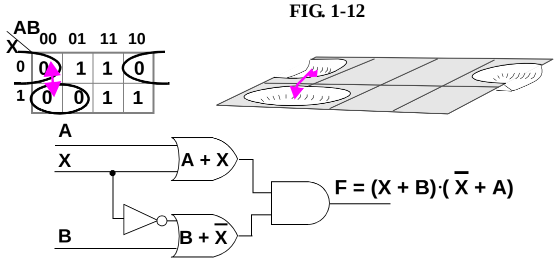
This gives the Π of Σ map for F.

Showing a Static-0 Hazards

Use a Π of Σ Map

Π of Σ maps show static-0 hazards.

FIG. 1-12



Plot Π of Σ map.

$F = (X + B)\cdot(\overline{X} + A)$

$\overline{F} = (\overline{X}\cdot\overline{B}) + (X\cdot\overline{A})$

Circle $\overline{F}$ on map for F.
Circle "0"s, not "1"s.

Gaps between adjacent circles show static-0 hazards.

If the circles overlap, there is no hazard,

The circles have to be adjacent, not corner-to-corner.

Static-0 Hazard with Map Wrap Around

Π of Σ maps show only static-0 hazards, not static-1 or dynamic hazards

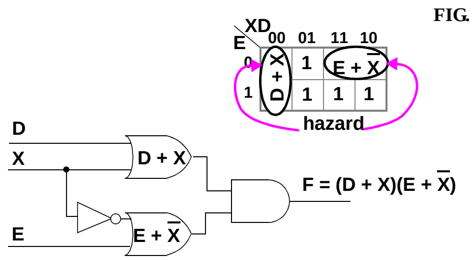


FIG. 1-13

Get Π of Σ map

$F = (D + X)(E + \overline{X})$

$\overline{F} = (\overline{D}\cdot\overline{X})+(\overline{E}\cdot X)$

Circle "0s" not "1s."

Gaps between adjacent circles show static-0 hazards.

Don't forget wrap around

Masking a Static-0 Hazard on a Π of Σ Map

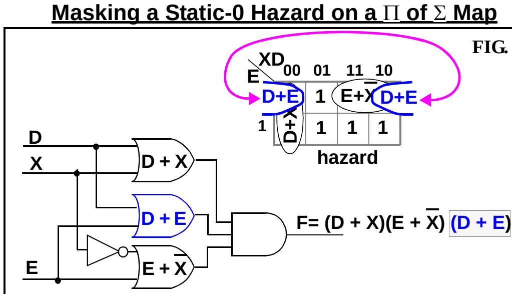


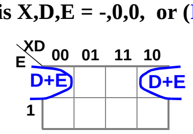
FIG. 1-14

To mask the static-0 hazard:

AND F with a term which stays 0 across the hazard.

The hazard is X,D,E = 1,0,0 to 0,0,0.

The term which stays 0 across the gap is X,D,E = -,0,0, or (D + E).



Algebra and Hazards.

In hazards, delays temporarily make $x = \bar{x}$.
In algebra with hazards, treat x and $\bar{x}$ as separate variables.

For work with hazards, do not use:

Complementing	Absorption	Swap	Consensus
$x\bar{x} = 0$	$x + \bar{x}y = x + y$	$(x + y)(\bar{x} + z) = xz + \bar{x}y$	$xy + yz + \bar{x}z = xy + \bar{x}z$
$x + \bar{x} = 1$	$(\bar{x} + y) = xy$	$xy + \bar{x}z = (x + z)(\bar{x} + y)$	$(x + y)(y + z)(\bar{x} + z) = (x+y)(\bar{x} + z)$
	$\bar{x}y + xy = y$		
	$(\bar{x} + y)(x + y) = y$		

For dynamic hazards:
avoid the distributive laws. (Factoring)
and laws derived from them (Simplification law)

The distributive laws can create dynamic hazards from static hazards, even a masked one.

They will not remove or create *static* hazards.

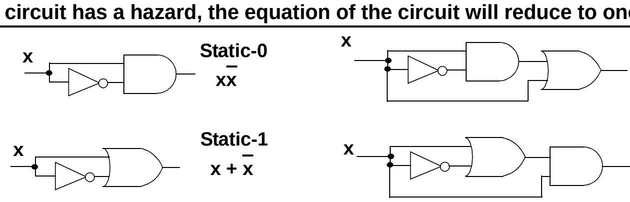
They can be used conditionally if both x and $\bar{x}$ are not included in the operation.

Distributive Laws	Simplification Laws	Derivation of Simplification
$x(y + z) = xy + xz$	$xy + x = x$	$xy + x$
$x + yz = (x + y)(x + z)$	$(x + y)x = x$	$= x(y+1)$ D1
		$= x(1)$
		$= x$

Algebra of Hazards

The basic forms for hazards and their equations.
x and $\bar{x}$ are treated as separate variables.
If a circuit has a hazard, the equation of the circuit will reduce to one of these forms.

FIG. 1-15



An Example

Below, a hazard in x must reduce to a basic hazard circuit when c=1 or when c=0.

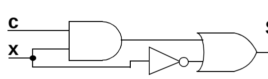


FIG. 1-16 Circuit equation is

$cx + \bar{x}$

when c = 1 get

$1x + \bar{x} = x + \bar{x}$

The hazard is "exposed"

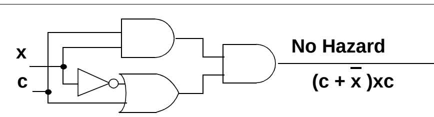


FIG. 1-17 Circuit equation is

$(c + \bar{x})xc$

When c = 1, get $(1 + \bar{x})x1 = x$

When c = 0, get $(0 + \bar{x})x0 = 0$

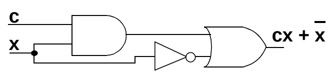
There are no hazard

The Distributive Law and Hazards

The distributive laws can change 2 parallel paths into 3,
this may create a dynamic hazard from a static one.
They can create a dynamic hazard from a masked hazard (FIG. 1-18 bottom).

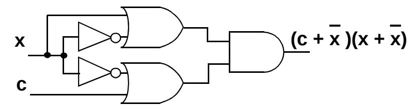
FIG. 1-18 **The distributive law changing static hazards to dynamic hazards.**

ORIGINAL CIRCUIT



Static-1 hazard

CIRCUIT AFTER APPLYING DISTRIBUTIVE LAW II

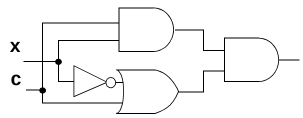


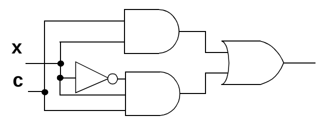
$cx + \overline{x} \;=\; (c + \overline{x})(x + \overline{x})$

When c=1 $x + \overline{x}$ $\quad (1 + \overline{x})(x + \overline{x}) = x + \overline{x}$ Static-1 hazard when c = 1;

When c=0 $\quad (0 + \overline{x})(x + \overline{x}) = \overline{x}(x + \overline{x})$ Dynamic hazard when c = 0

Masked Hazard





$xc(c + \overline{x}) \;=\; xc + xc\overline{x}$

When c=1 $x1(1 + \overline{x}) = x$ $\quad x1 + x1\overline{x} = x + x\overline{x}$ Dynamic hazard when c = 1

DeMorgan's Law Does Not Change Hazards

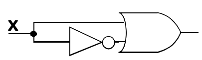
FIG. 1-19 **DeMorgan's Law does not change static hazards or dynamic hazards**

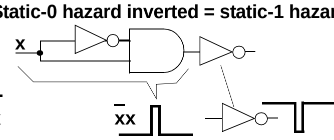
ORIGINAL CIRCUIT

CIRCUIT AFTER APPLYING DEMORGAN'S LAW

Static-1 hazard

Static-0 hazard inverted = static-1 hazard





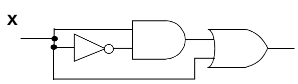
$x + \overline{x} \;=\; \overline{\overline{x}x}$

DeMorgan

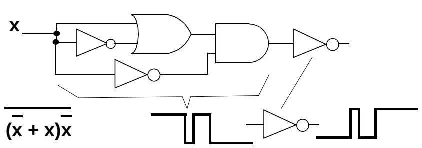
$a + b \;=\; \overline{\overline{a}\cdot\overline{b}}$

$a + \overline{b} \;=\; \overline{\overline{a}\cdot b}$

Dynamic hazard



DeMorgan form of dynamic hazard



$\overline{x}x + x \;=\; \overline{(\overline{x} + x)\overline{x}}$

Algebra and Hazards Summary

In hazards, delays temporarily make x = $\bar{x}$.
With hazards, treat x and $\bar{x}$ as separate variables.

With hazards use only:

Basic

x0 = 0
x + 1 = 1
x + x = x
xx = x

DeMorgan

All forms OK

Distributive

Use only if x and $\bar{x}$ do NOT both appear

x(y + z) = xy + xz OK

~~xc(c + $\bar{x}$) = xc + xc$\bar{x}$~~ NO

Simplification

Use only if x and $\bar{x}$ do NOT both appear

x + Ax = x OK

Let: B = $\bar{x}$ + y
xc + xcB = xc NO

Locating Hazards Algebraically

- This method will find all hazards
  static-1, static-0, and dynamic.
- The circuits do not need to be Σ of Π or Π of Σ like F = (a + b + c$\bar{b}$)de + ($\bar{e}$a + $\bar{d}$b)$\bar{c}$
- It will find all types of hazards on one pass.
- Masking is easier on a map.

Method

Step 1) Remove confusing extended overbars. using DeMorgan.

Step 2) Find which variables cannot have hazards.

Step 3) Reduce expression to standard hazard

Step 4) Select one variable for checking. make other variables 1 or 0 to bring out hazard.

1. $\overline{(A+X)} + \overline{X \cdot C}$
   => $\bar{A}\cdot\bar{X} + (\bar{X} + \bar{C})$

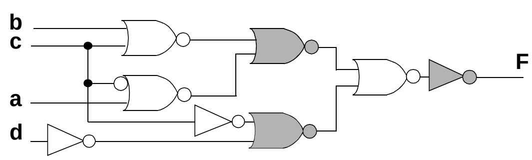
2. Hazards need both X and $\bar{X}$

3. $X\cdot\bar{X}$, $X + \bar{X}$, $X + X\cdot\bar{X}$

4. AX + (B$\bar{X}$ + C)
   Select x for checking
   AX + (B$\bar{X}$ + C)
   Make A=1, B=1, C=0
   1X + (1$\bar{X}$ + 0)
   Static-1 hazard
   X + $\bar{X}$

Example

Find All The Hazards In F.



Method

Step 1) **Remove confusing extended overbars.**

$$\overline{\overline{\overline{\overline{b + c} + \overline{\overline{c} + a}} + \overline{\overline{c} + \overline{d}}}}$$

This is legal because DeMorgan's law does not change hazards

DeMorgan's Laws in Graphical Form (Review)

FIG. 1-20 **Equivalent graphical forms for AND, OR, NAND and NOR.**

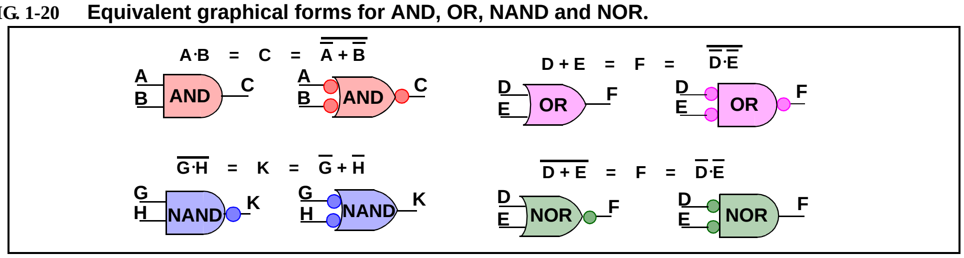
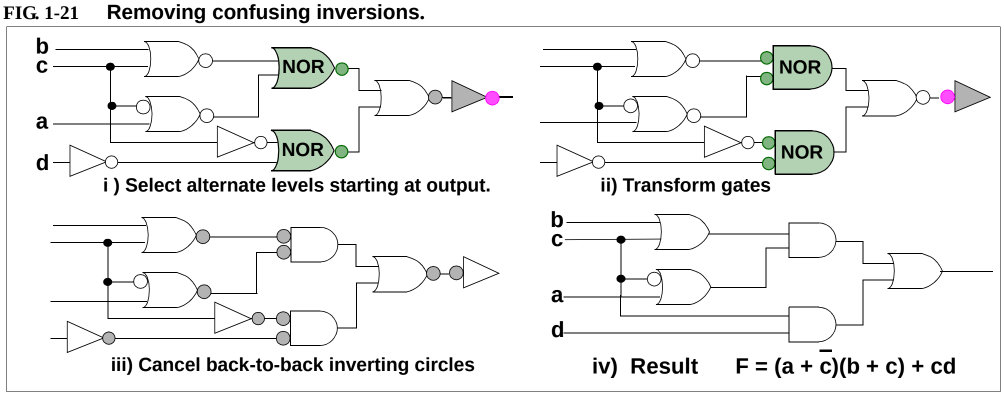


FIG. 1-21 **Removing confusing inversions.**



Step 2. Estimating which variables might have hazards.

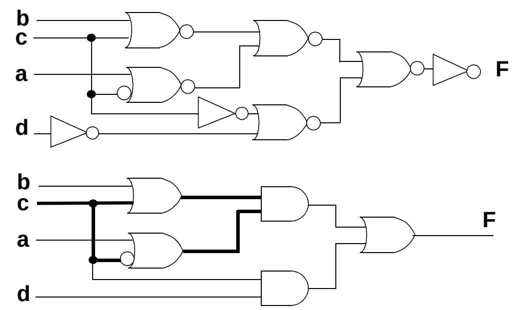
A hazard, has two paths which reconverge in an AND or OR gate.

One path must have an even number of inversions,
and the other path must have an odd number.

One need only check for hazards in variables which have such paths.

Checking a circuit for potentially hazardous paths.

FIG. 1-22 Remove internal inverting circles using DeMorgan's laws.



To see hazardous paths:

Check for reconvergent paths one of which is inverting.

Only variable c has such a path; only c can have hazards.

To check which variables can have hazards.

Check which variables have x and $\bar{x}$

\ Only c has both c and $\bar{c}$ terms.

$F = (a + \bar{c})(b + c) + cd$

Step 3. Locating Hazards From the Circuit Equation

A. Take the circuit equation.

$$F = (a + \bar{c})(b + c) + cd$$

B. Note which variables do not have both $\bar{x}$ and x.
In this case a, b and d. => only c needs to be checked.

C. Substitute 0s and 1s for the other variables. Try to get forms like:

$c\bar{c}$, $c + \bar{c}$, $\bar{c}c + c$, $(c + \bar{c})c$.

a	b	c	d	$(a + \bar{c}) \cdot (b + c) + cd$	F	Type of hazard.
0	0	c	0	$(0 + \bar{c}) \cdot (0 + c) + c0$	$c\bar{c}$	Static-0
0	0	c	1	$(0 + \bar{c}) \cdot (0 + c) + c1$	$\bar{c}c + c$	Dynamic
0	1	c	1	$(0 + \bar{c}) \cdot (1 + c) + c1$	$\bar{c} + c$	Static-1
0	1	c	0	$(0 + \bar{c}) \cdot (1 + c) + c0$	$\bar{c}$	
1	0	c	0	$(1 + \bar{c}) \cdot (0 + c) + c0$	c	
1	0	c	1	$(1 + \bar{c}) \cdot (0 + c) + c1$	c + c	c
1	1	c	1	$(1 + \bar{c}) \cdot (1 + c) + c1$	1 + c	1
1	1	c	0	$(1 + \bar{c}) \cdot (1 + c) + c0$	1	

Static-0 hazard in c when a,b,d = 0,0,0,
Dynamic hazard in c when a,b,d = 0,0,1,
Static-1 hazard in c when a,b,d = 0,1,1.

Same Example With More Organization and Less Writing

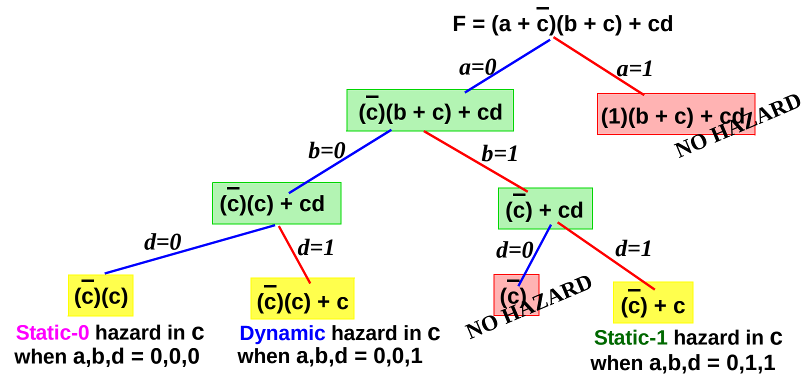
Equation.

$$F = (a + \bar{c})(b + c) + cd$$

Note only c can have a hazard.

Select c to to be the variable that changes.

Sequentially substitute 1 or 0 for the other letters.



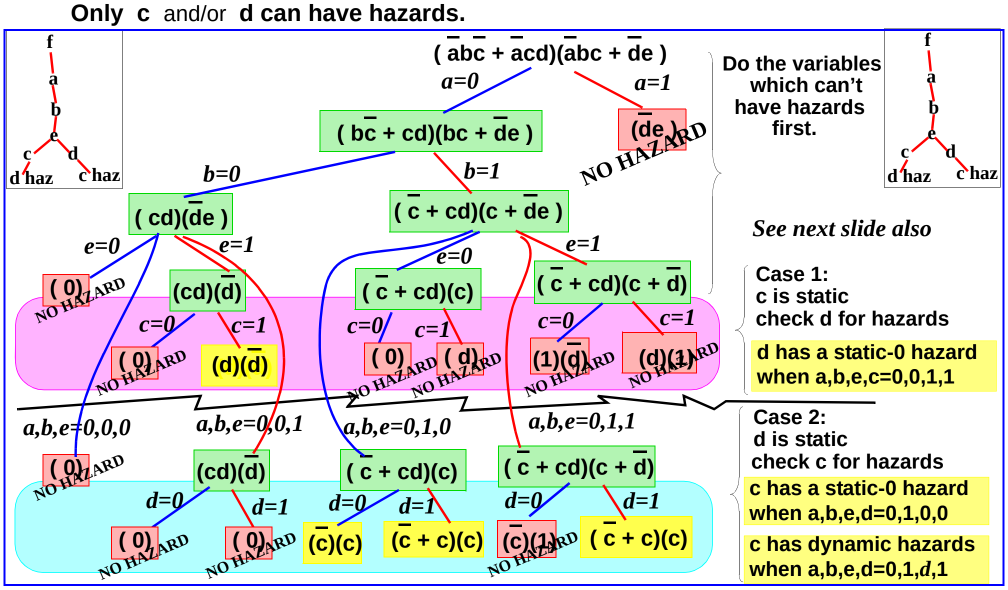
Remember this tree from MUX logic?

Example 2:

Find all the single-variable change hazards

$$f = (\bar{a}b\bar{c} + \bar{a}cd)(\bar{a}bc + \bar{d}e)$$

Only c and/or **d can have hazards.**



Example 2: (Overview)

Avoid duplicating work

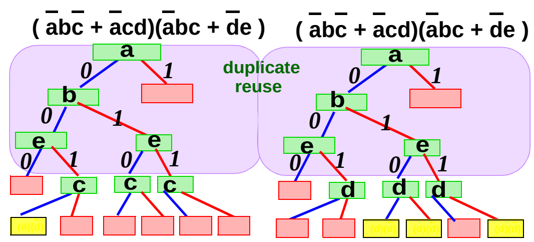
.

$(\bar a \bar b c + \bar a cd)(\bar a bc + \bar d e)$

a can't have hazards
b can't have hazards
e can't have hazards

expand on **a, b** and **e** first
That way you can reuse
your work

Pick **a** first
It occurs most often



Example 3:
Locating Hazards; More Complex Example (See next slide)

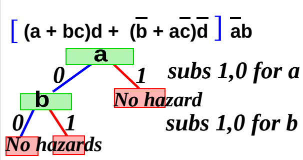
Equation. $F = [(a + bc)d + (\bar b + a\bar c)\bar d]\,\bar a b$

There is a, $\bar a$; b, $\bar b$; c, $\bar c$; and d, $\bar d$ in the expression.

All variables need checking

Overview: Avoid duplicating work.

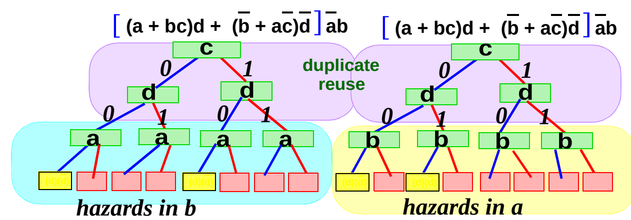
First fix a and b (they appear most often)
look for hazards in c and d



Then fix c and d

look for hazards in a and b

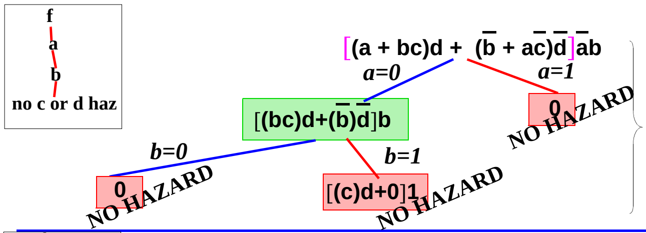
Result *from next page*
- no hazards in c or d.
- a and b may still have hazards.



Example 3: Locating Hazards; More Complex Example (cont)

Equation. $F = [(a + bc)d + (\bar{b} + a\bar{c})\bar{d}]\bar{a}b$

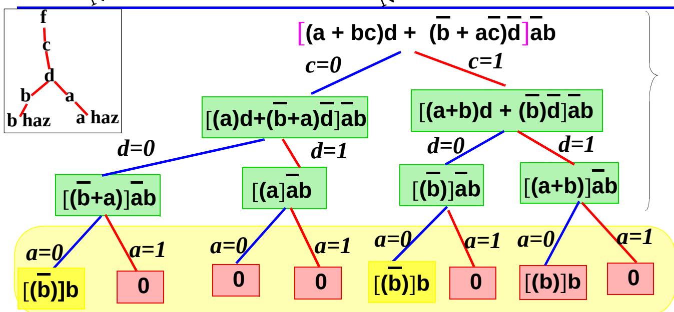
All variables need further checking because there is a, $\bar{a}$; b, $\bar{b}$; c, $\bar{c}$; and d, $\bar{d}$ in the equation.



Expand around a and b since they appear the most often.

This says c and d have no hazards for any combination of a and b.

No hazards in c or in d.



Make variables c and d static
Top 3 lines of calculation will be reused on next page.

Case 1:
a is static
check b for hazards

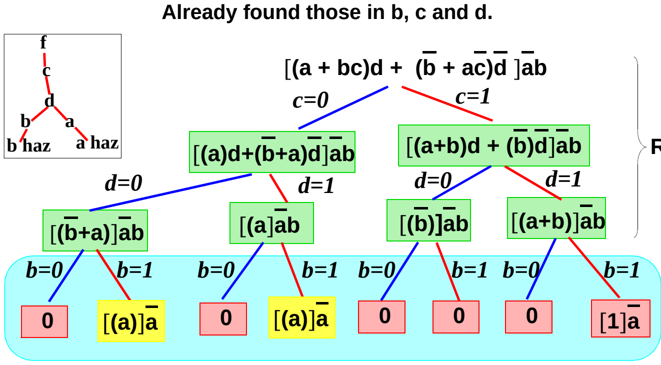
b has static-0 hazards when a,c,d=0,d,0

Example 3: More Complex Problem (Continued)

Equation. $F = [(a + bc)d + (\bar{b} + a\bar{c})\bar{d}]\bar{a}b$

Check for hazards in a

Already found those in b, c and d.



Make variables c and d static.
Allows reuse of work.

REPEAT OF LAST PAGE

Case 2:
b is static
check a for hazards

a has static-0 hazards when c,d,b=0,d,1

Notes

- **Start with the variables that cannot have hazards. It allows reuse.**
- **If you can't tell guess. Here we guessed c and d were static.**
- **Otherwise start with the variables with the most letters. See Example 3.**

Implementing Hazard Free Circuits

Sum-of-Product Circuits Have No Static-0 Hazards

Sum of products circuits always have an equation of the form

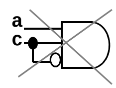
$F = abc + ab\bar{d} + ab\bar{c}d + \ldots\ldots\ldots + a\bar{b}c\bar{d}$

Static-0 hazards are like $c\bar{c}$. { $c + \bar{c}$ is static-1}

To get $c\bar{c}$ in F as above on must place c and $\bar{c}$ as inputs to the same AND gate.
This is ignorant.

Rule I:

Except for the gross carelessness of including terms like $ac\bar{c}$,
Σ of Π implementations have no static-0 hazards.



Sum-of-Product Circuits Have No Dynamic Hazards

Σ of Π circuit have equations of the form

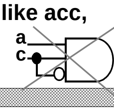
$F = abc + ab\bar{d} + ab\bar{c}d + \ldots\ldots\ldots + ab\bar{c}d + abc\bar{c}d$

Dynamic hazards are of the form $c\bar{c} + c$ or $(c+\bar{c})c$.
In F, try fixing a, b and d at any combination of 0 or 1.

A dynamic hazard in c, must have a term containing $c\bar{c}$.
In F above, one can only get a dynamic hazard by using the "ignorant" term $abc\bar{c}d$.

Thus Rule II is:

Except for the gross carelessness of including terms like $ac\bar{c}$,
Σ of Π implementations have no dynamic hazards.



Sum-of-Product Circuits Have Only Easily Eliminated Static-1 Hazards

Σ of Π circuits can still have static-1 hazards
They are easily found and removed using:
- a Karnaugh map,
- or algebraically.

.

FIG. 1-23 Map of function

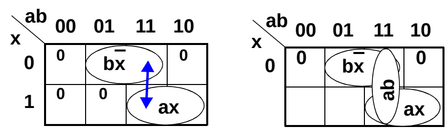
$F = b\bar{x} + ax$

It is Σ of Π
The hazards must all be static-1.

Hazard when a,b = 1,1.
Add term ab to mask the hazard.

$F = b\bar{x} + ax + ab$

Is shown on the right.



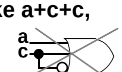
Product-of Sum Circuits Have No Static-1 Hazards

Π of Σ circuit equations are of the form

$F = (a+b+c)(a+b+\bar{d})(a+b+\bar{c}+d)(\ .\ .\ .\ .\ .\ .\ .)(a+b+\bar{c}+d)$

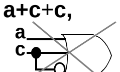
Static-1 hazards are of the form $c + \bar{c}$.
To get $c+\bar{c}$ in F one must place c and $\bar{c}$ as inputs to the same OR gate.
This is ignorant.

Except for the gross carelessness of including terms like $a+c+\bar{c}$, Π of Σ implementations have no static-1 hazards.



Product-of Sum Circuits Have No Dynamic Hazards

Except for the gross carelessness of including terms like $a+c+\bar{c}$, Π of Σ implementations have no dynamic hazards.



Product-of Sum Circuits Have Only Easily Eliminated Static-0 Hazards

Π of Σ circuits can still have static-0 hazards
They are easily found and removed using a Π of Σ Karnaugh map

Example: Single-Variable-Change Hazard-Free Circuit From a Map

A digital function defined by a map; FIG. 1-24(left).

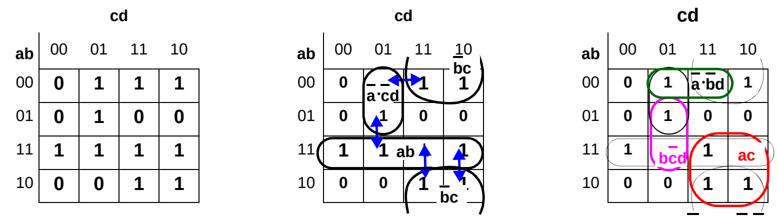
Choose a circling for the map; see FIG. 1-24 (middle),
←→ indicate the hazards.

$$F = a\cdot b + \bar{b}\cdot c + \bar{a}\cdot\bar{c}\cdot d$$

Then add circles which cover the arrows; FIG. 1-24(right).
The hazard free equation, on this final map, is -

$$F = a\cdot b + \bar{b}\cdot c + \bar{a}\cdot\bar{c}\cdot d + a\cdot c + b\bar{c}d + \bar{a}\cdot\bar{b}\cdot d$$

FIG. 1-24 Left) Example to be implemented as a hazard free circuit.
Centre) A possible Σ of Π looping showing hazards.
Right) The map with the hazards covered.



$F = a\cdot b + \bar{b}\cdot c + \bar{a}\cdot\bar{c}\cdot d$

$F = a\cdot b + \bar{b}\cdot c + \bar{a}\cdot\bar{c}\cdot d + a\cdot c + b\bar{c}d + \bar{a}\cdot\bar{b}\cdot d$

Since it is Σ of Π, <u>ALL</u> single-variable change hazards are removed

Hazards With Multiple Input Changes

Two-variable-change hazards

Two-variables changes, move two squares on the Karnaugh map.

Some 2-change hazards are maskable. (upper arrow in FIG. 1-25)
Many 2-variable hazards are not maskable. (lower arrow)

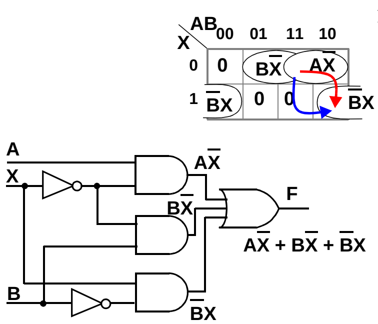


FIG. 1-25

Start at square A,B,X =1,1,0 (the tail of the arrows)
Change both B and X to move to square A,B,X =1,0,1 (the head of the arrows).

If B changes slightly before X, one travels the upper route.
The valley between $A\bar{X}$ and $\bar{B}X$ may glitch.
A masking term $A\bar{B}$ can cover the valley.
It only removes the glitch on the upper path.

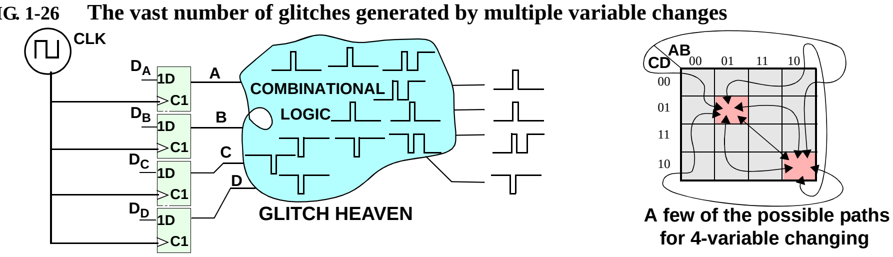
If X changes slightly before B, one takes the lower path.
This will always glitch.
It cannot be covered.
Covering the offending "0" changes the function.

When Are Hazards Important?

Multiple Variable Change Hazards are Plentiful

Take a synchronous circuit
Let 4 flip-flops change at once.
16 possible map squares.
Most paths will have function hazards

FIG. 1-26 The vast number of glitches generated by multiple variable changes



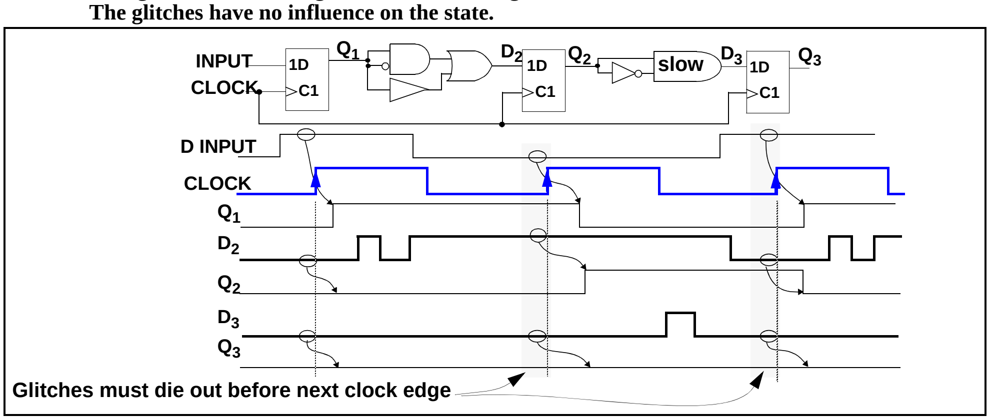
With 2 variables changing one is very likely to have hazards.
With more variables changing they are like waves in the ocean.

But very fast glitches will be absorbed inside gates (inertial delay)..

Hazards do not hurt synchronous circuits

In clocked logic, flip-flops only respond to the inputs slightly before the clock edge.
See the circles on the waveforms below.
All variables change shortly after the clock edge.
The clock cycle is made long enough so the glitches die out long before the clock edge.

FIG. 1-27 The flip-flops only respond in the circled region on the waveforms below.
A glitch at any other time will not influence state of the machine.
The glitches die out long before the clock edge.
The glitches have no influence on the state.

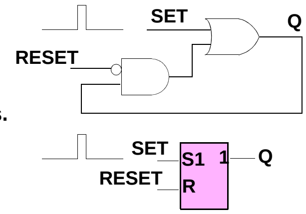


Hazards Kill Asynchronous Circuits

By asynchronous circuits, we mean ones with feedback that can latch signals.

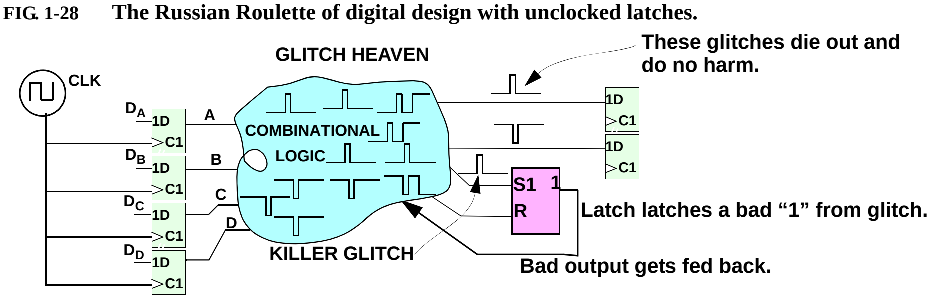
A glitch may causes a wrong value to be latched. All hazards must be eliminated, or proven harmless.

Analog simulation is used to prove it harmless.



Example: Placing an R-S Latch in a Synchronous Circuit

FIG. 1-28 The Russian Roulette of digital design with unclocked latches.



Outputs where hazards are of concern

Some displays are very sensitive to glitches.

Light emitting-diode displays may show slight “ghosts” in dim light.

Cathode-ray tube displays will often show any glitch-es on their input signals.

Memories

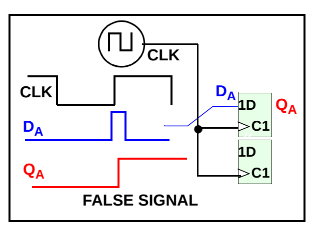
Memory chips are asynchronous latches, and are sensitive to glitches.

Memory control leads must be glitch free.

Glitches in asynchronous inputs to synchronous circuits

Asynchronous inputs to synchronous circuits must be hazard free.

An input glitch on the clock edge, may be captured as a valid input.



Summary Of Hazards

Single variable change hazards

Can be found and cured.

Multiple variable change hazards

Can be found
Are very plentiful
Cannot be cured in general, they are part of the logic.

Hazards are not important in truly synchronous circuits

Except for power consumption.

Don't mention false-paths.

Hazards are important in

Asynchronous circuits.

- **Latches and flip-flops**
- **Pulse catchers**
- **Debouncers**

- **Memory interface signals**
- **High speed displays**
- **Bus Control**

Appendix

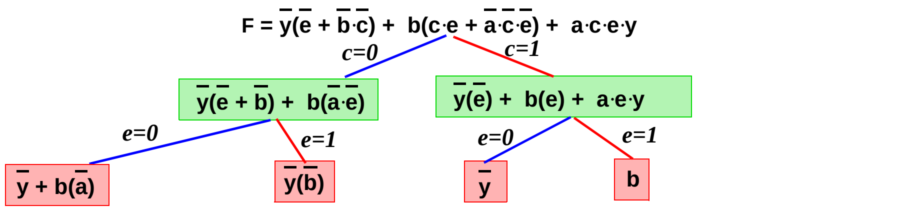
Example 4: Locating hazards with a binary tree
Steps for reducing the tree size
Example 5:
Problems
Common Errors

Locating Hazards; Example 4

Equation. $F = \bar{y}(\bar{e} + \bar{b}\cdot\bar{c}) + b(c\cdot e + \bar{a}\cdot\bar{c}\cdot\bar{e}) + a\cdot c\cdot e\cdot y$

Find all the single-variable change hazards.

- Select variables that can't have hazards
  Do them first.
  No obvious ones here. All variables appear as $\bar{X}$ and X
- Select the variables with the most letters
  Do them next.
  They will shorten the equation the fastest
  Use c and e.



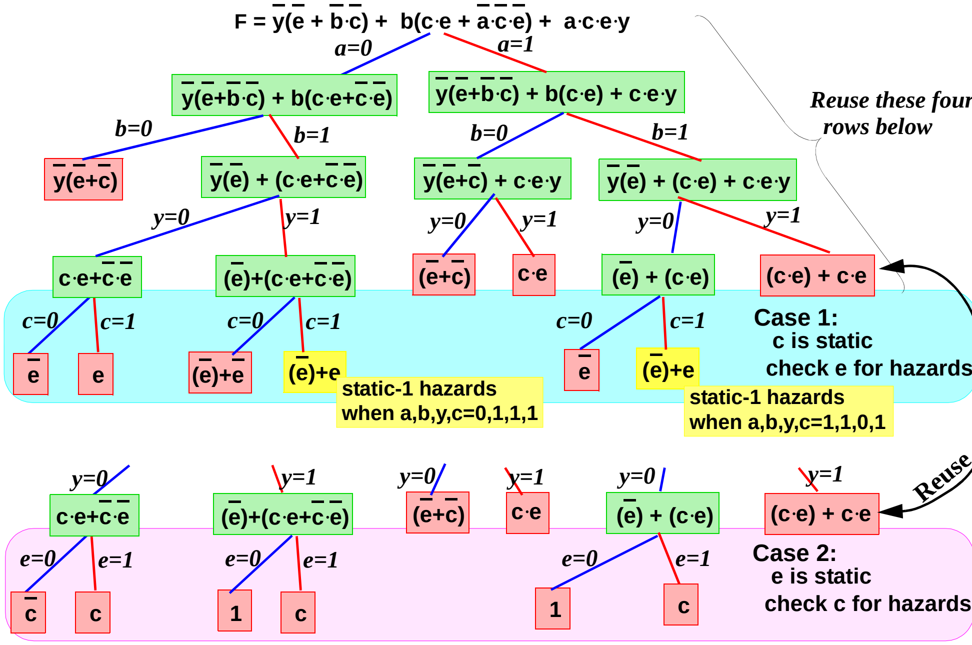
No hazards here
Thus a, b, and y cannot have hazards

- Now we know a, b, and y have no hazards
- Start a new tree doing a, b, and y first.

Steps for Reducing the Tree Size

1. When checking a variable, the order you used through the tree does not matter.
2. To save duplicating work:
   Put the variables that can't have hazards near the top of the tree
   That saves duplicating results.
3. After that expand the variables that have the most letters.
   They will simplify the equations in the fastest manner.
4. When you expand using a variable that might have hazards,
   you must make a new tree to check that variable.

A New Tree to Check e and c

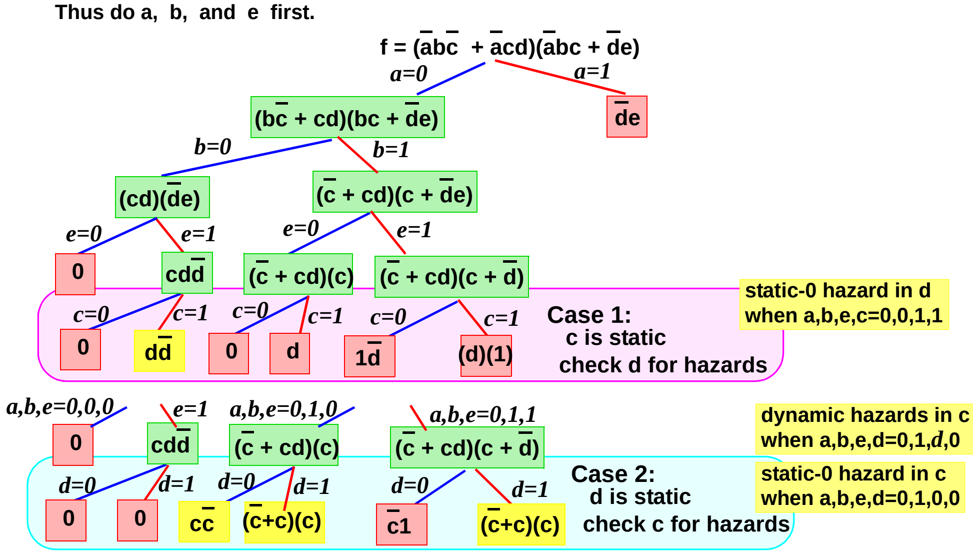


Locating Hazards; Example 5

Equation. F = (abc + acd)(abc + de)

Find all the single-variable change hazards.

- **Only c or d can have a hazard.**
  Thus do a, b, and e first.

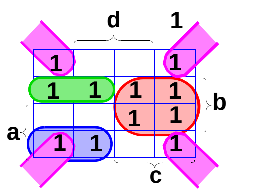


1. Problem

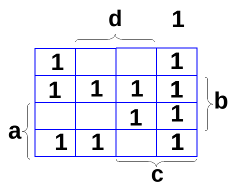
a) Place arrows on the K-map for F to show where all the single-variable-change static-1 hazards might occur.

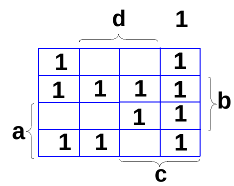
b) On another map show what AND terms must be added to F to mask these hazards.

c) Write the equation for the simplest F you can find that still has all hazards masked.
You may change the original four terms of F if it would be beneficial.



F = $a\cdot\bar{b}\cdot\bar{c} + bc + \bar{b}\cdot\bar{d} + \bar{a}b\bar{c}$





2. Problem

Given **G =** $b\cdot a + \bar{a}\cdot c + \bar{b}\cdot\bar{c}\cdot d$

(a) State with reasons, but without doing any calculation or map work:
i) How many static-0 hazards G has.
ii) How many dynamic hazards G has.

Given **G =** $b\cdot a\cdot g + \bar{a}\cdot c + \bar{b}\cdot\bar{c}\cdot d + e\cdot g\cdot d$

(b) Find all the single-variable-change hazards algebraically.

Glitches and Hazards in Digital Circuits ■ Locating Hazards; Example 5

Common Errors

- **Saying (A + B +** $\bar{A}$**D) with A=1 gives B**
- **Using law (D1) while you construct the binary tree.** $D\bar{A} + A(C + A) = D\bar{A} + AC + A\bar{A}$
  Here this added an extra dynamic hazard.
- **Forgetting wrap around when looking for hazards on a Karnaugh map.**
- **Trying to mask wrap arounds with no hazards, like** $C\bar{D}$ **with** $\bar{B}CD$