Name: ______________________________ Student Number: ______________

CARLETON UNIVERSITY

SELECTED FINAL EXAMINATION QUESTIONS

DURATION: 6 **HOURS**

Department Name & Course Number: ELEC 3908

Course Instructors: S. P. McGarry

Authorized Memoranda: Non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has twenty (20) pages.

This examination question paper **may not** be taken from the examination room.

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

SEE END OF EXAM FOR FORMULA & DATA SHEETS

WRITE YOUR NAME AND STUDENT NUMBER ON EACH PAGE

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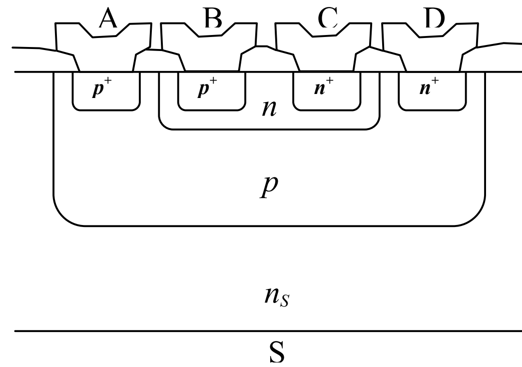
1. Consider a structure fabricated in silicon with the cross-section shown below.



a) The starting substrate has a doping of $n_s = 2\text{x}10^{14}$ cm^{-3}, the implant to form the *p*-region is $N_A = 8\text{x}10^{14}$ cm^{-3}, for the *n*-region it is $N_D = 5\text{x}10^{15}$ cm^{-3}, the n$^+$-region is $N_D^+ = 10^{18}$ cm^{-3} and the p^+-region is $N_A^+ = 5\text{x}10^{17}$ cm^{-3}. Calculate the carrier densities *p*, *n*, p^+ and n^+.

b) Assuming all the *PN* junctions act as isolated diodes and ignoring parasitic resistances, draw the equivalent circuit for this structure in terms of the contacts A, B, C, D and the substrate S. (i.e. draw how the diodes are connected to each other and A, B, C, D and S.)

c) Would it be possible to use this structure as a bipolar junction transistor (BJT)? If so, what type of transistor and which contacts would you choose to be the collector, base and emitter and why?

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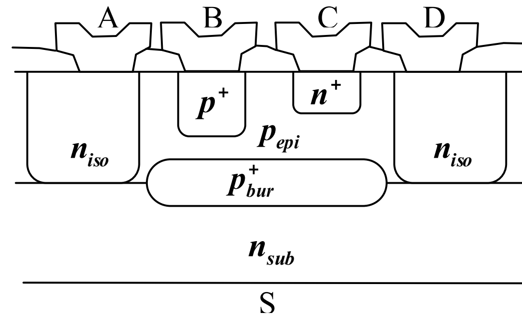
2. Consider a structure fabricated in silicon with the cross-section shown below.



a) What type of device does this structure define?

b) What is the purpose of the n_{iso} regions in this structure?

c) How many mask levels (i.e. patterning steps) are required to form this structure and what regions do they define?

d) The starting substrate has a doping of n_{sub} = 2x10^{14} cm^{-3}, the buried layer doping is p_{bur}^{+} = 5x10^{18} cm^{-3} and the epitaxial layer is grown with p_{epi} = 5x10^{16} cm^{-3}. The implant used for the n_{iso}-region it is N_D = 2x10^{17} cm^{-3}, the n^+-region is N_D^+ = 2x10^{18} cm^{-3} and the p^+-region is N_A^+ = 5x10^{17} cm^{-3}. Calculate the carrier densities n_{iso}, n^+ and p^+.

e) Assuming all the *PN* junctions act as isolated diodes and ignoring parasitic resistances, draw the equivalent circuit for this structure in terms of the contacts A, B, C, D and the substrate S. (i.e. draw how the diodes are connected to each other and A, B, C, D and S.)

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3. The Shockley-Read-Hall model uses the equation below to calculate the net recombination rate in a semiconductor.

$$U = \frac{n(x)p(x) - n_i^2}{\tau_0 \left(n(x) + p(x) + 2n_i\right)}$$

f) What is meant by “low-level injection”?

g) Under the conditions of low-level injection in a p-type material the above expression can be solved to give $n - n_{p0} = (n_0 - n_{p0})e^{-t/\tau_0} = \Delta n_0 e^{-t/\tau_0}$. If a *p*-type material is initially raised by Δn_0 under low-injection conditions how long will it take the excess carrier concentration to fall to $\Delta n_0/3$ if the minority carrier lifetime is τ_0 = 2x10^{-6} sec? How far, on average, will the carriers diffuse in this time?

h) What do the following imply with regards to the generation or recombination of carriers:

$U = 0$?

$U > 0$?

$U < 0$?

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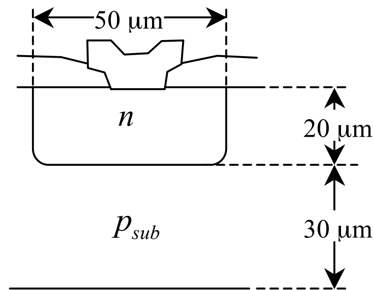
4. A deep-diffused junction substrate diode is formed as shown below with the starting substrate doping p_{sub}= 2x10^{17} cm^{-3} and an implant of N_D = 5x10^{17} cm^{-3} to form the n -region. The n -region extends for 100 μm into the page (to give an n-region area of 50 μm x 100 μm).



a) Assuming that the uniform doping approximation can be used and there is no current spreading, calculate the total series resistance, R_s, of the diode shown above.

b) If the process being used allows a maximum current density of J_{max} = 10^3 A/cm^2 what is the maximum current, I_{max}, that this diode can carry?

c) Using the results from (a) and (b), calculate the forward voltage, V_{Dx}, of this diode structure at the maximum current, I_{max}. (Assume L_p >> 20μm and L_n >> 30μm.)

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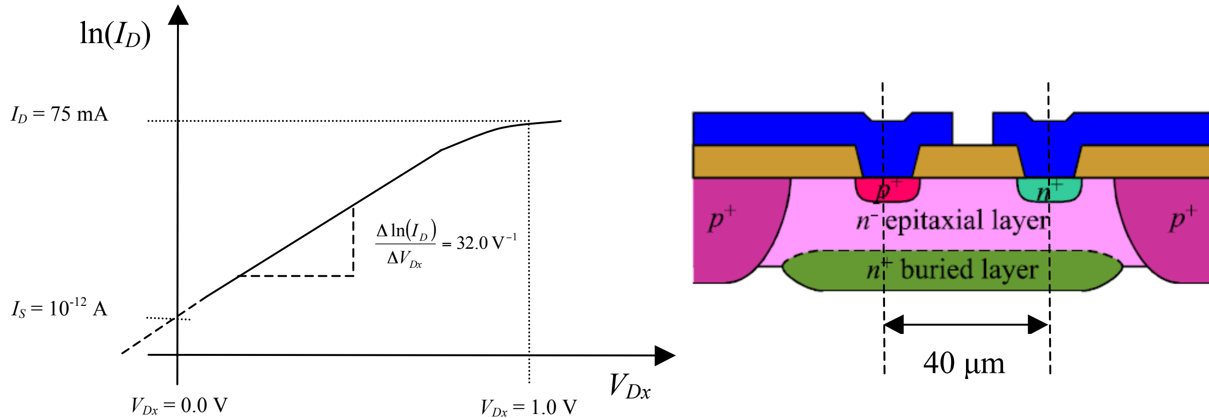
5. A epitaxial diode $\ln(I_D)$ *vs* V_{Dx} characteristic is measured at T = 300 K and plotted as shown below. The slope in the linear portion of the curve at $V_{Dx} > 3kT/q$ is found to be $\frac{\Delta \ln(I_D)}{\Delta V_{Dx}} = 32.0\ \text{V}^{-1}$ with an intercept of $I_S = 10^{-12}$ A. A point is measured at high current and found to be $I_D = 75$ mA at $V_{Dx} = 1.0$ V.



a) Extract the values of the series resistance, R_s, and ideality factor, n, for this diode from the $\ln(I_D)$ *vs* V_{Dx} characteristic.

b) The n+ buried layer is 2 µm thick, the contacts are 40 µm apart and 200 µm wide (into the page). Assume that the buried layer dominates the series resistance and that its n^+-doping is $N_D = 2\text{x}10^{18}\ \text{cm}^{-3}$. Using these values calculate the approximate value of R_s. (1 µm = 10^{-4} cm)

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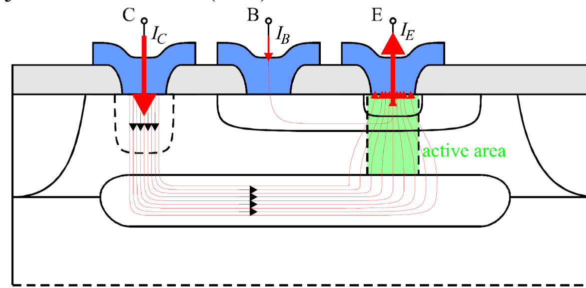
6. The structure of a bipolar junction transistor (BJT) is illustrated below.



a) What are the four regions of operation for a bipolar junction transistor (BJT)?

b) What is "transistor action" in a BJT?

c) Why the forward current gain, β_F, is larger than the reverse current gain, β_R, in a well-designed BJT.

d) What is the main physical cause of the Early effect in a BJT?

e) Why do we call a BJT a "minority carrier" device?

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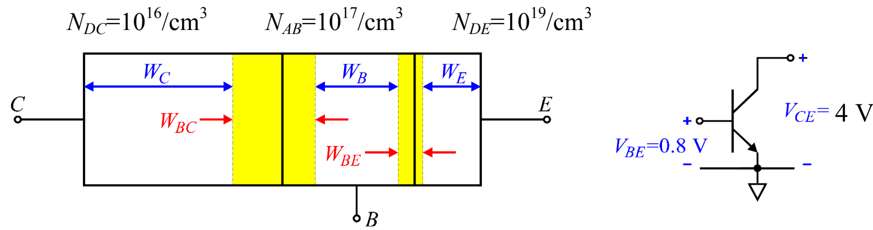
7. A bipolar junction transistor (BJT) has the parameters and biases shown in the diagram below. (T = 300 K)



i) The neutral region widths are W_C = 2µm, W_B = 1µm and W_E = 0.5µm. If the emitter area of the BJT above is 2µm by 10µm, what are the values of the base and collector currents? (You may use whatever approximations that are appropriate.)

j) What is the maximum field, $\boldsymbol{\mathcal{E}}_{depl\max}$, in the base-collector junction of the BJT above?

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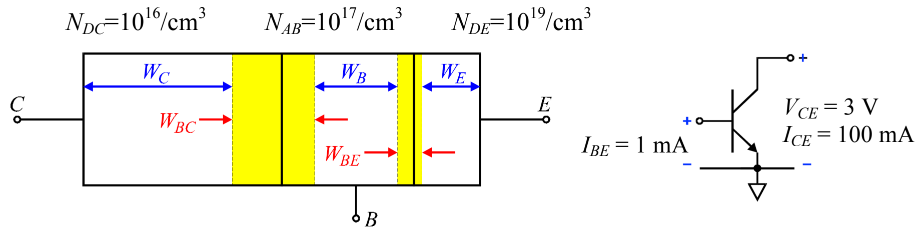
8. A bipolar junction transistor (BJT) has the parameters and currents shown in the diagram below. (T = 300 K)



a) If the neutral region width of the emitter is $W_E = 0.5\mu m$, what is the neutral region width of the base, W_B? (You must use the appropriate approximations.)

b) What is the collector-base breakdown voltage with the emitter open, BV_{CBO}, for the BJT shown above if it has a critical field of $\boldsymbol{\mathcal{E}}_{crit} = 3x10^5$ V/cm ?

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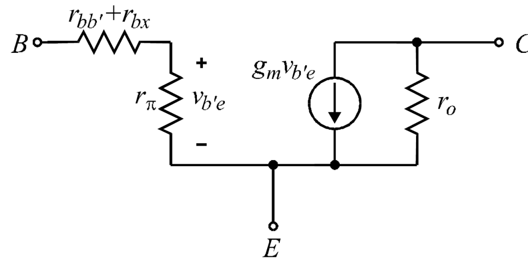
9. The small-signal hybrid-pi model for the bipolar transistor is shown below.



k) In what transistor operating range is this model normally used and what restrictions apply to the use of this model?

l) If the transistor collector current, I_C is 20 mA, what is the value of the transconductance, g_m, for this model? (V_{BE} >> 3kT, T = 300 K)

m) If the transistor collector current, I_C is 20 mA, what is the value of the output impedance, r_0, for this model (ignoring the Early effect)? (V_{BE} >> 3kT, T = 300 K)

n) If the transistor collector current I_C = 20 mA and the forward beta $\beta_F = 100$, what is the value of r_π for this model? (V_{BE} >> 3kT, T = 300 K)

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10. The maximum low-frequency voltage gain achievable using a FET is given by $G_{max} = g_m/g_o$.

a) Show that, in saturated mode, G_{max} is only dependent on the channel-shortening parameter, λ, and the biasing conditions (V_{GS}-V_T and V_{DS}) of the device.

b) What is G_{max} for V_{GS}-V_T = 1V and V_{DS} = 2V if $\lambda = 0.05\ V^{-1}$?

c) Find an expression for G_{max} if the FET is biased in triode mode.

d) What is G_{max} for V_{GS}-V_T = 2V and V_{DS} = 1V if $\lambda = 0.05\ V^{-1}$?

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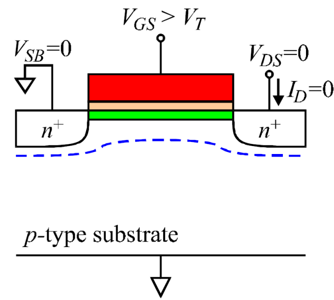
11. The cross section of a simple substrate *n*-channel MOSFET biased above threshold is illustrated below.



e) What is meant by "pinch-off" in a MOSFET and what happens to the channel when pinch-off occurs?

f) How do we add the effect of channel shortening to the MOSFET square law model when $V_{DS} > V_{DSsat}$?

g) A gate bias of V_{GS} = 2.5 V is applied to a MOSFET with a threshold voltage of V_T = 0.4 V and substrate doping of N_A = 5 x 10^{17} cm^{-3}. The gate oxide thickness is t_{ox} = 20 nm and the device has an effective channel length of 2 µm and width of 10 µm. If channel shortening can be ignored, what is the channel current, I_D, for V_{DS} = 1.5V ?

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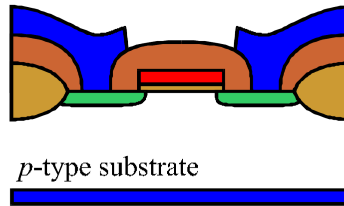
12. The cross section of a simple substrate MOSFET structure is illustrated below.



a) How many patterning steps are required to make the structure above and what features does each step define? (In the order in which they are processed.)

b) Why do we say that the source and drain implants are "self-aligned" to the gate in a MOSFET process?

c) We use the structure above to fabricate a MOSFET with a substrate doping of $N_A = 10^{16}$ cm^{-3} and a heavily doped p^+-polysilicon gate. Calculate the threshold voltage, V_T, if $t_{ox} = 25$ nm and $V_{SB} = 0$V. ($T = 300$K)

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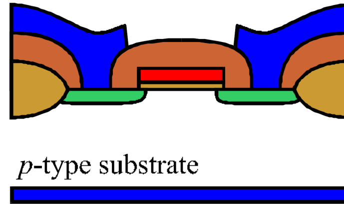
13. The cross section of a simple substrate MOSFET structure is illustrated below.



a) Explain briefly the difference between "drawn channel length" and "effective channel length".

b) What is the "short channel effect" on threshold voltage? What are the two main techniques used to mitigate this effect?

c) What is drift conduction in a semiconductor? How does drift conduction in a semiconductor change at high electric fields?

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14. There are three voltage components in the equation used to calculate the basic threshold voltage, V_{T0}, for a MOSFET.

$$V_{T0} = V_{FB} + 2\phi_B - \frac{\hat{Q}_{dep}}{\hat{C}_{ox}} = V_{FB} + 2\phi_B + \frac{\sqrt{2q\varepsilon_{Si}N_A(2\phi_B)}}{\hat{C}_{ox}}$$

d) A simple n-MOSFET process starts with a substrate doping of $p_{sub} = 5\text{x}10^{16}$ cm^{-3} uses a gate oxide (SiO_2) with a thickness of 30 nm and a heavily doped p^+ polysilicon gate. Calculate the basic threshold voltage, V_{T0}, for an *n*-channel MOSFET in this process. ($T = 300\text{K}$)

e) Briefly describe how the threshold voltage is changed if a voltage is applied between the source of the MOSFET and the substrate (bulk).

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15. A MOSFET has a layout as illustrated in the diagram below. There is 0.5 μm of lateral diffusion under the gate from the source and drain implants and the oxide thickness is t_{ox} = 20 nm. The source and drain are implanted at $N_D = 10^{18}$ cm^{-3} into the substrate having an initial doping of $N_A = 5\text{x}10^{16}$ cm^{-3}.

1 μm/division

(a) Calculate the intrinsic gate-source capacitance, C_{GS}^{int}, for this MOSFET structure assuming it is operating in saturated mode.

(b) Calculate the depletion gate-source capacitance, C_{GS}^{dep}, for this device assuming that the bottom depletion capacitance dominants (i.e. all other non-intrinsic capacitances can be neglected) and V_{SB} = 0V, z_{SB} = ½.

(c) The transit frequency for a FET is given by $f_\tau \approx \dfrac{g_m}{2\pi C_{GS}^{tot}} \approx \dfrac{g_m}{2\pi\left(C_{GS}^{\text{int}} + C_{GS}^{dep}\right)}$. If V_{GS}-V_T = 1V and channel shortening can be ignore, what is the transit frequency for this device? (Using the results from (a) and (b).)

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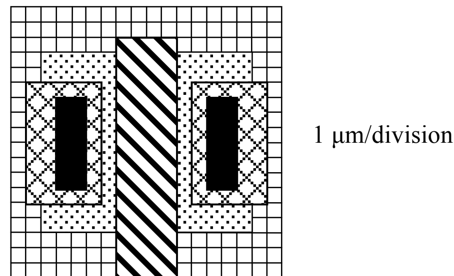
16. A MOSFET has a layout as illustrated in the diagram below. There is 0.5 μm of lateral diffusion under the gate from the source and drain implants.



(d) The source and drain are implanted at $N_D = 10^{18}$ cm^{-3} into the substrate having an initial doping of $N_A = 5\text{x}10^{16}$ cm^{-3}. Assuming that the sidewall capacitances can be ignored relative to the bottoms, calculate the depletion capacitance of the source and drain if $V_{DS} = 5$V, $V_{SB} = 0$V, $z_{SB} = z_{DB} = 1/2$?

(e) Under the same doping and biasing conditions as in (a), how far under the gate will the sidewall depletion regions of the source and drain extend?

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Equations

Ideal Diode: $I_D = I_S\left(e^{qV_D/kT} - 1\right)$

with depletion region GR: $I_D = I_S\left(e^{qV_D/nkT} - 1\right)$

with series resistance & GR: $I_D = I_S\left(e^{q(V_{Dx} - I_D R_s)/nkT} - 1\right)$ where $V_{Dx} = V_D + I_D R_s$

Shockley-Reed-Hall: $U = \dfrac{n(x)p(x) - n_i^2}{\tau_0\left(n(x) + p(x) + 2n_i\right)}$

Einstein Relations: $D_n \equiv \dfrac{kT}{q}\mu_n, \quad D_p \equiv \dfrac{kT}{q}\mu_p$

Diffusion Length: $L_n \equiv \sqrt{D_n \tau_0}, \quad L_p \equiv \sqrt{D_p \tau_0}$

Saturation Current Density: $J_S = J_{Sh} + J_{Se} = \dfrac{qD_p p_{n0}}{w_n} + \dfrac{qD_n n_{p0}}{w_p}$, for thin n and p

$J_S = J_{Sh} + J_{Se} = \dfrac{qD_p p_{n0}}{L_p} + \dfrac{qD_n n_{p0}}{L_n}$, for thick n and p

Gaussian Integral: $\int_0^\infty e^{-\frac{x^2}{2\sigma^2}} = \sqrt{\dfrac{\pi}{2}}\sigma$

Resistivity: $\rho \equiv \left(\dfrac{1}{\rho_n} + \dfrac{1}{\rho_p}\right)^{-1} = \left(\sigma_n + \sigma_p\right)^{-1} = \left(qn\mu_n + qp\mu_p\right)^{-1}, \quad R = \dfrac{\rho \cdot l}{A}$

Poisson's Equation: $-\dfrac{d^2\psi(x)}{dx^2} = \dfrac{d\mathcal{E}(x)}{dx} = \dfrac{\rho(x)}{\varepsilon_{Si}}$

Excess Charge Density in a Diode: $\rho(x) = q\left[p(x) - n(x) + N_D - N_A\right]$

Built-In Voltage: $V_{bi} = \dfrac{kT}{q}\ln\left(\dfrac{N_A N_D}{n_i^2}\right)$

Depletion Width: $W = \sqrt{\dfrac{2\varepsilon_{Si}}{q}\left(\dfrac{1}{N_A} + \dfrac{1}{N_D}\right)\left(V_{bi} - V_D\right)}, \quad x_n = W\left(\dfrac{N_A}{N_A + N_D}\right), \quad x_p = W\left(\dfrac{N_D}{N_A + N_D}\right)$

Maximum Electric Field: $\left|\mathcal{E}_{depl\ \max}\right| = \sqrt{\dfrac{2q}{\varepsilon_{Si}}\left(\dfrac{N_A N_D}{N_A + N_D}\right)\left(V_{bi} - V_D\right)}$

Avalanche Multiplication Factor: $M = \dfrac{1}{1 - p_{ii}}$

Impact Ionization Probability: $p_{ii} = \left(\dfrac{\left|\mathcal{E}_{depl\ \max}\right|}{\mathcal{E}_{crit}}\right)^{\nu}, \quad 3 < \nu < 6$

Diode Junction Conductance: $g_D = \dfrac{dI_D}{dV_D} = \dfrac{q}{nkT} I_S e^{qV_D/nkT} \approx \dfrac{q}{nkT} I_D$

Diode Junction Capacitance (per area): $\hat{C}_{depl}(V_D) = \dfrac{d\hat{Q}_{depl}}{dV_D} = \dfrac{d\hat{Q}_{depl}}{dW}\dfrac{dW}{dV_D} = \left[-q\dfrac{N_A N_D}{N_A + N_D}\right]\left[-\dfrac{\varepsilon_{Si}}{Wq}\dfrac{N_A + N_D}{N_A N_D}\right] = \dfrac{\varepsilon_{Si}}{W(V_D)}$

Charge Control Equation: $\dfrac{dQ_p(t)}{dt} = i_D(t) - \dfrac{Q_p(t)}{\tau_0}$

Charge Storage Time: $t_s = \tau_0 \ln\left(1 - \dfrac{I_F}{I_R}\right) \approx \tau_0 \ln\left(1 - \dfrac{V_F}{V_R}\right)$ for $|V_F|, |V_R| >> |V_D|$

Heat Flow: $\Phi = -\kappa\dfrac{dT}{dx}, \quad T_{rise} = P_D R_{TH}$

BJT Injection Model Currents: $I_C = I_{pC} + I_{nB}, \quad I_B = -I_{pC} + I_{pE}, \quad I_E = I_{nB} + I_{pE}$

$$I_C = -\frac{qA_E D_{pC} p_{Co}}{W_C}\left(e^{qV_{BC}/kT} - 1\right) + \frac{qA_E D_{nB} n_{Bo}}{W_B}\left(e^{qV_{BE}/kT} - e^{qV_{BC}/kT}\right)$$

$$I_E = \frac{qA_E D_{nB} n_{Bo}}{W_B}\left(e^{qV_{BE}/kT} - e^{qV_{BC}/kT}\right) + \frac{qA_E D_{pE} p_{Eo}}{W_E}\left(e^{qV_{BE}/kT} - 1\right)$$

$$I_B = \frac{qA_E D_{pC} p_{Co}}{W_C}\left(e^{qV_{BC}/kT} - 1\right) + \frac{qA_E D_{pE} p_{Eo}}{W_E}\left(e^{qV_{BE}/kT} - 1\right)$$

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BJT Ebbers-Moll Model:

$$I_{ES} \equiv \frac{qA_E D_{nB} n_{Bo}}{W_B} + \frac{qA_E D_{pE} p_{Eo}}{W_E} \qquad I_{CS} \equiv \frac{qA_E D_{nB} n_{Bo}}{W_B} + \frac{qA_E D_{pC} p_{Co}}{W_C}$$

$$\alpha_F \equiv \frac{qA_E D_{nB} n_{Bo}/W_B}{qA_E D_{nB} n_{Bo}/W_B + qA_E D_{pE} p_{Eo}/W_E} \qquad \alpha_R \equiv \frac{qA_E D_{nB} n_{Bo}/W_B}{qA_E D_{nB} n_{Bo}/W_B + qA_E D_{pC} p_{Co}/W_C}$$

$$I_E = I_{ES}\left(e^{qV_{BE}/kT} - 1\right) - \alpha_R I_{CS}\left(e^{qV_{BC}/kT} - 1\right)$$

$$I_B = \left(1 - \alpha_F\right) I_{ES}\left(e^{qV_{BE}/kT} - 1\right) + \left(1 - \alpha_R\right) I_{CS}\left(e^{qV_{BC}/kT} - 1\right)$$

$$I_C = \alpha_F I_{ES}\left(e^{qV_{BE}/kT} - 1\right) - I_{CS}\left(e^{qV_{BC}/kT} - 1\right)$$

BJT Base Diffusion Capacitance:

$$C_\pi = \tau_B g_m, \quad \tau_B = \frac{W_B^2}{2D_{nB}}$$

BJT Transit Frequency:

$$f_\tau = \frac{1}{2\pi\left[\left(C_{depBC} + C_{depBE}\right)/g_m + \tau_B\right]}$$

MOSFET Gate Capacitance: (per unit area)

$$\hat{C}_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}}$$

Drift Conduction:

$$J = qnv_n + qpv_p = \left(qn\mu_n + qp\mu_p\right)\mathcal{E} = \sigma\mathcal{E}$$

Carrier Density Relative to E_F

$$n = N_C e^{-(E_C - E_F)/kT}, \quad p = N_V e^{-(E_F - E_V)/kT}$$

Flat Band Voltage:

$$V_{FB} = \Phi_{MS}/q = \left(\Phi_M - \Phi_S\right)/q$$

Bulk Potential (p-type):

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

MOSFET Threshold Voltage:

$$\boldsymbol{V_{T0} = V_{FB} + 2\phi_B - \frac{\hat{Q}_{dep}}{\hat{C}_{ox}} = V_{FB} + 2\phi_B + \frac{\sqrt{2q\varepsilon_{Si} N_A (2\phi_B)}}{\hat{C}_{ox}}}$$

MOSFET Threshold Modulation:

$$V_T = V_{To} + \gamma\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right)$$

$$V_{To} = V_{FB} + 2\phi_B + \frac{\sqrt{2q\varepsilon_{Si} N_A (2\phi_B)}}{\hat{C}_{ox}} \qquad \gamma = \frac{\sqrt{2q\varepsilon_{Si} N_A}}{\hat{C}_{ox}}$$

MOSFET Square Law Model:

$$I_D = \bar{\mu}_n \hat{C}_{ox}\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right)\left(1 + \lambda V_{DS}\right) \quad V_{GS} \ge V_T, V_{DS} \le V_{DS,sat}$$

$$= \bar{\mu}_n \hat{C}_{ox}\frac{W}{L}\left(\frac{\left(V_{GS} - V_T\right)^2}{2}\right)\left(1 + \lambda V_{DS}\right) \quad V_{GS} \ge V_T, V_{DS} \ge V_{DS,sat}$$

Channel shortening depletion charge

$$\hat{Q}'_{dep} = \hat{Q}_{dep}\left[1 - \underbrace{\frac{x_J}{2L}\left(\sqrt{1 + \frac{2W_S}{x_J}} + \sqrt{1 + \frac{2W_D}{x_J}} - 2\right)}_{\text{correction term for trapezoidal area}}\right]$$

$$W_S \approx \sqrt{\frac{2\varepsilon_{Si}}{qN_A}\left(2\phi_B + V_{SB}\right)} \quad , \quad W_D \approx \sqrt{\frac{2\varepsilon_{Si}}{qN_A}\left(2\phi_B + V_{DB}\right)}$$

MOSFET Transconductance: (saturated)

$$g_m \equiv \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}} = \bar{\mu}_n \hat{C}_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)\left(1 + \lambda V_{DS}\right)$$

MOSFET Output Conductance: (saturated)

$$g_o \equiv \left.\frac{dI_D}{dV_{DS}}\right|_{V_{GS}} = \bar{\mu}_n \hat{C}_{ox}\frac{W}{L}\frac{\left(V_{GS} - V_T\right)^2}{2}\lambda$$

MOSFET Depletion Capacitances:

$$C_{SB} = \underbrace{\frac{C'_{depSw} P_S}{\left(1 + V_{SB}/V_{biSB}\right)^{z_{SB}}}}_{\text{sidewall}} + \underbrace{\frac{\hat{C}_{depBot} A_S}{\left(1 + V_{SB}/V_{biSB}\right)^{z_{SB}}}}_{\text{bottom}} \quad C_{DB} = \underbrace{\frac{C'_{depSw} P_D}{\left(1 + V_{DB}/V_{biDB}\right)^{z_{DB}}}}_{\text{sidewall}} + \underbrace{\frac{\hat{C}_{depBot} A_D}{\left(1 + V_{DB}/V_{biDB}\right)^{z_{DB}}}}_{\text{bottom}}$$

MOSFET Overlap Capacitances:

$$C_{GS,ovl} = C_{GD,ovl} = \frac{\varepsilon_{ox}}{t_{ox}} x_{ovl} W$$

MOSFET Intrinsic Capacitances: $\left(V_{DS} \le V_{DS,sat}\right)$

$$C_{GS} = \frac{2}{3}C_{ox}\left[1 - \left(\frac{\left(V_{GS} - V_T\right) - V_{DS}}{2\left(V_{GS} - V_T\right) - V_{DS}}\right)^2\right], \quad C_{GD} = \frac{2}{3}C_{ox}\left[1 - \left(\frac{\left(V_{GS} - V_T\right)}{2\left(V_{GS} - V_T\right) - V_{DS}}\right)^2\right]$$

MOSFET Velocity Saturation Model:

$$v = \frac{\mu_o \mathcal{E}}{1 + \mathcal{E}/\mathcal{E}_{crit}}$$

MOSFET Current with Vel. Sat.

$$I_D = \bar{\mu}_n \hat{C}_{ox}\frac{W}{L\left(1 + V_{DS}/\left(L\mathcal{E}_{crit}\right)\right)}\left(\frac{\left(V_{GS} - V_T\right)^2}{2}\right)\left(1 + \lambda V_{DS}\right) \quad \text{saturation}$$

Name: ______________________________ Student Number: ____________

Physical Constants and Material Properties

Quantity	Symbol	Value
Angstrom Unit	Å	10^{-8} cm = 10^{-10} m
Boltzmann's Constant	k	8.62×10^{-5} eV/K
		1.381×10^{-23} J/K
Electronic Charge	q	1.602×10^{-19} C
Electron Volt	eV	1.602×10^{-19} J
Electron Rest Mass	m_o	9.11×10^{-31} kg
Free Space Permittivity	ε_o	8.854×10^{-14} F/cm
Plank's Constant	h	6.626×10^{-34} J-s
		4.14×10^{-15} eV-s
Thermal Voltage at 300K	kT/q	0.0259 V

Properties of Silicon at 300K

Quantity	Symbol	Value
Intrinsic Carrier Concentration	n_i	1.45×10^{10} cm^{-3}
Effective Densities of States	N_v	1.08×10^{19} cm^{-3}
	N_c	2.8×10^{19} cm^{-3}
Electron Affinity	χ^{Si}	4.05 eV
Energy Gap	E_g	1.08 eV
Bulk Electron Mobility	μ_n	1350 cm^2/V-s
Bulk Hole Mobility	μ_p	470 cm^2/V-s
Surface Electron Mobility	$\overline{\mu_n}$	520 cm^2/V-s
Permittivity	ε_{Si}	$11.7\varepsilon_o$

Properties of Silicon Dioxide

Quantity	Symbol	Value
Permittivity	ε_{ox}	$3.9\varepsilon_o$